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TITLE : LIST OF INFORMED PATENTS (ISSUE 4)

This document lists up the patents which have been informed the Specialists Group before November 6, 1989 as being relevant to either of the nx384 kbit/s Flexible Hardware specification (Doc. #249), the current Rec. H.261 (Blue Book) or the px64 kbit/s Flexible Hardware specification (Annex 4 to Doc. #540R).

The following documents are referred to;

#124 (BT, GEC)
#161 (NTT, KDD, NEC, FUJITSU)
#172 (USA)
#209 (PICTEL)
#238 (NTT, KDD, NEC, FUJITSU)
#262 (BT)
#278 (CLI)
#368 (NTT, KDD, NEC, FUJITSU)
#371 (BT)
#383 (PKI)
#388 (SWEDEN)
#398 (AEG)
#483 (CNET)
#494 (BELLCORE)
#502 (FINLAND)
#521 (BT)

It should be noted that this list is simply reproduction of informed patents, not mentioning to what extent these patents are relevant to the draft revision of Recommendation H.261 (Doc. #572).

The list also includes those patents which may be related to the implementation of the specification. It should also be noted that this categorization is tentative.

RELEVANT PATENTS

US 3,632,865 (Jan. 4, 1972)
PREDICTIVE VIDEO ENCODING USING MEASURED SUBJECTIVE VELOCITY
B. Haskell, J.O. Limb
Bell Telephone Laboratories
- Motion compensated interframe prediction.
- One vector per moving region.

US 3,679,821 (July 25, 1972)
TRANSFORM CODING OF IMAGE DIFFERENCE SIGNALS
M.R. Shroeder
Bell Telephone Laboratories
- Prediction errors are transformed, quantized.

US 4,281,344 (July 28, 1981)
VIDEO INTERFRAME TRANSFORM CODING TECHNIQUE
F.W. Mounts, A.N. Netravali
Bell Telephone Laboratories
- Interframe prediction errors are transformed. Non significant error pels are replaced by some significant pels, thus number of transmitted coefficients are reduced.
- Shares common idea with variable blocksize transform.

US 3,553,361 (Jan. 5, 1971)
CONDITIONAL REPLENISHMENT VIDEO SYSTEM SAMPLE GROUPING
US 3,553,362 (Jan. 5, 1971)
CONDITIONAL REPLENISHMENT VIDEO SYSTEM WITH RUN LENGTH CODING OF POSITION
F.W. Mounts
Bell Telephone Laboratories
- Conditional replenishment with PCM.
- Number of consecutive significant pels are coded with RLC/EOR.

US 3,609,244 (Sep. 28, 1971)
CONDITIONAL REPLENISHMENT VIDEO SYSTEM WITH VARIABLE LENGTH ADDRESS CODE
F.W. Mounts
Bell Telephone Laboratories
- Address of significant samples are transmitted as the length of the interval between the location of its respective sample and the of the group.
- Address is variable length coded.

US 4,541,012 (Jan. 4, 1982) / EP 0,084,270
VIDEO BANDWIDTH REDUCTION SYSTEM EMPLOYING INTERFRAME BLOCK DIFFERENCING AND TRANSFORM DOMAIN CODING
A.G. Tesher
Compression Labs, Inc.
- Block based conditional replenishment according to interframe difference.
- Significant blocks are transformed.
- Relevant to the 'intra mode' of the Flexible Hardware.

JP 57-041069-A (Mar. 6, 1982)
INTERFRAME-ENCODING SYSTEM
H.Kuroda, T.Matsuoka
NTT
- Demand refresh

JP 60-029068-A (Feb. 14, 1985)
TRANSMISSION ERROR DETECTION SYSTEM
M. Nishiwaki, S. Tsugane, H. Kuroda, N. Mukawa, K. Matsuda, M. Hiraoka
NEC, NTT, FUJITSU
- Parity check between frame memory contents in the coder and decoder for demand refresh.

US XXXXXX (applied Jan. 7, 1986)
PictureTel Corp.
- Filtering control of the motion compensated block by sending side information.

JP 61-288678-A (Dec. 18, 1986)
QUANTIZING NOISE SUPPRESSING SYSTEM IN INTERFRAME CODING
H. Kuroda, H. Hashimoto
NTT
- Motion vector control of loop filter

US 4,562,466 (Dec. 31, 1985)
DIGITAL DATA TRANSMISSION/RECEPTION HAVING ADAPTIVE ERROR CONTROL
C.S. Clapp, D.P. Devimeux, JC.R. Jolivet, A.Riou, N.L. Shilston
BT
- Lines of the raster are numbered cyclically in groups of 8, the numbers being part of line synchronizing code words

US 4,698,672 (Dec. 6, 1987)
CODING SYSTEM FOR REDUNDANCY REDUCTION
W. Chen, D.J. Klenke
CLI
- Two runlength coding codes, one is for the run followed by the first non-zero value, the second is for the run followed by other non-zero values

JP 63-121374-A (May 25, 1988)
MOTION COMPENSATED INTERFRAME CODING SCHEME
K. Matsuda, Y. Kato, J. Koike, M. Ohta et al
NTT, KDD, NEC, FUJITSU
- Motion vector control of the loop filter

JP 63-121321-A (May 25, 1988)
ENCODING SYSTEM CAPABLE OF ACCOMPLISHING A HIGH EFFICIENCY BY ANTERIOR AND/OR POSTERIOR PROCESSING TO QUANTIZATION
J. Koike, Y. Kato, M. Ohta, K. Matsuda
NTT, KDD, NEC, FUJITSU
- Multiple VLCs
- Last non-zero trick

XXXXXX (filed 19/4/86, 18/6/86, 8/11/86)
HYBRID CODER WITH DIGITAL LOW-PASS-FILTER CONTROLLED BY THE MOTION VECTOR AND/OR THE QUANTIZER INDEX
PKI

XXXXXX (filed 13/9/86, 8/11/86, 23/5/87)
BITRATE REDUCTION BY A TWO-DIMENSIONAL CODING TABLE FOR ENCODING THE QUANTIZER INDICES IN A HYBRID CODER
PKI

XXXXXX (filed 6/7/87, 10/8/87, 28/12/87)
REDUCTION OF SIDE INFORMATION IN A HYBRID CODER BY MACRO BLOCKS
PKI

XXXXXX (filed Sweden: 1987/02/20, Europe: 1988/02/11, USA: 1988/02/17)
END OF BLOCK TRICK
STA

DE 3629 472 A1 (29.6.86)
EP 0259 562 A1
US 07-090,875
G. Kummerfeldt, F. May, W. Wolf
AEG
- Adaptive prediction among block displacements, object related displacement vector calculation, nullification of the displacement, and nullification of the prediction

DE 30 29 190 (01.08.80)
F. May
AEG
- A hybrid coding scheme with blockwise cosine transform and adaptive quantization in which a frame to frame prediction coefficient is computed, quantized and transmitted.

86 05 213 (April 86)
NON-LINEAR QUANTIZATION TECHNIQUE
CNET

86 07 713 (May 86)
VARIABLE BLOCKSIZE TECHNIQUE
CNET

Bellcore Patent Application No. 221
METHOD AND APPARATUS FOR LOW BIT-RATE INTERFRAME VIDEO CODING
H. Gharavi

In accordance with the present invention, the two-dimensional blocks of m x m pel data at the input to the hybrid-type of encoder are subdivided, after subtracting the corresponding block data from the previous frame, into smaller sub-blocks of size n x n ($n < m$). Transformation within the loop of the hybrid coder is then performed on a sub-block basis. After transformation and quantization, the block is reconstructed and the coefficients of the block transmitted to the receiver on a block by block basis, together with the block overhead data. This overhead data includes block classification (static or dynamic block) and the block matching motion estimation of a dynamic block which are both performed on the main block basis.

4,717,957 (December 5, 1985)
VIDEO COMPRESSION METHOD
VISTACOM
- Application Number 899,291

Note: Block matching motion compensation scheme first appeared in an IECEJ convention record published in July 1974 (July 25-27). The paper was authored by Y. Taki, M. Hatori and S. Tanaka (Tokyo University). The scheme was not filed as a patent.

IMPLEMENTATION METHODS

The following patents may not be directly relevant to the Flexible Hardware specification or draft H.261 but describe implementation methods.

EP 113514-A (Nov. 30, 1982)
TELEVISION SIGNAL TRANSMISSION SYSTEM USING CONDITIONAL REPLENISHMENT - USES DIFFERING SCANNING RATES FOR TRANSMITTER AND RECEIVER WHICH USES STANDARD RATE
M.D. Carr, D.G. Morrison, R.C. Nicol
BT
- Asynchronous operation between coder and decoder

EP 103380-A (July 23, 1982)
TRANSMISSION OF VIDEO INFORMATION USING CONDITIONAL REPLENISHMENT - HAS DATA FED TO PATH AT CONSTANT RATE FROM ENCODER BUFFER AND RECEIVED AT DECODER BUFFER, AND DATA READ AT UNEVEN RATE FROM BUFFER
JC.R. Jolivet, D.P. Devimeux, S.K. Clapp, A. Riou, N.L. Shilston
BT
- Marker signals are stored in an auxiliary buffer store for reference by the reading device.

JP 55-158784-A (Dec. 10, 1980)
INTER-FRAME CODING DEVICE
A. Hirano
NEC
- Multi-step motion vector detection

JP 56-143776-A (Nov. 9, 1981)
INTERFRAME ENCODER
A. Hirano
NEC
- Multi-step motion vector detection with use of the previous frame motion vector as the first step

JP 57-037988-A (Mar. 2, 1982)
TELEVISION SIGNAL ENCODING EQUIPMENT
A. Hirano
NEC
- Matching error accumulation method using quantized values

JP 58-107785-A (June 27, 1983)
ENCODER BETWEEN MOVEMENT COMPENSATION FRAMES
A. Hirano
NEC
- Use of forced simple interframe prediction

JP 60-146588-A (Aug. 2, 1985)
SYSTEM AND DEVICE FOR ENCODING ANIMATION PICTURE SIGNAL
J. Ooki
NEC
- Halting of motion compensation in case of update operation

XXXXXX (applied 9 July 1987)
CLASSIFIER IMPLEMENTATION
BT
- Circuit to find the optimum order of transmission for a set of transform coefficients

JP 63 238783-A (Oct. 4, 1988)
IMAGE CODING SYSTEM CAPABLE OF MONITORING AN AMOUNT OF INFORMATION BY FORMING A HISTOGRAM
Y. Hatori, N. Mukawa, T. Koga, K. Matsuda
NTT, KDD, NEC, FUJITSU
- Feed-forward coding control using data generation estimation

JP 63-121372-A (May, 25, 1988)
MOVING IMAGE SIGNAL CODING SYSTEM
Y. Hatori, N. Kato, M. Ohta, Y. Kosugi
NTT, KDD, NEC, FUJITSU
- Significant/insignificant and intra/inter block decision

JP 63-120570-A (May 24, 1988)
DECODING DEVICE CAPABLE OF PRODUCING A DECODED VIDEO SIGNAL WITH A REDUCED DELAY
M. Nishiwaki, N. Kato, Y. Hatori
NTT, KDD, NEC
- Receiving buffer control method

XXXXXX (applied 3 August 1987)
TRANSFORM CODING
BT
- Omission of higher sequency transform coefficients

XXXXXX (applied 23 September 1987)
VIDEO MULTIPLEX
BT
- Multiplexing of blocks of image data and associated overhead

XXXXXX (applied 25 September 1987)
MOTION ESTIMATION
BT
- All comparisons involving a line n of the video signal before commencing comparisons involving n+p (where p is the number of lines encompassed by a block).

XXXXXX (applied 26 February 1988)
VARIABLE LENGTH DECODING
BT
- A VLC decoder configuration.

XXXXXX (filed 10/6/86)
DIGITAL FILTER FOR VIDEO APPLICATIONS
PKI

XXXXXX (filed 6/6/87)
A METHOD FOR MOTION ESTIMATION IN A MOTION COMPENSATED HYBRID CODER
PKI

XXXXXX (filed 27/3/87)
CONTROL OF THE QUANTIZER IN A HYBRID CODER BY THE CODER STATUS
PKI

DE 36 44 407 (24.12.86)
G. Kummerfeldt, W. Schwerzel
AEG
- A process for displacement vector search by a programmable array of processor elements

DE 33 28 341 (05.08.83)
F. May, W. Wolf
AEG
- A process of frame to frame prediction coding in which the motion compensated estimated picture is computed in a hierarchical manner.

85 15 649 (October 85)
SCANNING CLASSES AND POST-DECISION TECHNIQUE
CNET

88 12 186 (September 88)
VARIABLE THRESHOLDING TECHNIQUE
CNET

US 4,971,598 (Dec. 13, 1989)
TWO-DIMENSIONAL DISCRETE COSINE TRANSFORM PROCESSOR
M.L. Liou, M.T. Sun, L.Wu
BELLCORE

The 2-D processor consists of a 1-D DCT processor, a transposition memory and another 1-D DCT processor. The 1-D DCT processor simultaneously computes an entire row or column of vector inner products by using distributed arithmetic and using decimation-in-frequency to reduce the amount of memory capacity (ROM) required. Partial sums may also be used to further reduce ROM size.

Bellcore Patent Application No.258)
CIRCUIT IMPLEMENTATION OF BLOCK MATCHING ALGORITHM
K.M. Yang, L. Wu
BELLCORE

The invention relates to a VLSI implementation of a block matching algorithm with full search capability for detecting and compensating differences between successive video frames caused by motion.

Application Number 138,846 (September 28, 1987)
METHOD AND APPARATUS FOR DETECTING THE MOST POWERFULLY CHANGED PICTURE AREAS IN A LIVE VIDEO SIGNAL
VISTACOM

XXXXXXXX (13 December 1988)
BIAS CANCELLING DCT CODEC
BT

A predictive decoder, eg a hybrid DCT interframe predictive decoder, reduces the tendency of long-term bias error in the decoded difference signal to accumulate in the predictor by periodically alternating the polarity of the bias error relative to the contents of the predictor. The inverse discrete cosine transform (IDCT) stage in the receiver is bracketed by switchable invertors which, when operating, invert the signal into the IDCT stage and then re-invert the signal, plus error, out of the IDCT stage, thereby inverting the error relative to the difference signal. Control means eg a

pseudo-random number generator, switches the invertors in and out periodically such that over several frames each block spends an equal amount of time in 'normal' and 'inverted' mode.

END