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TITLE : IDCT MISMATCH FOUND IN FLEXIBLE HARDWARE EXPERIMENTS

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1. INTRODUCTION

Recent Flexible Hardware experiments in Japan as well as between UK and Japan have revealed that IDCT mismatch occurs even when both IDCTs meet the CCITT specification. This mismatch is mostly observed as blocks, particularly if the stepsize is fixed at 8. The mechanism is now clearly understood and a smart solution is requested.

2. MECHANISM

Assuming that only one IDCT input component $F(u_o,v_o)$ is non-zero, the IDCT output $f(x,y)$ is given as follows according to the definition in §1.2.4 of the Flexible Hardware specification;

$$f(x,y) = 1/4\ B(u,x)\ B(v,y)\ F(u_o,v_o)$$

where $B(w,z) = C(w) \cos[\pi w(2z+1)/16]$
$C(w) = 1/\mathrm{sqrt}(2)$ for $w=0$, 1 otherwise

The product $B(u,x)\ B(v,y)$ becomes rational numbers +/- 1/2 when $u,v = 0$ or 4. In this case the IDCT output is given as follows;

$$f(x,y) = 1/8\ F(u_o,v_o)$$

If $F(u_o,v_o)$ is equal to $(8m + 4)$ where m is an integer, then the IDCT output is $(m + 1/2)$. This exact value of 1/2 is the problem. According to the internal intermediate computation such as two 1-dimensional transforms being cascaded, or scaling of transform coefficients, the output may be a little bit smaller or greater than the exact value of $(m + 0.5)$, giving rounded number m or m+1. When the IDCT output gives exactly $(m + 1/2)$, then how to round this to the 9 bit becomes another problem. See Appendix for two specific examples of IDCT implementation.

A particular example is for stepsize = 8. If only dc component is +12 or -12, the first representative values of the quantizer, and all other components are zero at the IDCT input, then the IDCT output may vary as follows according to the design;

	IDCT input	IDCT output
a)	+12/-12	+2/-1
b)	+12/-12	+2/-2
c)	+12/-12	+1/-1
d)	+12/-12	+1/-2

The mismatch was found out in the experiment between the schemes a) and b). Noticeable mismatch blocks are mostly due to the (0,0) component. Other

possibilities for the mismatch are stepsizes 24, 40, 56. At least 24 was also found problematic in an experiment.

Second order combinations such as (0,0) and (4,0) components may cause the same problem for (8m + 2) or (8m + 6) representative values, and this happens for stepsizes 4 or 12.

3. REQUEST FOR SOLUTION

Members are requested to find a solution for coping with the above problem. Immediate thoughts may be to shift those problematic representative values by one, or to drop the stepsizes 8/24/40/56.

Perhaps we have to consider the following (may be conflicting?) requirements:

- It should allow simple quantization process at the coder.
- It should allow simple generation of the representative values.
- It should not necessitate quantizer look up tables.
- It should not degrade the coding performance.
- It should be verified that it does not cause another new problem.

4. CONCLUSION

An IDCT mismatch problem has been analyzed. The solution should been included in the final Recommendation.

END

Two examples of IDCT implementation

$$f(x,y) = \frac{1}{4}\sum_{u=0}^{7}\sum_{v=0}^{7} C(u)C(v)F(u,v)\cos\left[\frac{\pi u(2x+1)}{16}\right]\cos\left[\frac{\pi v(2y+1)}{16}\right] \quad ①$$

$$= \frac{1}{8}\sum_{u=0}^{7}\sum_{v=0}^{7} F(u,v)\cdot \underbrace{\left\{\sqrt{2}\,C(u)\cos\left[\frac{mu(2x+1)}{16}\right]\right\}}_{B_1(u,x)}\underbrace{\left\{\sqrt{2}\,C(v)\cos\left[\frac{mv(2y+1)}{16}\right]\right\}}_{B_1(v,y)} \quad ②$$

$$= \sum_{u=0}^{7}\sum_{v=0}^{7} F(u,v) \underbrace{\left\{\frac{1}{2}C(u)\cos\left[\frac{mu(2x+1)}{16}\right]\right\}}_{B_2(u,x)}\underbrace{\left\{\frac{1}{2}C(v)\cos\left[\frac{mv(2y+1)}{16}\right]\right\}}_{B_2(v,y)} \quad ③$$

$$B_1(0,0) = 1$$

$$B_2(0,0) = \frac{1}{2\sqrt{2}} = 0.353553390594\cdots \quad (d)$$

$$\simeq \frac{16A1\ (h)}{4000\ (h)} = 0.353576660156 \quad (d)$$

② INMOS chip $B_1(0,0)^2 \times 12 \div 8 = 1.5$

③ 384 FH specification $B_2(0,0)^2 \times 12 = 1.500197457\cdots$

IDCT Input	IDCT output	
	INMOS chip	384 FH
+12	+2	+2
-12	-1	-2