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Title : Error correction by parallel decoder with switching function
(cf. Section 3.7.2 of Annex 4 to Doc.#540R)

1. Introduction

In this document, the parallel decoder with switching function which selects a random error decoder or a burst error decoder based on the characteristics of the transmission lines is described. This document also describes the comparison of the error correction capabilities for code C1 and code C17 (see Annex) using this parallel decoder.

2. Parallel decoder with switching function

The Block diagram of the parallel decoder with switching function is shown in Figure 1. In this parallel decoder, a random error decoder(RED) or a burst error decoder(BED) is selected by a controller. For example, when a probability of the uncorrectable error detection by RED increases, the controller selects BED.

This parallel decoder has following advantages:

i) Only one decoder is always operated so that the low power operation is possible.
ii) Number of uncorrected error is lower than the previous parallel decoder without switching function (Fig. 1 of doc.#507).

We compared the performance of this parallel decoder with switching function between code C1 and code C17 as follows:

2.1 Comparison of the random error correction capability

For the random errors, those two codes have the same capability.

2.2 Comparison of the burst error correction capability

The burst error correction capability of (511, 493) BCH code is specified with the Riger bound and the maximum length of the correctable burst errors is 9 bits or less. The correction capability of burst error which length is 6 bits or less is same between code C1 and code C17. But, for the burst errors which length is 7, 8 or 9 bits, code C1 has more powerful error detection capability than code C17. The comparison between code C1 and code C17 is shown in Table 1.

Table 1 Comparison of burst error correction capability between code C1 and code C17

burst error (7~9 bits)	code C1	code C17
error detection	107,303 (95.13 %)	106,311 (94.25%)
miscorrected error	5,497 (4.87 %)	6,489 (5.75 %)

3. Performance for composite errors

Using the previous parallel decoder without switching function, the comparison of correction capability for composite errors, i.e. random and burst errors, between code C1 and code C17 is shown in Table 2. In this case, code C17 excels code C1.

Table 2 Comparison of composite error detection capability between code C1 and code C17

composite error	code C1	code C17
corrected error	135,988 (94.72 %)	138,419 (96.13%)
miscorrected error	7,600 (5.28 %)	5,569 (3.87 %)

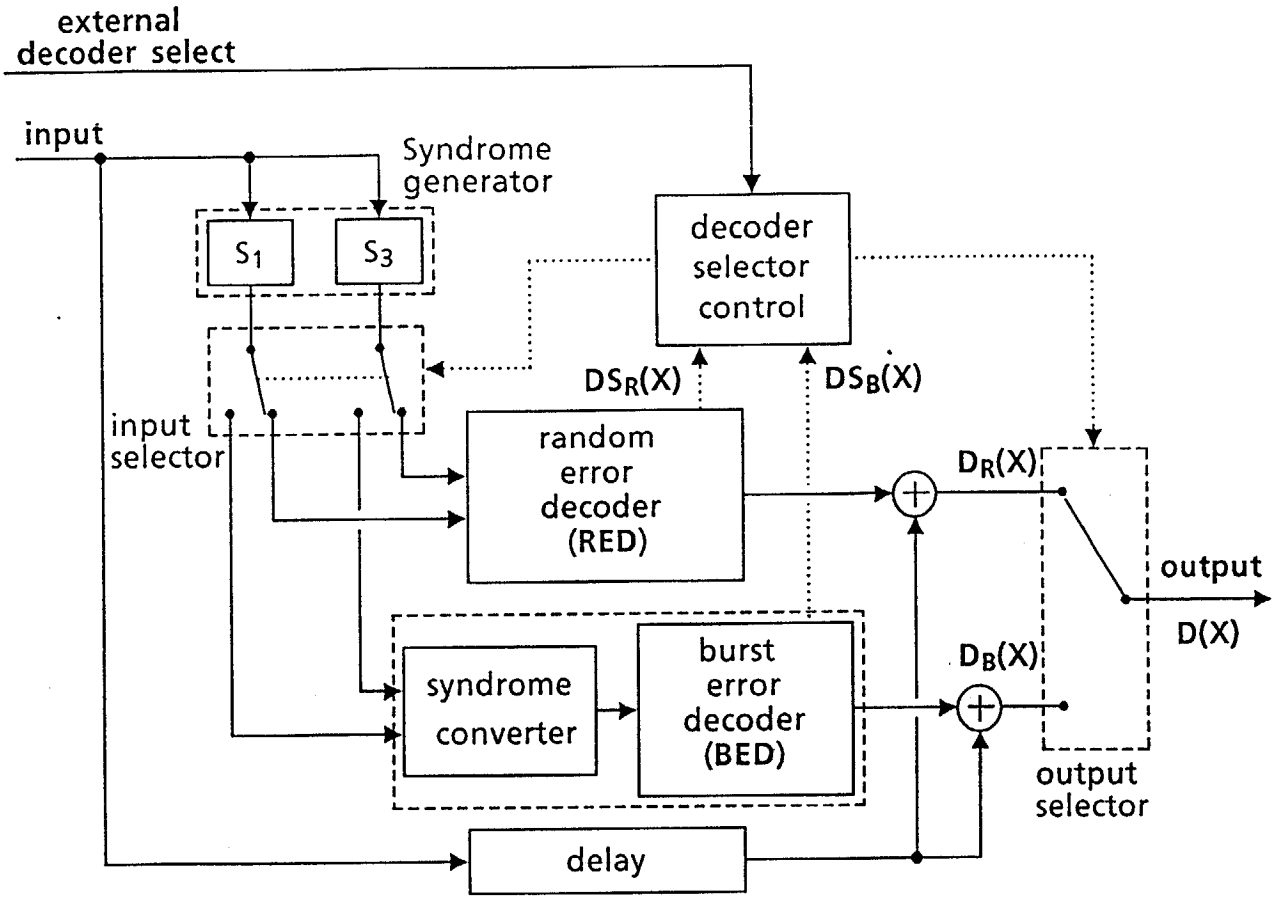
4. Hardware implementation

In the syndrome generator and the other circuits of decoder, the number of EXOR gates for code C17 is more than twice for code C1. Therefore the delay time on generating the syndromes with code C17 is longer than code C1. And when a fast algorithm is applied, hardware size for code C17 is significantly large.

5. Conclusion

Parallel decoder with switching function which we described in this document has more powerful performance for both error corrections and operates lower power than previous parallel decoder without switching function. For this new parallel decoder, code C1 is superior to code C17 about the burst error correction capability and hardware size of the decoder. Therefore code C1 should be used as before.

END.



$D_R(X)$ decoded signal by random decoder
$D_B(X)$ decoded signal by burst decoder
$DS_R(X)$ uncorrectable error detection by random decoder
$DS_B(X)$ uncorrectable error detection by burst decoder

Figure 1. Block diagram of the parallel decoder with switching function

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Code C1 use the following generator polynominal :

$$g_1(x) = (x^9 + x^4 + 1)\,(x^9 + x^6 + x^4 + x^3 + 1)$$

Code C17 use the following generator polynominal :

$$g_{17}(x) = (x^9 + x^7 + x^6 + x^4 + x^3 + x + 1)\,(x^9 + x^8 + x^7 + x^6 + x^4 + x^2 + 1)$$