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Specialists Group on Coding for Visual Telephony

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Title: Error correction framing lock-up time

1. Introduction

This document proposes a maximum error correction framing lock-up time under switched multipoint configuration, which Document #519 has pointed out to specify.

2. Background

Typical switched multipoint configuration is shown in Appendix 1. According to a request, a switching sequence takes place. First, MCU sends a FPR (Freeze Picture Request) signal to the decoder. Then MCU switches its input bit stream from COD1 to COD2, and the decoder starts re-lock operation to establish the error correction framing synchronization. Next the MCU sends a FUR (Fast Update Request) signal to COD2 to make it encode the next video frame with intraframe mode. The coded bit stream is transmitted to the decoder with PFR (Picture Freeze Release) bit ON.

To prevent the decoder from missing the intraframe coded data, it needs to complete the re-lock operation before the data arrive. This can be realized by defining the maximum re-lock time and by delaying the transmission of FUR signal for a certain time. This document proposes the maximum re-lock time, considering:

1) estimated worst case lock-up time,
2) flexibility of hardware design,
3) man-machine interface, and
4) system design.

3.1 Estimation of lock-up time

An estimation of the lock-up time has been carried out assuming:

- all 8 bits are used in pattern matching, and
- re-synchronization is established after consecutive m-time synchronization detections.

The worst case is that a detection starts after the first bit of the frame pattern. It reads 4096 * m + 3584 bits before the establishment. In case of m=3, 15,872 bits are necessary and this corresponds to 0.34 second when the video transmission rate is 46.4 kb/s (see Appendix 2).

3.2 Flexibility of hardware design

Taking following two points into account, two or three times of the estimated value, namely 0.68 to 1.02 seconds, had better be allowed.

- leave flexibility on the hardware architecture mainly to make it possible to design a compact codec, and

- processing delay is not included in the estimation.

3.3 Man-machine interface

From the viewpoint of man-machine interface, it is generally said that the maximum response time allowed is about 3 seconds. In case of multipoint switching, the total time from the decision of switching, or from the arrival time of a certain signal that shows the request of switching, to the appearance of a picture from the new encoder should satisfy this time limit.

The time before the switched bit stream reaches to the decoder will be negligible, since the transmission time of FPR signal may be on the order of several 10 ms, or several sub-multiframe time, and the switching time from COD1 to COD2 may not depend on the transmission rate but on the device speed. Therefore the bottleneck consists in re-lock time, transmission time of intraframe coded picture, and decoding time.

As for the decoding time, it will be less than 134ms since each codec is expected to have ability to decode at least 7.5 frames per second. And it turns out to be negligible.

As a result, almost whole the 3 seconds can be shared by the re-lock time and the transmission time.

3.4 System design

From the viewpoints of system design margin, it seems desirable to reduce the total of re-lock and transmission time to 2 or 2.5 seconds. The remaining problem is how to divide this time between re-lock and transmission. The transmission time exactly corresponds to the amount of information. Therefore allowing a long transmission time is better since it will show a fine picture. But a longer transmission time imposes a heavier load on the re-lock time.

When the total time is divided evenly to the re-lock and transmission time, from 1 to 1.25 seconds are allocated to the transmission time. In case of 7.5 Hz coding, this period corresponds to 7.5 to 9 times of average transmission time of each video frame. In this sense, 1 to 1.25 seconds of transmission time seems sufficient. And it leaves 1 to 1.25 seconds for the re-lock time.

3.5 Conclusion

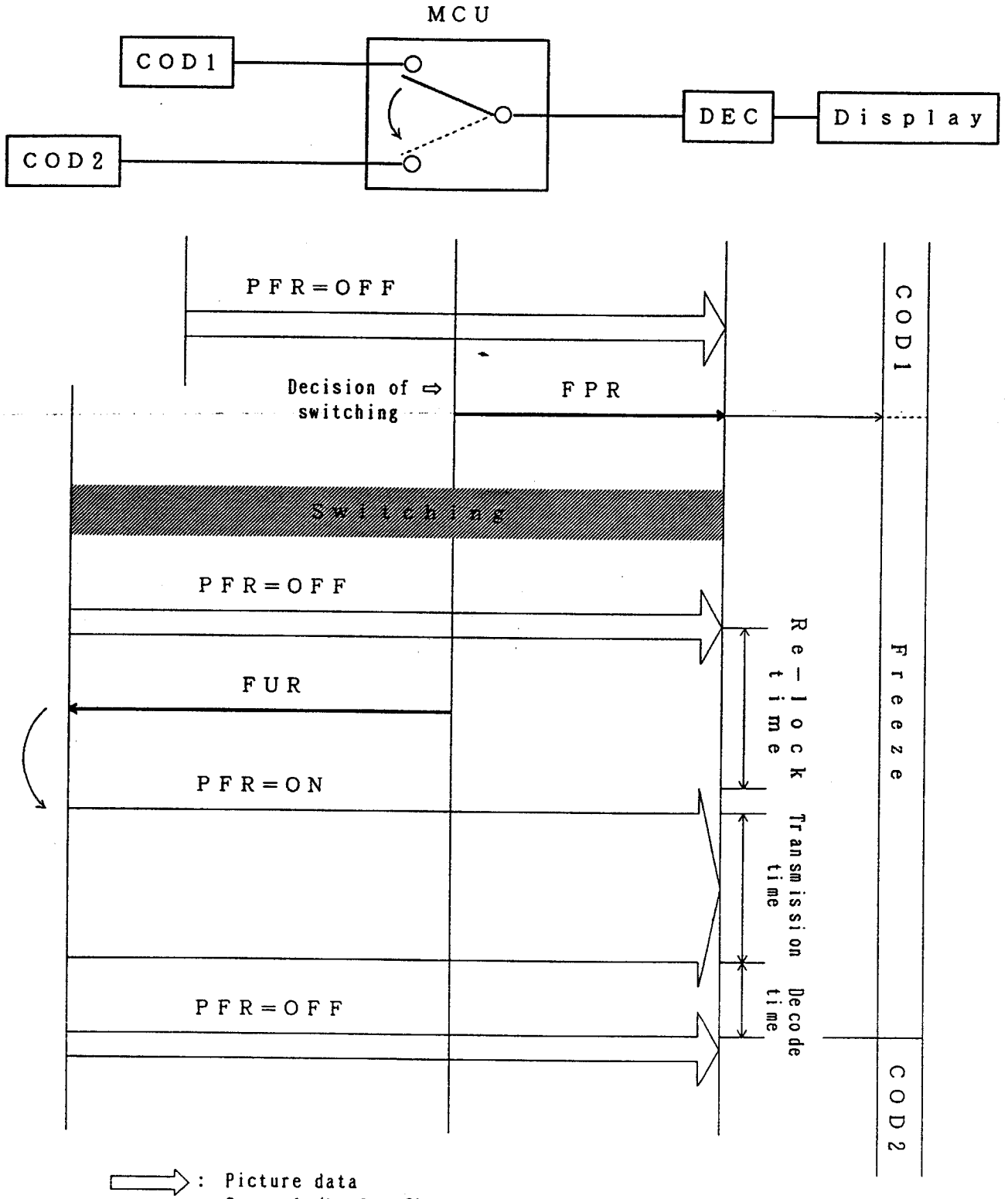
From the hardware consideration, about 0.7 to 1 second is required. While the system margin consideration allows about 1 to 1.25 seconds. Taking both considerations into account, the re-lock time of 1 second seems reasonable.

4. Proposal

Re-lock time of error correction framing has been studied under switched multipoint configuration. Based on the discussion above, we propose 1 second as the maximum re-lock time.

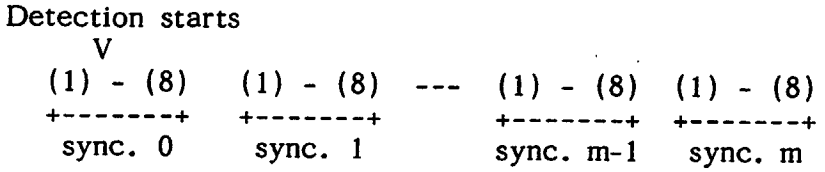
Appendix 1 to Document #556

Multipoint configuration and switching sequence



Estimation of lock-up time

A result of estimation of error correction framing lock-up time is shown. Eight framing bits are designated by (1) - (8). Synchronization will be established after consecutive m-time synchronization detections.



The worst case is that the detection starts just after bit (1) of synchronized frame 0. This case needs following number of bits before synchronization establishment.

$512 * 7 + 512 * 8 * m = 4096\ m + 3584$ bits.

In case of m=3, total bits are 15872 and corresponding times are:

Video rate	Time
46.4 kb/s	0.34 s
62.4	0.26
312.0	0.05