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Specialists Group on Coding
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Title: **RE-LOCK TIME FOR THE ERROR CORRECTION FRAMING**

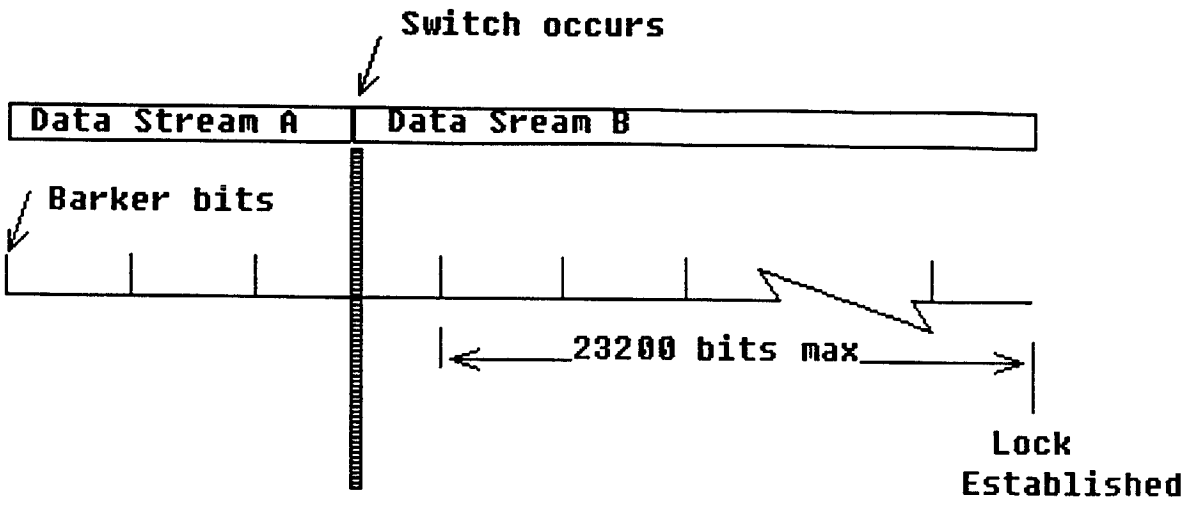
Source: N, S, UK, F, FRG, NL, I

The error correction frame re-lock time needs to be specified in H.261 to ensure that all decoder designs can be made compatible with a future multipoint control unit specification. During multipoint operation video data streams are switched between encoder sources. The time taken for a decoder to settle once a switch has taken place (the re-lock time) needs to known so that Picture Freeze Release Signals are not lost. For example, if after a multipoint switch has taken place a decoder has not established error correction frame synchronisation then the video demultiplex process cannot track the data and any Freeze Picture Release header transmitted in bit 3 of type 1 will be missed. This will mean that the fast update picture will be lost and the picture will recover using systematic intra-coded blocks only. If we know the maximum time taken for a decoder to settle after a switch then we can ensure that the Picture Freeze Release signal arrives at a time when the video demultiplex is correctly in track.

Simply specifying the period taken to lock to a new error correction framing sequence is probably insufficient. This is because there is a probability that the video data itself will contain emulations of the error correction framing sequence. A simple deframing circuit might examine only a single Barker sequence and thus be able to quickly lock to the error correction framing under certain video data conditions. There is however a very high probability that such a circuit would lock erroneously to the 8 bit Barker sequence emulated by the video data.

To overcome this problem the specification should also include the number of consecutive error free barker sequences to be found before lock is said to have taken place. It can be shown by statistical calculations that if we state 3 Barker sequences must be found consecutively before lock occurs, the probability of erroneously locking to random data is acceptably low.

We therefore propose that the specification should state that decoders should be designed so that 3 consecutive error correction frame Barker sequences should be received before frame lock is said to be achieved and the design should be such that frame lock will always be re-established within 23200 bits are a change of error correction framing phase (see diagram below). The specification would have to contain a note to say that this assumes that 3 correctly phased erroneous Barker sequences generated by video data do not occur within the error correction frame locking period. 23200 bits has been chosen so that lock will be achieved within 0.5 second when the video bit rate is 46.4kbit/s.



In addition, we also propose that the Barker sequence should be specified as a fixed pattern of 8 bits. Currently, the sequence is specified as a fixed pattern of 7 bits with a 1 bit don't care. The don't care bit is usually used for establishing a multiframe sequence to allow additional layers of signalling in the framing. In the case of error correction framing this is not required and the existence of a don't care state merely increases the chances that a framing circuit will erroneously lock to framing patterns generated by the video data itself. If we set this don't care bit to 1 then erroneous locking will occur 8 times less frequently. This is because we have to detect 3 consecutive error correction frame Barker sequences before establishing lock and the number of bits used for framing will be increased from 21 bits to 24 bits.