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Specialists Group on Coding
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Title: **ERROR CORRECTION CONFORMANCE**

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The H.261 specification uses a double error correcting BCH (511, 493) error correcting code. The generator polynomial for the error corrector is also specified. These statements clearly specify the mathematical process involved for the error correction system. Unfortunately, when implementing such a scheme it is possible to interpret the mathematics correctly and still end up with an incompatible error correction scheme. This is because the way that the mathematics in the error correction scheme are applied is a matter of convention rather than definitive specifications. This means that it is possible for a manufacturer to apparently meet the specification with inverted parity bits because of a misunderstanding about unwritten conventions. We would therefore like to propose that a statement is added to the specification which defines the exact error correction parity bit pattern for a specific data input.

A suitable pattern results when the fillbit is set to 0 in a error correction frame. The error correction data then becomes 0 followed by 492 bits set to 1. The resulting error correction data (according to BTRL simulations) will be:

011011010100011011