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Specialists Group on
Coding for Visual Telephony

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Title: ERROR CORRECTION FRAMING LOCK-UP TIME - MULTIPOINT CONSIDERATIONS

Source: UK, France, FRG, Italy, Netherlands, Norway, Sweden

At the last CCITT SGXV/1 meeting the Japanese proposal for error correction framing was agreed. The framing consists of one bit every 512 bits and the framing pattern is repeated every 4096 bits. The framing for the error corrector is "in-band" as far as the video signal is concerned. During multipoint switching this framing pattern will be interrupted as the MCU switches from one source to another source. The time taken for a decoder to lock to the new frame alignment signal after a multipoint switch is therefore important.

There are two techniques which can be used for detecting framing structures. The first is a hardware implementation comprising of several serial delays and a look-up table which examines the complete framing pattern. The second method uses a state machine technique. Each bit is examined in sequence to determine if a framing structure is present. Both schemes are practical if we assume that the framing structure rarely gets interrupted and that lock-up time after framing loss is unimportant.

In our application, lock-up time is very important and therefore schemes based on bit sequences should not be used.

Proposal

Include a nominal maximum frame structure lock-up time in the final specification.