CCITT SGXV
Working Party XV/1
Specialists Group on Coding for Visual Telephony

Document #499R
March 10, 1989

SOURCE: CHAIRMAN
TITLE : REPORT OF THE FIFTEENTH MEETING IN OSLO (March 7 - 10, 1989)

CONTENTS

1. GENERAL

The Specialists Group met in Oslo, Norway, from March 7 to 10, 1989 at the kind invitation of Norwegian Telecommunications Administration. Welcoming address was delivered by Mr. Fjøsne on behalf of the hosting organization.

The list of participants appears at the end of this report.

Mr. Nicol announced through VTR that Mr. Morrison replaces him as Core Member of UK.

At the closing session, Chairman thanked the hosting organization for the meeting facilities provided and the excellent operation of the meeting.

2. DOCUMENTS FOR THE MEETING (TD 2)

For this meeting, 54 normal documents and 14 temporary documents have been available. Annex 1 shows the outline of each document.

3. TAPE DEMONSTRATIONS (TD 3)

A number of tape demonstrations as listed in Annex 2 were presented during the meeting.

4. REFERENCE MODEL AND ALGORITHM STUDY

4.1 Reference Model 7 (#446, #454, #455, #471, #479, #482, #489)

According to Document #446 which provides a complete description of RM7, various participating organizations implemented the Reference Model. Obtained performance in terms of reproduced picture and statistics showed similarity, indicating that understanding is common. Some discrepancy in statistics, number of bits for macroblock attributes and EOBs in particular, was worked out among concerned members.

4.2 Buffer Regulation (#455, #458, #471, #480)

RM7 was found to give bad buffer regulation, particularly at QCIF operation, due to the increased GOB size. The meeting agreed to adopt quantizer change at every 11 macroblocks for future simulation works. How to count the number of bit for signalling the quantizer step size was dealt with in the discussion of RM8.

4.3 RM8 and Action Plans (#486, #490)

Mr. Haskell suggested the study on the following two ideas for improving the coding algorithm;

- Use of tug-bit to indicate the regions of interest requiring special treatment in coding, post-processing, etc.

- Use of conditional motion compensated interpolation which transmits interpolation errors.

Mr. Guichard undertook to coordinate a small group meeting which discussed revision of Reference Model according to the study results made available at this meeting and identified action points for further simulation works by use of the Reference Model 8. The outcome is in Annex 3.

5. SOURCE CODING

5.1 Maximum Coded Picture Rate (#456)

Mr. Takizawa pointed out that if the decoder processing capability concerning the temporal aspect of the source format is defined taking into account the features of DSP-oriented architecture, it will contribute to allowing simpler hardware with increased temporal resolution on an average. One example of such specification is illustrated in Doc. #456.

After some exchange of opinions on this idea, expressing support to this idea or worry about specification too much dependent on implementation, the meeting concluded that this matter should be studied further toward finalizing the draft Recommendation, leaving the Flexible Hardware specification as it is.

5.2 Motion Compensation (#453, #458)

Whether to allow 8x8 MC was discussed.

The two experimental results from Europe and Japan were first reviewed with respect to methods of 8x8 MC use, SNR figures and reproduced pictures. It was found that these two works were showing similar results with similar methods.

Next, the following opinions were expressed on whether 8x8 MC is required for the px64 kbit/s Flexible Hardware;

- Since there is no supporting evidence, a simpler solution should be chosen without stressing every decoder to have 8x8 MC capability in source decoder and video demultiplex. If hardware can prove its effectiveness, the final Recommendation may include it. (Mr. Hatori).

- Since it has already been agreed that the decoder should accept one vector for each 8x8 luminance or chrominance block, some means to utilize it should be defined. (Mr. Carr).

- Flexible Hardware should include this capability. If it will be proved useless, then it may be dropped in the final Recommendation. (Mr. Bruder).

After some discussion, the meeting concluded to drop the use of 8x8 MC in the Flexible Hardware specification in favour of simpler specification. Volunteers are encouraged, however, to test this 8x8 MC feature in their hardware so that we may not lose the way to future improvements.

5.3 Loop Filter (#459, #472, #475)

Based on the presented study results, the meeting agreed on the following loop filter specification;

a. Position: after the frame memory.
b. Characteristics: simplified 121 as in Fig. 1(b)/Doc. #472.
c. Signalling method for filter on/off: TYPE3 with DMV field as described in Item 2) of § 1/Doc. #459.

During discussion, Mr. Ericsson raised that the capability to switch off the loop filter even in motion compensated blocks may be necessary to avoid resolution reduction for panning scenes. There were also some opinions on the possible use of TYPE2, danger of IDCT mismatch increase, etc. The conclusion is, however, unchanged.

5.4 Adaptive Quantization (#460, #486)

Mr. Asai presented an experimental result on adaptive quantization using MC attribute. According to his experiences, Mr. Plompen suggested that drawing conclusion on a single test sequence is dangerous and that assigning smaller distortions to some regions means assigning larger distortions to other regions, thus trade-off should be well considered.

5.5 IDCT (#496)

The meeting agreed to modify the number '128' into '132' in the forced updating specification (§ 1.4/Annex 3 to Doc. #445R) to allow updating three macroblocks per coded picture.

6. VIDEO MULTIPLEX CODING

6.1 Picture and GOB Headers (#484)

Mr. Brusewitz raised the need to study possible reductions of the Picture and GOB header overhead bits and presented some results on the search of emulation of GOB Start Code by error free video data. Mr. Koga stated that hardware design can be eased if PSC and GBSC start codes are guaranteed free of emulation, for which Mr. Carr stated there is some way to cope with possible emulations by carefully using the knowledge of Picture and GOB Headers etc.

As a conclusion, members are encouraged to study further on these two topics.

6.2 Macroblock Layer

6.2.1 MBA (#449, #462)

How to use the combination of relative and absolute addressings agreed previously was reviewed. Since the maximum value of the macroblock address is greatly reduced in the current macroblock structure, effectiveness of the absolute addressing for the tail part of the VLC set is reduced. The meeting agreed to adopt only the relative addressing. Codewords in Table 1/Doc. #449 was also agreed.

6.2.2 TYPE3 (#449, § 2.2.3/#467, #497)

The meeting agreed on use of the seven macroblock types consisting of such attributes as prediction, motion vector, coded/not-coded, and quantizer update. There were some discussions on that the code table in Doc. #449 does not correspond to the RM7 statistics because the table is based on the 384 kbit/s data. Setting a guideline that we should use the code table optimized for lower bit rates, the meeting left the code word assignment to the small group meeting Mr. Morrison chaired. Giving a nickname for each type was also left to the group.

Mr. Helkiö suggested the quantizer change of every 11 macroblocks without using TYPE3 having the quantizer change attribute, on the grounds that more efficient TYPE3 coding is required. This idea was not accepted by other members because of its rigid restriction on the coding control.

6.2.3 MVD (#449, #459, #462, § 2.2.3/#467)

First it was agreed to send zero differential motion vectors as data, not as part of TYPE3. Next the arithmetic wrap for motion vector data, such as used in the nx384 kbit/s Flexible Hardware, was adopted. Finally the code set in Table 3/Doc. #449 was adopted.

6.2.4 CBP (#449, #461, #481)

Independent works by Japan and Europe showed corresponding results on the coding performance of the method to use 63 coded block patterns (variable length coded) and the "start of block" trick. The meeting agreed to adopt this method for addressing the coded blocks in a macroblock. The code set in Table 4/Doc. #449 was adopted.

During the discussion, it was pointed out that current transmission order of Y, C_R, C_B does not conform to CCIR Rec. 601. The updated Flexible Hardware specification is made aligned with CCIR Rec. 601.

6.3 INTRA Mode (#457, #478)

Mr. Takizawa and Mr. Speidel presented their works addressed to the transmission elements of INTRA mode with proposals different in various features; the number of transmitted DC values, their accuracy, how to handle the first AC value, use of INTRA-NOT-CODED mode, and TYPE2 indication.

After some exchange of views, the meeting requested Mr. Brusewitz to coordinate a small group to sort out the problems and find solutions. The outcome is as follows;

A small group with participants from Europe, Japan and North America met in order to define the INTRA mode. Taking picture quality, hardware complexity and specification simplicity into consideration, the small group came to the following conclusion.

1) CBP is not used (all sub-blocks are always coded).
2) TYPE2 layer is skipped (only TYPE3 is used).
3) Six DC values, each with 8 bits are transmitted for each macro-block.
4) 'INTRA-NOT-CODED' mode is not used.

a)

MBA	TYPE3	TCOEFF
vlc	4 bits	vlc

b)

MBA	TYPE3	QUANT2	TCOEFF
vlc	7 bits	5 bits	vlc

Note: 4/7 bits for TYPE3 is an example from #449.

TCOEFF

DC_{Y1}	AC	EOB	. . . .	DC_{Y4}	AC	EOB
8 bits	vlc	2 bits		8 bits	vlc	2 bits

DC_{CB}	AC	EOB		DC_{CR}	AC	EOB
8 bits	vlc	2 bits		8 bits	vlc	2 bits

Note 1: The first AC-component in each sub-block corresponds to run length = 0.
Note 2: Exact bit patterns for DC values still remain to be defined.

<u>Observation</u>: Minimum number of bits for one INTRA macro-block is 65.

Note 3: 'DC' means the first DCT coefficient quantized uniformly (without dead zone) with step size = 8. 8 bits covers the whole dynamic range.
Note 4: "Start of block trick" is not used in INTRA mode.

6.4 Block Layer

6.4.1 CLASS (#463, § 2.2.4/#467)

Mr. Ohzeki presented his work on the adaptive scanning at higher bit rates, proposing the single zigzag scanning at the whole bit rate range and subsequent changes in the corresponding part of the Flexible Hardware;

removal of "CLASSIFICATION" in Fig. 3, Bit 3/TYPE2 becoming "Spare", removal of "CLASSIFICATION" from Block Header, modified description of TCOEFF.

This proposal was accepted.

6.4.2 TCOEFF (#449, #462)

The use of the "start of block code" trick was agreed, which utilizes the fact that the first event in each block can never be EOB. Mr. Koga suggested that possibility of PSC/GBSC emulation may be reduced if ESCAPE code word is changed and if some code words for fixed code length are forbidden. The code set in Table 5/Doc. #449 was adopted with the following modifications, which Mr. Brusewitz worked out;

ESCAPE	0010 00	→	0000 01
(R,L)=(0,6)	0000 0101 s	→	0010 0001 s
(R,L)=(11,1)	0000 0111 s	→	0010 0011 s
(R,L)=(12,1)	0000 0110 s	→	0010 0010 s
(R,L)=(13,1)	0000 0100 s	→	0010 0000 s
(R,L)=(X,0)	allowed	→	forbidden
(R,L)=(X, -128)	allowed	→	forbidden

6.5 VLCs

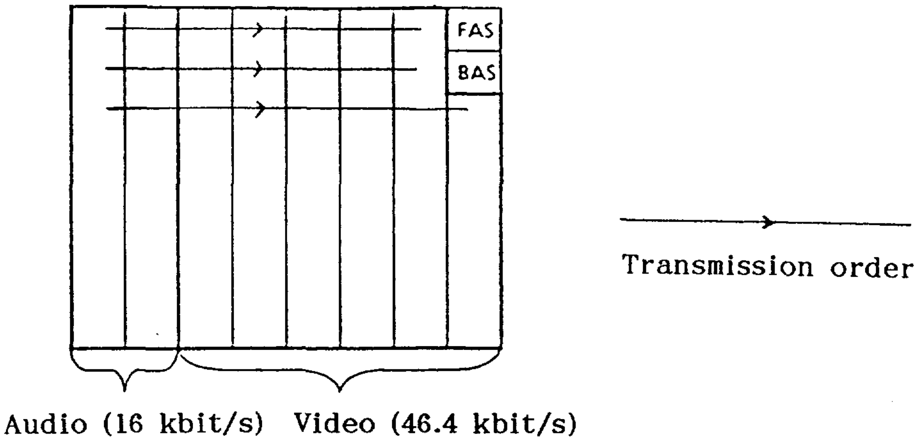
Chairman raised that the restriction of maximum number of bits for each VLC code set may be useful to ease the hardware design, so that possible changes of parameters based on the simulation or hardware optimization results can be incorporated later. Mr. Carr expressed his view that it is highly likely that these VLC sets may also be used in the final Recommendation with exceptions of removing mistakes, etc. Participating members shared this view. Mr. Haskell also pointed out that even they should be optimized, changes would happen only in short codes. The meeting expects these information may help the hardware designers.

7. TRANSMISSION CODING

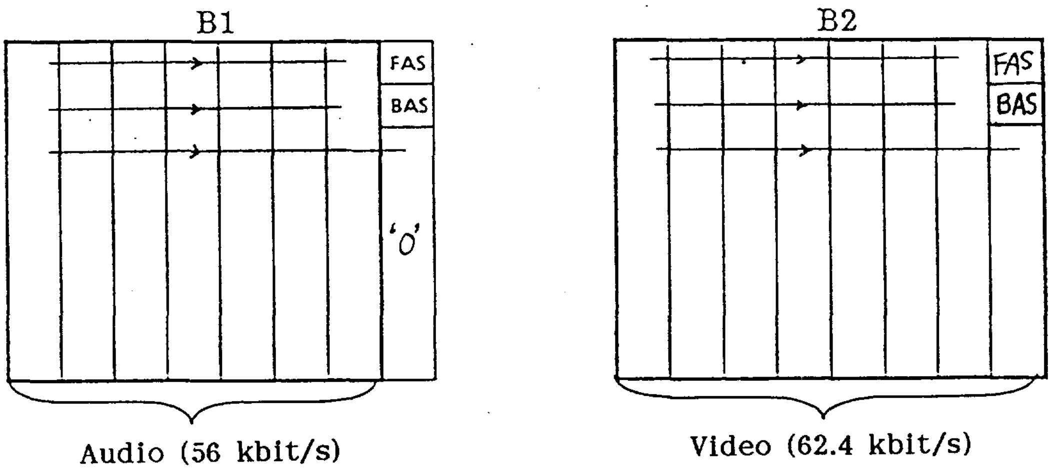
7.1 Bit Rates and its Allocations (#448, #465, #495; TD7)

Flexible Hardware trials are mainly targeted to verify video compatibility, but with the arrangement of the final form as far as possible. Taking into account this principle and the fact that the Working Party XV/1 is responsible for this matter, the meeting agreed that the attached illustrations, which Mr. Wada summarized, are applied for the bit rate arrangements in the H.221 frame structure. Necessity of BAS in the second B channel for p=2, and in the second to sixth B channels for p=6, was discussed to some extent, concluding the solution in the attached Figures 1(a) through (c) as default and subject to change according to the study results in the Working Party meeting held from March 14. Chairman will inform the members of the results as soon as they are made available.

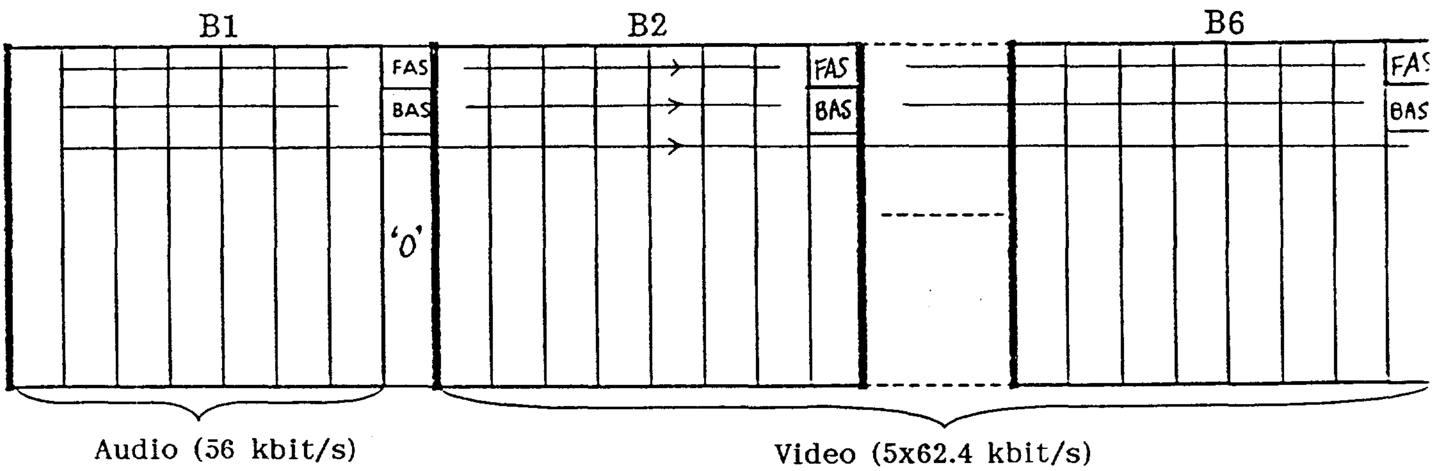
Chairman's Note: Results of the Working Party XV/1 meeting (March 14-17, 1989) indicated that it is likely in the final Recommendation that not only FAS but also BAS would be inserted in each 64 kbit/s channel (at least up to p=6). Therefore, the Flexible Hardware includes FAS and BAS in each 64 kbit/s channel. The attached Figures 1(b) and (c) have been modified accordingly.



(a) 1B case, p=1



(b) 2B case, p=2



(c) 6B case, p=6 (in I.431 frame)

Note 1: Octet timings of H.221 and ISDN may not be synchronized in the Flexible Hardware experiments.

Note 2: In the 6B case, positions of FAS in six B channels are aligned with each other.

Figure 1 Bit rate allocations in Flexible Hardware

FAS of H.221 framing may not be synchronized with the ISDN octet timing for the experimental purpose. It has been recognized, however, that they should be synchronized when intercommunication with audio terminals comes to life.

7.2 Clock Source (#452, § 3.1/#467)

The idea of using looped timing regardless of whether the network is synchronous or asynchronous was withdrawn in Doc. #452. Hence some description on the clock source switchable from free running to looped timing is required in the Flexible Hardware specification. Specific wording is dealt with by Mr. Morrison's small group.

Indication bit for the clock source switching according to the nature of the network, being synchronous or asynchronous, is now required somewhere in the H.221 framing. This point is put forward to the consideration of Working Party XV/1.

7.3 Data Buffer (#451, #485, § 3.2/#467)

1) Maximum number of bits per coded picture

The following values were agreed;

CIF 256 Kbits (K=1024), and
QCIF 64 Kbits.

2) Additional specification

It was recognized that there is a potential problem of some coder generating small number of bits per picture, packing them and sending them in a short period, then ending up with the buffer overflow in the decoder.

Some possibilities indicated in Doc. #485 and others were discussed. The members are requested of further study toward the final Recommendation so that different design codecs can be compatible.

3) Framing for the underflow prevention

According to the conclusion on the error correction code (see § 7.4), the framing proposal for the underflow prevention contained in § 3.2/#467 was accepted except whether framing bits be distributed as in the proposal or concentrated as in Doc. #432 (Florida). This matter was further discussed among concerned members, resulting in the conclusion to adopt the arrangement in § 3.2/Doc. #467.

7.4 Forward Error Correction (#464, #476, #487, #498)

First, related four papers were presented by Mr. Asai, Mr. Plompen, Mr. Ericsson and Mr. Carr. Next, some information was exchanged on the the content of each document, particularly on details of the three schemes proposed; (511, 493)BCH, (511, 484)BCH and (1024, 992)Reed-Solomon.

After some general discussions on requirements, performance and implementation of the three schemes, Mr. Speidel undertook to chair a small group to sort out the problems and to reach a conclusion. The outcome is as follows;

A group with members from Japan, North America, Korea and Europe met to decide upon an FEC scheme to be used in the Flexible Hardware. Documents under discussion were

Doc. #464 (Japan), Doc. #467 (Japan), Doc. #476 (Europe), Doc. #487 (USA) and Doc. #498 (UK).

Three different proposals were on the table

- Japan (511, 493) BCH code,
- UK (511, 484) BCH code,
- USA (1024, 992) Reed-Solomon code.

The UK proposal was supported by Europe. At the beginning participants shared the opinion that

- only one scheme should be adopted,
- a decision should be taken at this CCITT-meeting (Note).

Note: The Netherlands disagreed to have a decision at this meeting.

Discussion items have been

- channel errors (random and/or burst errors?),
- correcting performance of FEC (random, burst errors),
- delay,
- redundancy overhead,
- hardware and software complexity.

All delegates were of the opinion that an FEC should be able to correct random as well as burst errors. Japan stressed the point that at least random double errors should be correctable and was satisfied with a maximum burst length of 6 bits. USA put emphasis on a larger burst length of 9 bits. UK has designed their FEC mainly for burst errors with length up to 11 bits.

After discussion of the Japanese proposal it turned out that the solution can handle burst as well as double random errors. But the question whether the performance of double error correction is decreased by about 17% or not in this case is for further study. As the capability of correcting random double errors was considered as an important requirement by Japan and because the UK and the Japanese codes were of the same kind, UK withdrew their proposal after some discussion to give room for a further compromise.

USA pointed out the superior simultaneous burst and random error correcting capability of the RS code. This was generally agreed. An interleaving technique which would have increased the BCH performance in this respect was refused due to the increasing delay time.

An extensive discussion took place about the implementation complexity of RS versus BCH codes. Japan and Europe were of the opinion that the complexity of the RS code is significantly higher than of the BCH code and they considered this as an important point in view of the tight time schedule for implementing Flexible Hardware. These arguments were heavily opposed by the US delegate.

Finally the decision was made by Mr. Okubo as the chairman of the group to use the (511, 493) BCH code proposed by Japan.

7.5 Non-ISDN Applications (#450, #470)

Mr. Carr and Mr. Zingman raised the necessity to study on the applications of the px64 kbit/s Recommendation H.261 to the following networks;

- 56 kbit/s,
- p=6, 24 with one's density restriction.

It has also been recognized that the interworking between H0 channel and 6xB channels should be resolved.

For the Flexible Hardware experiments, we would use 2x64 kbit/s or 384kbit/s or primary rate clear channels. If there are problems in these arrangements, they would be solved on a bilateral basis between the participating organizations. As for interconnections between 56 kbit/s and 64 kbit/s, Septet format and the arrangement in Appendix can be considered as a possible solution.

Toward the final Recommendation and the time when H.261 codecs are in real use, these interworkings among different networks should be clarified. This point will be put forward to WPXV/1 together with handshaking for the 64 vs 56 kbit/s connection raised in Doc. #470.

At the same time, members are requested to seriously consider how to cope with these problems, including the zero byte replacement method proposed in Doc. #470.

7.6 Audio Coding (#448)

The 16 kbit/s audio coding sub-channels are ignored in the Flexible Hardware experiments.

7.7 System Aspects (#468, #469, #491, #495)

Communications among same or different type of audiovisual terminals require negotiations after the call is established. The following four papers were introduced for the consideration of the Specialists Group;

- Doc. #468: Audiovisual communication procedure (Mr. Wada),
- Doc. #469: Video telephone communication procedure (Mr. Okubo),
- Doc. #495: Intercommunication among Audio/Visual terminals (Mr. Tabatabai).

Though this topic is also under responsibility of WPXV/1, members are requested to investigate them toward the next meeting so that we can clarify at least the requirements for those "system aspects" Recommendations.

Mr. Guglielmo provided information on a H.221 LSI with Doc. #491.

8. FLEXIBLE HARDWARE

8.1 Test Signal Generator (#466, #492)

Mr. Wada presented some requirements to the test signal generator considering the interest of implementation at p=1, 2. Mr. Randall provided information on the current status of designing the Generator. After discussion, the followings were decided;

a. Output signals: Coded audio at one 64 kbit/s port, coded video at another 64 kbit/s port.
b. Interface: RS422/449.

Since the test signal generator should better be tested before the delivery, Mr. Speidel undertook to do this checking with his software based decoder by June. Mr. Randall announced his plan to distribute a document on the coded data for members' review when it completed.

8.2 Hardware Trials (#447, #473, #488)

Current status and plans were presented by Europe and USA. Japan presented a plan for interconnections with other countries.

8.3 Specification

Mr. Morrison undertook to chair a small group for elaborating the Flexible Hardware specification. Based on the current specification in Annex 3 to Doc. #445R, this small group revised the text by incorporating the contents agreed during this meeting and discussing the necessary details.

The outcome is in Annex 4.

9. INTELLECTUAL PROPERTY

9.1 Patent Information Disclosure Policy (#474)

Statements have been submitted by three organizations.

9.2 Relevant Patents (#483, #494)

CNET and Bellcore informed the Group of their 4 patents and 3 patents, respectively.

9.3 Patent Licensing Policy (#493; TD4)

Bellcore submitted a statement on their licensing policy concerning standards related patents.

Chairman reminded members of the CCITT "code of practice" and previous agreements on the course of actions in the Specialists Group.

Since the scope of the Recommendation H.261 is going to be extended, the following actions are requested of the participating organizations in the Specialists Group;

1) Organizations which have already submitted statements

Check the object of statement and clarify that it covers the patents relevant to CCITT Recommendations on the px64 kbit/s video codec by submitting a document to express so or by submitting a new statement.

2) Organizations which have not yet submitted statements

Submit such statements at the earliest occasion.

10. REPORT TO STUDY GROUP XV (TD5, TD6, TD14)

In addition to the two already submitted papers (TD5, TD6) covering the previous two meetings in Paris and Florida, the following two items are further reported to Study Group XV as outcome of this meeting;

- Preliminary draft revision of Rec. H.261,
- Particular points requiring the guidance of Study Group XV.

11. OTHERS (TD8)

In response to the request of MPEG, a call for pre-registration for "Standard for Coded Representation of Moving Picture for DSM (digital storage media)" has been distributed among participating members.

12. FUTURE PLAN AND MEETINGS

1) 16th meeting of the Specialists Group: June 13(Tue) - 16(Fri), 1989, in Stuttgart, hosted by SEL. Projected topics are;

   - Items to be solved before the final Recommendation,
   - Items to be tested through hardware trials,
   - Plans for international compatibility checks,
   - Parameter optimization,
   - System aspects,
   - Terms of reference for the editorial group,
   - Others.

2) Supply of the test signal generator: June 1989.
3) Initiate the international compatibility check: September 1989.
4) Parameter optimization: Sep - Oct, 1989.
5) Editorial group meeting for Rec. H.261: mid Oct 1989, at BTRL.
6) 17th meeting of the Specialists Group: Nov. 7(Tue) - 10(Fri), 1989, in Tokyo.
7) Working Party XV/1 meeting: Nov. 27 - Dec. 1, 1989.
8) Revise Rec. H.261 through Resolution No. 2: mid 1990.

END

LIST OF PARTICIPANTS
(Oslo; March 7 - 10, 1989)

Chairman	S. Okubo	- NTT, Japan

Core Members

F. R. of Germany	J. Speidel	- PKI
	G. Zedler	- FTZ
Canada	D. Lemay	- BNR
USA	A. Tabatabai	- BELLCORE
	B.G. Haskell	- AT&T Bell Laboratories
	N. Randall	- DIS (acting for R.A. Schaphorst)
France	G. Eude	- CNET
	J. Guichard	- CNET
Italy	M. Guglielmo	- CSELT (acting for L. Chariglione)
Japan	Y. Kato	- NTT
	M. Wada	- KDD
Korea	J-H. Jeong	- ETRI (acting for J-S. Lee)
Norway	G. Bjø ntegaard	- Norwegian Telecom
The Netherlands	R. Plompen	- PTT-RNL
United Kingdom	D. G. Morrison	- BTRL
	N.L. Shilston	- GPT Video Systems
Sweden	H. Brusewitz	- Swedish Telecom Admin.

Assisting Experts

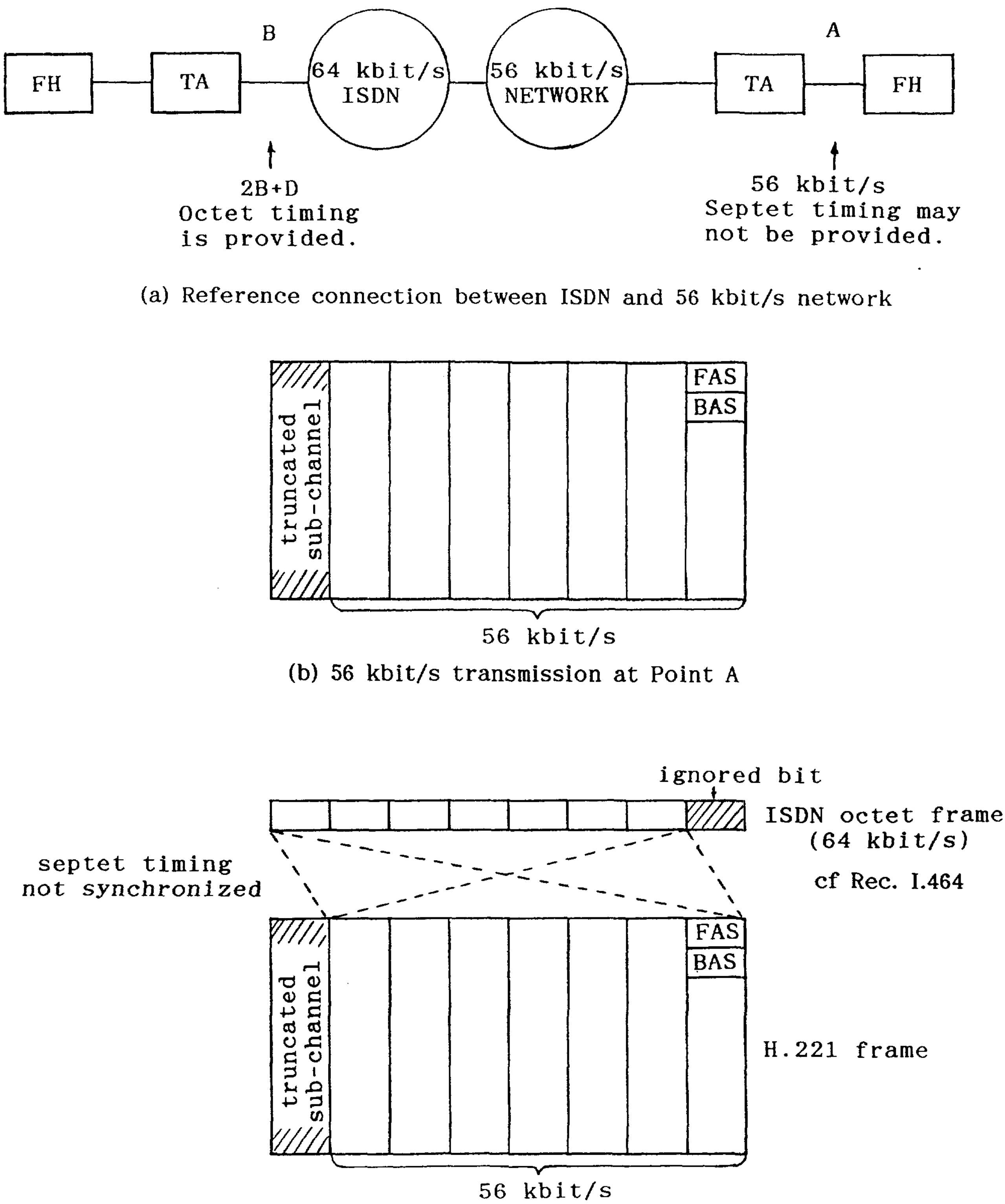
F. R. of Germany	W. Geuen	- SEL
	F. May	- AEG
USA	J. Bruder	- PictureTel
	S. Ericsson	- PictureTel
	D.N. Hein	- Video Telecom
	J. Zingman	- CLI
France	D. Devimeux	- SAT
Japan	K. Asai	- Mitsubishi Electric
	H. Fujiwara	- GCT
	Y. Hatori	- KDD
	T. Koga	- NEC
	K. Matsuda	- FUJITSU
	K. Ohzeki	- Toshiba
	M. Takizawa	- Hitachi
Norway	J. Bording	- Norwegian Telecom
	H. Sandgrind	- Norwegian Telecom
United Kingdom	M.D. Carr	- BTRL

Observer

Finland	R. Helkiö	- VISTACOM

Appendix to Doc. #495R

Relation between ISDN framing and H.221 framing
in the 64 to 56 kbit/s connection



(a) Reference connection between ISDN and 56 kbit/s network

(b) 56 kbit/s transmission at Point A

(c) 56 kbit/s reception at Point B

DOCUMENTS FOR THE OSLO MEETING

Normal Documents

#445R REPORT OF THE FOURTEENTH MEETING IN FLORIDA (CHAIRMAN)

Points agreed upon and/or left for further study in the previous meeting are recorded to provide backgrounds for discussions in this meeting.

#446 DESCRIPTION OF REF. MODEL 7 - RM7 (SPECIALISTS GROUP)

A complete description of RM7 is given.

#447 HARDWARE STATUS AND PLANS (AEG, BT, FRANCE, IMAGIN PROJECT, PKI)

The work in Europe aimed at providing hardware to verify the px64 kbit/s Recommendation is outlined, which is carried out by the source organizations.

#448 BIT RATES FOR FLEXIBLE HARDWARE EXPERIMENTS
(FRG, FRANCE, ITALY, NETHERLANDS, NORWAY, SWEDEN, UK)

Exact bit rates for hardware tests, and also for the final Recommendation as far as as possible, are proposed;

	Audio	FAS/BAS/C&I	Message Channel	Data	Video	
p=1	16*	4	0/4	0	44/40	*vacant for
p>1	56/48	$\underbrace{\hspace{6em}}_{8/16}$			(p-1)x62.4	FH tests

#449 VLCs FOR px64 kbit/s INITIAL COMPATIBILITY CHECK
(FRG, FRANCE, ITALY, NETHERLANDS, NORWAY, SWEDEN, UK)

VLCs representing MA, TYPE3, MVD, CBP and TCOEFF are proposed for the initial compatibility check, intending that these are sufficiently optimum to make a good start for the final optimization.

#450 H.261 - THE ONE'S DENSITY PROBLEM AND 'NON px64 kbit/s' USE
(FRANCE, FRG, GREECE, ITALY, NETHERLANDS, NORWAY, SWEDEN, UK)

Extension of the H.261 specification to non-ISDN type network use is raised, inviting discussion on such items as;

- interworking with networks having one's density restriction,
- nx56 kbit/s variant with minimal modification,
- interworking between H.261 codecs and nx56 kbit/s variants.

#451 BITS PER PICTURE SPECIFICATION
(FRANCE, FRG, GREECE, ITALY, NETHERLANDS, NORWAY, SWEDEN, UK)

Considering whole INTRA coded pictures and decoder hardware design, specification for the maximum number of bits created by a single coded picture is proposed as 256 Kbits for CIF and 64 Kbits for QCIF.

#452 CLOCK SYNCHRONISATION FOR THE H.261 px64 kbit/s CODEC
(FRANCE, FRG, GREECE, ITALY, NETHERLANDS, NORWAY, SWEDEN, UK)

After investigating the possible problems in the idea of adopting looped timing regardless of whether networks are synchronous or asynchronous, it is proposed to use some bits in the H.221 framing for indicating whether the codec is connected to a synchronous or asynchronous network.

#453 MOTION VECTORS FOR 8x8 BLOCKS IN RM7
(FRANCE, FRG, GREECE, ITALY, NETHERLANDS, NORWAY, SWEDEN, UK)

Based on the experimental results concerning improved buffer control (damping the rate of change of the quantizer step size) and use of 8x8 block based motion compensation, it is proposed that video multiplex structure should allow the optional application of 8x8 MC. It is also proposed that the signalling data should be hierarchical in nature, allowing encoders without 8x8 MC to efficiently signal only 16x16 motion vectors.

#454 RM7 SIMULATION RESULTS (JAPAN)

A typical example of RM7 implementation in Japan is presented for CIF at q=1.

#455 HIGHER BIT RATE OPERATION OF REFERENCE MODEL 7 (JAPAN)

Performance of RM7 at p=6, 12, 18, 24 are presented. Instability of buffer control is pointed out on on SWING at p=6. From the experiments with bit rates varied around 60 kbit/s, it is observed that 100 bit saving per coded picture corresponds to 0.03 - 0.06 dB improvement of SNR at 10Hz operation.

#456 MAXIMUM FRAME RATE SPECIFICATION ACCORDING WITH THE NUMBER OF SIGNIFICANT BLOCKS IN EACH FRAME (JAPAN)

A proposal is made to study on the maximum coded frame rate specification more appropriate for codecs with DSP oriented architecture toward the final Recommendation. One way to secure compatibility is illustrated where the decoder indicates its "minimum processing period per significant block" to the coder, then the coder counts the number of significant blocks in each frame and sends dummy signals if it exceeds the decoder capability by keeping the minimum coded frame interval as well.

#457 IMPROVEMENTS OF INTRA MODE (JAPAN)

The following proposals are made concerning INTRA mode based on simulation results and hardware consideration;

1) DC-offset values (Y, C_R, C_B) for a macroblock are transmitted. All the transform coefficients for the input block relative to the DC-offset values are subject to transmission, including differential DC components, as in INTER coded blocks.
2) DC-offset values in transform coefficient domain are coded with 8 bit FLC.
3) INTRA NOT CODED is defined as one of TYPE3, where only DC-offset values are transmitted.

#458 TYPE4 IN FLEXIBLE HARDWARE SPECIFICATION (JAPAN)

One MC vector for each macroblock is concluded sufficient for the px64 kbit/s Flexible Hardware as well as for the Recommendation, according to the simulation results showing only small differences between RM7 and either of the following two methods;

- 8x8 block based motion compensation (for QCIF),
- first to find a motion vector for 16x16 macroblock, then to decide MC and Loop Filter on/off for each 8x8 sub-block, if the 16x16 motion vector is not zero (CIF and QCIF).

#459 LOOP FILTER PROPOSAL FOR px64 kbit/s FH (JAPAN)

The following proposals are made;

1) RM7 loop filter (121) controlled on a macroblock by macroblock basis by motion vectors,
2) Loop filter on/off is indicated by TYPE3 with differential motion vector (DMV) field,
3) DMV=0 is transmitted as data,

according to such experimental results (CIF and QCIF at p=1) as;

- comparison of 121, 131 and 141 filters,
- comparison of RM7, side information control and coded/non-coded based filter controls.

It is also confirmed that the loop filter is essential even for QCIF.

#460 CODING RESULTS USING ADAPTIVE QUANTIZATION (JAPAN)

Information is provided on adaptive quantization methods assigning smaller step sizes for motion compensated macroblocks, discarding higher sequency coefficients and combinations of these two.

#461 SIGNALLING CODED SUB-BLOCKS (JAPAN)

From the performance and hardware complexity considerations, use of 63 patterns with VLC plus "start of block trick" is supported. For hardware design, decision is requested on the two-dimensional code table(s) for TCOEFF or alternatively the number of signals and their bits that go into the code table(s).

#462 VLC OPTIMIZATION (JAPAN)

1) Two-dimensional VLC for TCOEFF: Code tables optimized at q=1 (10Hz), 6(10Hz), 24(30Hz) are compared with the RM7 table, concluding that the RM7 code table can be a good candidate for the initial compatibility check parameters.
2) VLC for BA: Code tables optimized at q=1 (10Hz), 6 (10Hz) are compared with the RM7 table, concluding the same way as above.
3) DMV=0 attribute: There is no significant difference between sending it as TYPE3 or data at q=1 (10Hz).

#463 SCANNING CLASSES AT HIGHER BIT RATES (JAPAN)

A single scanning class is proposed for the whole bit rate range according to the simulation and hardware experiments at higher bit rates comparing single class (zigzag) and four classes.

#464 COMPARISON BETWEEN BCH CODE AND REED-SOLOMON CODE (JAPAN)

Based on a comparison between BCH(511,493) and Reed-Solomon(1024,992) codes in terms of MTBF, decoding delay, acquisition time, computational steps, etc., the former code is supported. Information on a burst error corrector for BCH (Meggitt decoder) is also provided.

#465 EXACT VIDEO BITRATES AND BIT ALLOCATION IN THE H.221 FRAME STRUCTURE (JAPAN)

The following bit rates are proposed for the Flexible Hardware experiments with illustrations of bit allocations;

	B1			B2 - B6	
p	Audio	Video	FAS/BAS/etc	Video	FAS
1	16	46.4	1.6		
2 (No. 1)	56	0	8	64	0
2 (No. 2)	62.4		1.6	63.2	0.8
6	56		8	63.2	0.8

#466 REQUIREMENTS FOR TEST SIGNAL GENERATOR (JAPAN)

A simple interface such as RS422/449 (64 kbit/s) is suggested, considering those Flexible Hardware which operate at p<=2 and QCIF only implementation.

#467 REVISION OF px64 kbit/s FLEXIBLE HARDWARE SPECIFICATION (JAPAN)

A proposed text is given as summary of the work in Japan.

#468 CONTRIBUTION TO FIRST MEETING OF CCITT SGXV CONCERNING NEGOTIATION PROCEDURES (JAPAN)

This is a contribution submitted to SGXV for the study of audiovisual service intercommunication, focusing on a principle for multi-facility negotiation procedures and extension of the scope of AV242.

#469 VISUAL TELEPHONE COMMUNICATION PROCEDURE (JAPAN)

This is a contribution submitted to SGXV for the study of "system aspects" of visual telephony, focusing on detailed communication procedures specific to visual telephony and C&I signals transmitted during communication.

#470 USA DOMESTIC NETWORK CONSIDERATIONS (USA)

Network restrictions in North America are described with proposals to cope with them.

1) p=1, 2: Only 56 kbit/s of each DS0 channel is unrestricted. International trials involving North America are proposed to use px56 kbit/s with Septet based transmission format. It is also proposed handshaking in the call initiation should include 56 kbit/s operation.
2) p=6, 24: One's density requirement exists for hardware trials and coming

years. Zero byte replacement method is proposed to make sure that the coded bit stream will be transmittable.

#471 QUANTISER CONTROL EVERY 11 MACROBLOCKS
(NORWAY, NETHERLANDS, FRG, FRANCE, SWEDEN, ITALY, UK, GREECE)

It is proposed to assign a new quantizer step size every 11 macroblocks for simulation work using Reference Model.

#472 PROPOSAL FOR USE OF SIMPLIFIED LOOPFILTER
(NORWAY, NETHERLANDS, FRG, FRANCE, SWEDEN, ITALY, UK, GREECE)

Simplified processing at block edges is proposed for the 121 loop filter based on the experimental results that this simplification gives equal picture quality compared with the RM7 filter and on the consideration that it needs 20-40% fewer operations.

$$\begin{array}{|ll} \hline 6 & 3 \\ 3 & 1 \end{array} \;->\; \begin{array}{|l} \hline 1 \end{array} \qquad \begin{array}{ccc} \hline 3 & 6 & 3 \\ 1 & 2 & 1 \end{array} \;->\; \begin{array}{ccc} \hline 1 & 2 & 1 \end{array}$$

#473 INTERNATIONAL CONNECTION OF FLEXIBLE HARDWARE (JAPAN)

It is proposed to carry out international compatibility checks through international telecommunication lines; ISDN for p=1, 2, and leased lines for p=6.

#474 PATENT INFORMATION DISCLOSURE POLICIES (CHAIRMAN)

Statements from 3 organizations.

#475 PRE- IN- AND POST CODEC FILTERING
(NETHERLANDS, FRANCE, FRG, UK, ITALY, SWEDEN, NORWAY, E, GREECE)

An overview is given concerning three clusters of filters to be used or omitted in the Reference Model. Experimental results are also presented on post codec processing which gives similar results to those of noise reduction filter in the loop, and on comparison of two in-codec filters; RM7 filter vs adaptive directional filter.

#476 COMPARISON BOSE-CHAUDHURI-HOCQUENGHEM BCH AND REED SOLOMON
(NETHERLANDS, FRG, UK)

Error correcting performance is compared. BCH is shown adaptable to burst errors. The complexity of BCH and RS is also discussed.

#477 SIMULATION RESULTS RM 7 (NETHERLANDS)

Performance of RM7 at q=1 is presented.

#478 ABOUT THE IMPLEMENTATION OF THE INTRA MODE
(FRG, UK, SWEDEN, NORWAY, FRANCE, ITALY, NETHERLANDS)

The followings are proposed;

1) In an INTRA mode macroblock, all sub-blocks have to be coded in INTRA mode and the CBP does not exist.
2) TYPE2 indication of whole GOB being coded in INTRA is removed on the

grounds that bit saving is only 1% and video multiplex becomes simplified.

#479 RM7 SIMULATIONS AT 64 kbit/s; FULL CIF & QCIF (FRANCE)

Performance of RM7 is presented.

#480 REGULATION AT THE MACRO BLOCK LEVEL (FRANCE)

It is pointed out that the coding control method defined in RM7 gives overflow in SWING for CIF and very bad buffer regulation for QCIF. Another coding control method to assign a new quantizer step size on a macroblock basis and to transmit differential values of the step size is found to solve the problem.

#481 PROPOSAL FOR A NEW 63 PATTERN BLOCK ADDRESSING TECHNIQUE (FRANCE, NORWAY, UK, SWEDEN, NETHERLANDS, FRG, ITALY)

A combination of the 63 pattern method and 2-D VLC with the "start of block trick" is proposed to replace the previous 7 pattern CBP method, since it requires less hardware and brings a gain in terms of bits and SNR.

#482 VIDEO TAPE DEMONSTRATION (FRANCE)

A list of tape demonstrations concerning simulation and hardware experimental results.

#483 PATENTS APPLICATIONS BY CNET ON LOW BIT RATE CODING (CNET - FRANCE TELECOM)

Four relevant patents are informed.

#484 PICTURE AND GOB HEADER BITS (SWEDEN)

Possibilities to decrease overhead bits in Picture and GOB headers are indicted toward the final Recommendation. Possible emulations of GBSC by error free video data are also discussed according to the code tables in Doc. #449.

#485 VIDEO DATA BUFFERING (JAPAN)

It is pointed out that some specification is required in addition to the minimum differential TR values and maximum number of bits per coded picture, in order to secure stable decoder operation. Two alternatives are listed;

a. to define a permitted limit of deviation of the positions of PSC on the transmission line from the constant frame reference timing,
b. to define a permitted limit of delay between the source coder input of a frame and the transmission coder output of the corresponding PSC.

#486 RM7 MODIFICATION TO ALLOW IMPORTANT MACRO-BLOCK IDENTIFICATION FOR SELECTIVE CODING (AT&T)

Use of tag-bit for indicating important macroblocks is proposed to improve performance in regions of interest. Possible special treatment is for coding, post-processing or error recovery. If necessary this indication can be proprietary, with the possibility of resorting to predetermined default mode in unconcerned codecs.

#487 INFORMATION ON A MEANS FOR IMPLEMENTATION OF REED-SOLOMON ERROR CORRECTION FOR px64 kbit/s VIDEO TELEPHONY (USA)

Detailed implementation of Reed-Solomon error correcting codes is presented with full description of hardware and software, dividing the error correcting procedure into three tasks; checksum generation, syndrome generation and error corrector.

#488 FLEXIBLE HARDWARE STATUS AND PLANS (AT&T BELL LABS, BELLCORE)

A plan to implement a PC plug-in board system is described, which performs audio coding, framing structure, FEC and ISDN interconnectivity. This system is placed between a video codec and the ISDN channel for interworking with other systems, either local or remote.

#489 COMPUTER IMPLEMENTATION OF REFERENCE MODEL 7, AND EVALUATION OF RESULTS (AT&T)

RM7 is used to compare tradeoffs in spatio-temporal artifacts for 'Claire' sequence with 7.5Hz, 10Hz, 15Hz and 30Hz at q=1, concluding that RM7 seems robust enough to code low activity sequences over wide range of frame rates. It is pointed out that 'Claire' can be coded at 15Hz instead of 10Hz with hardly noticeable increase in spatial artifacts.

#490 RM7 IMPROVEMENT BY CONDITIONAL MOTION-COMPENSATED INTERPOLATION (AT&T)

A CMCI based coding scheme is proposed, where the traditional motion compensated predictive coding structure is exploited to code temporally distant frames, while the intermediate frames are coded by motion interpolative coding using the reconstructed neighboring frames. It is concluded that CMCI offers potential for improved temporal rendition, or alternatively for a given temporal resolution, it offers the potential of improved spatial resolution at the expense of added delay.

#491 A SIGNAL GENERATOR TO TEST px64 kbit/s VIDEO DECODERS (DELTA INFORMATION SYSTEMS)

Technical characteristics of the signal generator is given, which provides coded bit streams for both an artificial test sequence and a real-life image sequence.

#492 BASIC FEATURES OF THE H.221-MULDEX INTEGRATED CIRCUIT (ITALY)

Information is provided on an LSI which implements H.221 protocol and multiplexes up to 8 sources within the 64 kbit/s input stream.

#493 BELLCORE POLICY ON PATENTS RELATING TO STANDARDS (BELLCORE)

Statement on the licensing policy and the information disclosure policy for patents relating to standards.

#494 PATENT DISCLOSURE (BELLCORE)

Information on three relevant patents.

#495 INTERCOMMUNICATION AMONG AUDIO/VISUAL TERMINALS FOR FLEXIBLE HARDWARE TRIAL (AT&T, BELLCORE, CLI, DIS, VTC, PICTURETEL)

A detailed description is provided on intercommunication procedure and the framing structure between audiovisual terminals capable of operating in a single or multiple 64 kbit/s channels, following closely the existing H.221 and AV242. Some unresolved issues are also listed.

#496 SMALL MODIFICATION OF IDCT MISMATCH SPECIFICATION (SWEDEN)

Considering a possible strategy of refreshing 3 macroblocks per coded picture, change of the refresh interval specification to "at least every 132 coded frames" is proposed.

#497 SIGNALLING QUANTIZER STEPSIZE CHANGE IN TYPE2 OR TYPE3 (FINLAND)

Observations are first given that RM7 with QCIF resulted in coding control instability, and the problem was solved by changing the quantizer step size every 11 macroblocks. A way to reduce bit rates for signalling is then presented, where the change of quantizer step size is restricted to occur regularly once in a GOB or or every 11th macroblock (three times in a GOB).

#498 BURST ERROR CORRECTING BOSE-CHAUDHURI-HOQUENGHEM (BCH) CODING FOR THE p*64 kbit/s H261 VIDEO CODEC (UK)

BCH(511,484) coding is proposed since its 11 bits burst error correcting capability covers substantially both random error and burst error correcting requirements with very simple hardware.

Temporary Documents

No. 1 Agenda for the Oslo meeting (Chairman)
No. 2 Available documents (Chairman)
No. 3 List of tape demonstrations (Chairman)
No. 4 Licensing policy of patents relevant to CCITT Recommendations on px64 kbit/s codec (Chairman)
No. 5 Proposal on extending the scope of Rec. H.261 to lower bit rates (Specialists Group on coding for Visual Telephony)
No. 6 Report of the interregnum activities (Specialists Group on coding for Visual Telephony)
No. 7 Codec interfaces with network (Chairman)
No. 8 Liaison letter to related organisations (ISO/IEC JTC1/SC2/WG8)
No. 9 INTRA mode definition (Small group)
No.10 RM8 and action points (Small group)
No.11 Specification for p*64 kbit/s Flexible Hardware (Small group)
No.12 Forward error correction - FEC (Small group)
No.13 Draft report of the fifteenth meeting in Oslo (Chairman)
No.14 Progress report of the interregnum activities - Part 2 (Specialists Group on coding for Visual Telephony)

LIST OF TAPE DEMONSTRATIONS (March 7, 1988)

	Topics	Source	Doc.
a	RM7 simulation at 4 frame rates	AT&T	#489
b	Higher bit rate operation of RM7	Japan	#455
c	Quantizer step size control at QCIF	Finland	#497
d	RM7 at CIF	France	#479
e	RM7 at QCIF and regulation at MB level	France	#480
f	RM7 + 63 patterns block addressing technique	France	#481
g	Flexible Hardware at 64 kbit/s	France	#482
h	Reference Model 7	NL	#446
i	Pre-, In- and Post-codec filtering	NL	#475
j	Motion vector for 8x8 blocks	UK	#453
k	Flexible Hardware	UK	-
l	MC for 8x8 blocks	Japan	#458
m	Loop filter coefficients and control	Japan	#459
n	Simplified loop filter	Norway	#472
o	Adaptive quantization	Japan	#460
p	Improvements of INTRA mode	Japan	#457
q	Scanning classes at higher bit rates	Japan	#463

RM8 AND ACTION POINTS

I. RM8

The following modifications have been introduced in RM7;

- Intra mode: see § 6.3/Doc. #499R note that the 2D-VLC always includes the EOB word).

- Type 3 VLC (Annex 4 to Doc. #499R)

Inter coded	1
MC coded	0 1
MC not coded	0 0 1
Intra	0 0 0 1
Inter coded + Q	0 0 0 0 1
MC coded + Q	0 0 0 0 0 1
Intra + Q	0 0 0 0 0 0 1

- Coded Block Pattern (#481, #449)

  The numbering of the patterns are defined as follows:

Y_1	Y_2		C_B	C_R
Y_3	Y_4			

  Pattern number = $32*Y_1 + 16*Y_2 + 8*Y_3 + 4*Y_4 + 2*C_B + C_R$
  See Appendix 1 for the VLC.
  See Appendix 2 for the 2D-VLCs.

- New filter in the loop (#472)

  See Appendix 3.

- Buffer regulation

  The step size of the quantizer is transmitted every 11 macroblocks. The number of bits for the step size as well as for the Type 3 VLC must be taken into account.

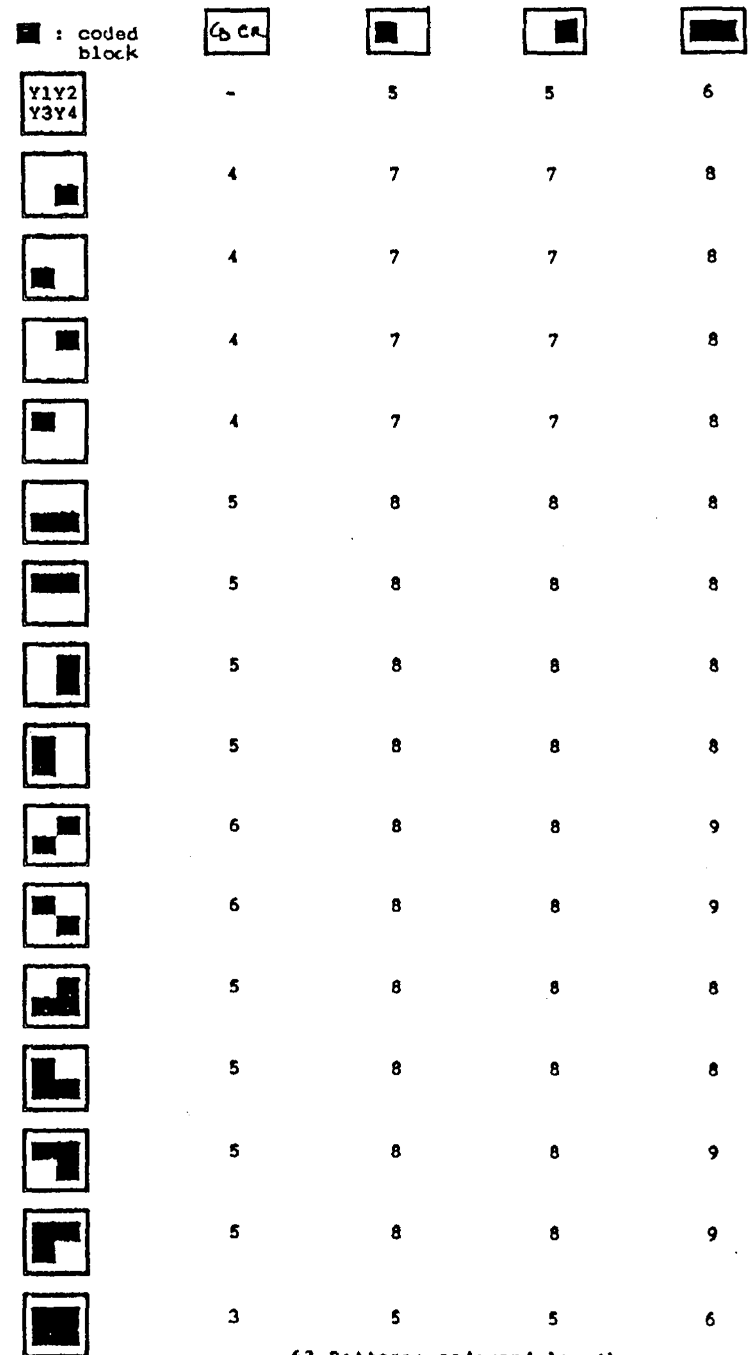
II. Action points

1. Optimization of type 3 VLC
2. Buffer regulation
3. Impact of the modification at q x 64 kbit/s q>1
4. QCIF simulation work
5. Up and down converters CIF ⟷ QCIF
6. Refresh mode: minimum step size of the quantizer
7. Scene change
8. Simulation at CIF and QCIF taking into account the exact number of bits as defined in the hardware specification document.

<u>63 PATTERNS VLC</u>

Pattern number : 32*Y1 + 16*Y2 + 8*Y3 + 4*Y4 + 2*CB + CR

Pattern	Length	Codeword
60	3	000
4	4	0010
8	4	0011
16	4	0100
32	4	0101
12	5	01100
48	5	01101
20	5	01110
40	5	01111
28	5	10000
44	5	10001
52	5	10010
56	5	10011
1	5	10100
61	5	10101
2	5	10110
62	5	10111
24	6	110000
36	6	110001
3	6	110010
63	6	110011
5	7	1101000
9	7	1101001
17	7	1101010
33	7	1101011
6	7	1101100
10	7	1101101
18	7	1101110
34	7	1101111
7	8	11100000
11	8	11100001
19	8	11100010
35	8	11100011
13	8	11100100
49	8	11100101
21	8	11100110
41	8	11100111
14	8	11101000
50	8	11101001
22	8	11101010
42	8	11101011
15	8	11101100
51	8	11101101
23	8	11101110
43	8	11101111
25	8	11110000
37	8	11110001
26	8	11110010
38	8	11110011
29	8	11110100
45	8	11110101
53	8	11110110
57	8	11110111
30	8	11111000
46	8	11111001
54	8	11111010
58	8	11111011
31	8	11111100
47	8	11111101
27	9	111111100
39	9	111111101
55	9	111111110
59	9	111111111



<u>63 Patterns codeword length</u>

Codes for Coefficient Data

The last bit 's' denotes the sign of the level, '0' for +ve and '1' for -ve.

RUN	¦ LEVEL ¦	CODE
EOB		10
0	1	1s IF FIRST COEFFICIENT
0	1	11s NOT FIRST COEFFICIENT
0	2	0100 s
0	3	0010 1s
0	4	0000 110s
0	5	0010 0110 s
0	6	0010 0001 s
0	7	0000 0010 10s
0	8	0000 0001 1101 s
0	9	0000 0001 1000 s
0	10	0000 0001 0011 s
0	11	0000 0001 0000 s
0	12	0000 0000 1101 0s
0	13	0000 0000 1100 1s
0	14	0000 0000 1100 0s
0	15	0000 0000 1011 1s
1	1	011s
1	2	0001 10s
1	3	0010 0101 s
1	4	0000 0011 00s
1	5	0000 0001 1011 s
1	6	0000 0000 1011 0s
1	7	0000 0000 1010 1s
2	1	0101 s
2	2	0000 100s
2	3	0000 0010 11s
2	4	0000 0001 0100 s
2	5	0000 0000 1010 0s
3	1	0011 1s
3	2	0010 0100 s
3	3	0000 0001 1100 s
3	4	0000 0000 1001 1s
4	1	0011 0s
4	2	0000 0011 11s
4	3	0000 0001 0010 s
5	1	0001 11s
5	2	0000 0010 01s
5	3	0000 0000 1001 0s
6	1	0001 01s
6	2	0000 0001 1110 s

7	1	0001 00s
7	2	0000 0001 0101 s
8	1	0000 111s
8	2	0000 0001 0001 s
9	1	0000 101s
9	2	0000 0000 1000 1s
10	1	0010 0111 s
10	2	0000 0000 1000 0s
11	1	0010 0011 s
12	1	0010 0010 s
13	1	0010 0000 s
14	1	0000 0011 10s
15	1	0000 0011 01s
16	1	0000 0010 00s
17	1	0000 0001 1111 s
18	1	0000 0001 1010 s
19	1	0000 0001 1001 s
20	1	0000 0001 0111 s
21	1	0000 0001 0110 s
22	1	0000 0000 1111 1s
23	1	0000 0000 1111 0s
24	1	0000 0000 1110 1s
25	1	0000 0000 1110 0s
26	1	0000 0000 1101 1s
ESCAPE		0000 01

RUN is a 6 bit fixed length code

0	0000 00
1	0000 01
2	0000 10
.	.
.	.
63	1111 11

LEVEL is an 8 bit fixed length code

-128	1000 0000	FORBIDDEN
-127	1000 0001	
.	.	
.	.	
-2	1111 1110	
-1	1111 1111	
0	0000 0000	FORBIDDEN
1	0000 0001	
2	0000 0010	
.	.	
127	0111 1111	

1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2 4 2	2
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1
1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1 2 1	1

Specification for p*64 kbit/s Flexible Hardware

CONTENTS

An outline block diagram of the codec is given in Figure 1.

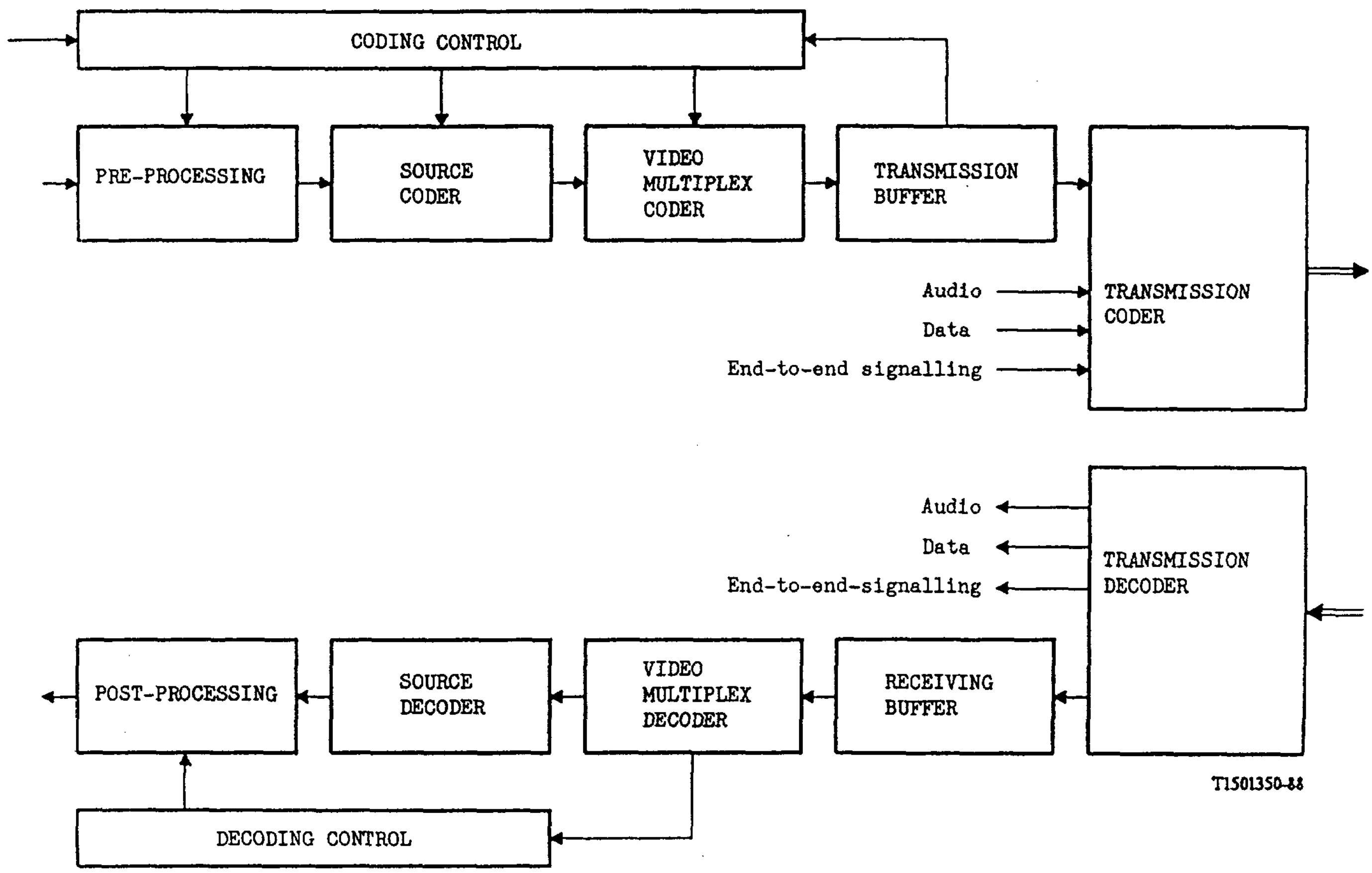


Figure 1 Outline blockdiagram of the codec

1. Source Coder

1.1 Source format

The source coder operates on non-interlaced pictures occurring 30000/1001 (approximately 29.97) times per second. The tolerance on picture frequency is +/-50 ppm.

Pictures are coded as luminance and two colour difference components (Y, C_B

and C_R). These components and the codes representing their sampled values are as defined in CCIR Recommendation 601.

Black = 16
White = 235
Zero colour difference = 128
Peak colour difference = 16 and 240

These values are nominal ones and the coding algorithm functions with input values of 1 through to 254. Values of 0 and 255 are not allowed.

Two picture scanning formats are specified.

In the first format (CIF), the luminance sampling structure is 288 lines per picture, 352 pels per line in an orthogonal arrangement. Sampling of each of the two colour difference components is at 144 lines, 176 pels per line, orthogonal. Colour difference samples are sited such that their block boundaries coincide with luminance block boundaries as shown in Figure 2. The picture area covered by these numbers of pels and lines has an aspect ratio of 4:3 and corresponds to the active portion of the local standard video input.

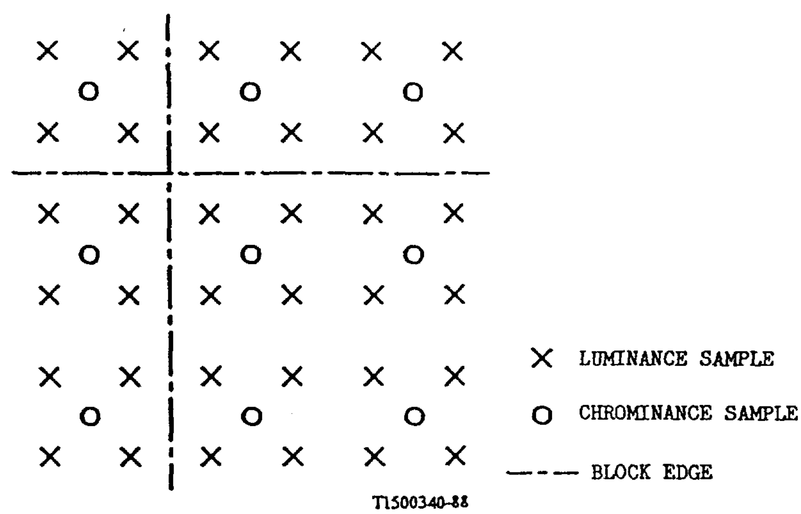


Figure 2 Positioning of luminance and chrominance samples

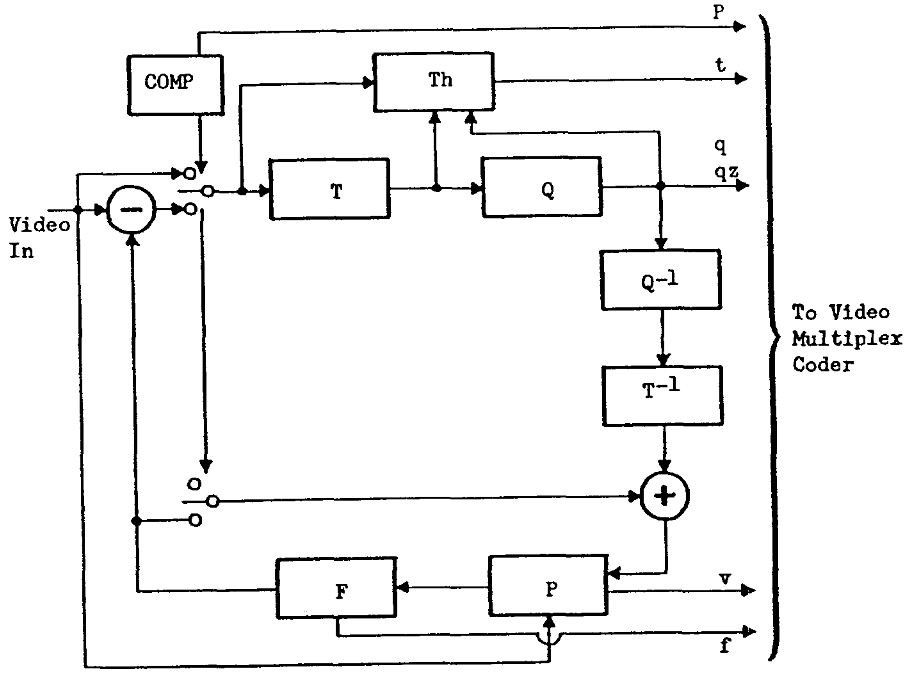
The second video format (QCIF) has half the number of pels and half the number of lines stated above.

The maximum picture rate (CIF and QCIF) is under study. Means shall be provided to restrict the maximum picture rate of encoders by having at least 0, 1, 2 or 3 non-transmitted pictures between transmitted ones. Selection of this minimum number will be performed manually.

All codecs must be able to operate using QCIF. Some codecs can also operate with CIF.

1.2 Video source coding algorithm

The video coding algorithm is shown in generalised form in Figure 3. The main elements are prediction, block transformation, and quantisation.



COMP	Comparator for intra/inter
Th	Threshold
T	Transform
Q	Quantizer
P	Picture memory with motion compensated variable delay
F	Loop filter
p	Flag for intra/inter
t	Flag for transmitted or not
q	Quantizing index for transform coefficients
qz	Quantizer indication
v	Motion vector
f	Switching on/off of the loop filter

Figure 3 Video coding algorithm

The prediction error (INTER mode) or the input picture (INTRA mode) is subdivided into 8 pel by 8 line blocks which are segmented as transmitted or non-transmitted. The criteria for choice of mode and transmitting a block are not subject to recommendation and may be varied dynamically as part of the data rate control strategy. Transmitted blocks are transformed and resulting coefficients are quantised and variable length coded.

1.2.1 Prediction

The prediction is inter-picture and may be augmented by motion compensation (§ 1.2.2) and a spatial filter (§ 1.2.3).

1.2.2 Motion compensation

Motion compensation is optional in the encoder. The decoder will accept one vector per macroblock. Both horizontal and vertical components of these motion vectors have integer values not exceeding +/- 15. The vector is used for all four luminance blocks in the macroblock. The motion vector for both colour difference blocks is derived by halving the component values of the macroblock vector and truncating towards zero.

A positive value of the horizontal or vertical component of the motion vector signifies that the prediction is formed from pels in the previous picture which are spatially to the right or below the pels being predicted.

Motion vectors are restricted such that all pels referenced by them are within the coded picture area.

1.2.3 Loop filter

The prediction process may be modified by a two-dimensional spatial filter which operates on pels within a predicted 8 by 8 block.

The filter is separable into one dimensional horizontal and vertical functions. Both are non-recursive with coefficients of 1/4, 1/2, 1/4 except at block edges where one of the taps would fall outside the block. In such cases the 1-D filter is changed to have coefficients of 0, 1, 0. Full arithmetic precision is retained with rounding to 8 bit integer values at the 2-D filter output. Values whose fractional part is one half are rounded up.

The filter is switched on for all 6 blocks in a macroblock if the macroblock is declared to have a motion vector. (See TYPE3).

Note: The filter is applied even if the motion vector is zero. An encoder without motion compensation can switch on the loop filter by signalling a macroblock as motion compensated with a zero vector.

1.2.4 Transformer

Transmitted blocks are coded with a separable 2-dimensional Discrete Cosine Transform of size 8 by 8. The input to the forward transform and output from the inverse transform have 9 bits. The transfer function of the inverse transform is given by

$$f(x,y) = \frac{1}{4} \sum_{u=0}^{7} \sum_{v=0}^{7} C(u)\, C(v)\, F(u,v) \cos\left[\frac{\pi u(2x+1)}{16}\right] \cos\left[\frac{\pi v(2y+1)}{16}\right]$$

with $u,v,x,y = 0, 1, 2, \ldots, 7$

where x,y = spatial coordinates in the pixel domain
u,v = coordinates in the transform domain

$$C(u), C(v) = \begin{cases} 1/\sqrt{2} & \text{for } u,v = 0 \\ 1 & \text{otherwise} \end{cases}$$

The arithmetic procedures for computing the transforms are not defined, but the inverse one should meet the error tolerance specified in Appendix 1.

1.2.5 Quantisation

The number of quantisers is 32. Their characteristics are given in Appendix 2. Assignment of quantisers is as in Figure 4.

1.2.6 Clipping

To prevent quantisation distortion of transform coefficient amplitudes

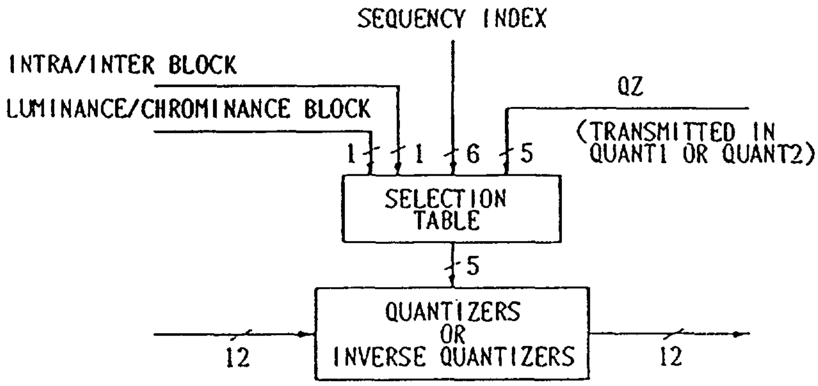


Figure 4 Quantiser assignment

causing arithmetic overflow in the encoder and decoder loops, clipping functions are inserted. In addition to those in the inverse transform, a clipping function is applied at both encoder and decoder to the reconstructed picture which is formed by summing the prediction and the prediction error as modified by the coding process. This clipper operates on resulting pel values less than 0 or greater than 255, changing them to 0 and 255 respectively.

1.3 Data rate control

Sections where parameters which may be varied to control the rate of generation of coded video data include processing prior to the source coder, the quantiser, block significance criterion and temporal subsampling. The proportions of such measures in the overall control strategy are not subject to recommendation.

When invoked, temporal subsampling is performed by discarding complete pictures. Interpolated pictures are not placed in the picture memory.

1.4 Forced updating

This function is achieved by forcing the use of the INTRA mode of the coding algorithm. The update pattern is not defined. For control of accumulation of inverse transform mismatch error a block should be forcibly updated at least once per every 132 times it is transmitted.

2. Video Multiplex Coder

2.1 Data Structure

Note 1: Unless specified otherwise the most significant bit is transmitted first.
Note 2: Unless specified otherwise Bit 1 is transmitted first.
Note 3: Unless specified otherwise all unused or spare bits are set to '1'.

2.2 Video Multiplex arrangement

The video multiplex is arranged in a hierarchical structure with four layers. From top to bottom the layers are:

Picture
Group of Blocks (GOB)
Macroblock (MB)
Block

2.2.1 Picture Layer

Data for each Picture consists of a Picture Header followed by data for GOBs. The structure is shown in Figure 5. Picture Headers for dropped pictures are not transmitted.

PSC	TR	TYPE1	PEI1	PARITY	PEI2	PSPARE	GOB Data

Figure 5 Structure of the Picture Layer

Picture Start Code (PSC) 20 bits

A word of 20 bits. Its value is 0000 0000 0000 0001 0000

Temporal Reference (TR) 5 bits

A five bit number which can have 32 possible values. It is formed by incrementing its value in the previously transmitted Picture header by 1 plus the number of non-transmitted pictures (at 29.97 Hz) since that last transmitted one. The arithmetic is performed with only the 5 LSBs.

Type Information (TYPE1) 13 bits

Information about the complete picture;

Bit 1 Split screen indicator. '0' off, '1' on.
Bit 2 Document camera. '0' off, '1' on.
Bit 3 Freeze Picture Release. Under study.
Bit 4 Format indicator. '0' QCIF, '1' CIF.
Bits 5 to 13 Under study.

Extra Insertion Information (PEI1) 1 bit

A bit which signals the presence of the following optional data field.

Parity Information (PARITY) 0 or 8 bits

For optional use and present only if the PEI1 bit is set to '1'. Eight parity bits each representing odd parity of the aggregate of the corresponding bit planes of the locally decoded PCM values of Y, C_B and C_R in the previous picture period.

Extra Insertion Information (PEI2) 1 bit

A bit which signals the presence of the following optional data field.

Spare Information (PSPARE) 0 or 16 bits

Sixteen bits are present when the PEI2 bit is set to '1'. The use of these bits is under study.

2.2.2 Group of Blocks Layer

Each picture is divided into Groups of Blocks (GOBs). A group of blocks (GOB) comprises one twelfth of the CIF or one third of the QCIF picture areas (see Figure 6). A GOB relates to 176 pels by 48 lines of Y and the spatially corresponding 88 pels by 24 lines of each of C_R and C_B.

1	2
3	4
5	6
7	8
9	10
11	12

CIF

1
3
5

QCIF

Figure 6 Arrangement of GOBs in a Picture

Data for each Group of Blocks consists of a GOB Header followed by data for macroblocks. The structure is shown in Figure 7. Each GOB Header is transmitted once between Picture Start Codes in the CIF or QCIF sequence numbered above, even if no macroblock data is present in that GOB.

GBSC	GN	TYPE2	QUANT1	GEI	GSPARE	MB Data

Figure 7 Structure of Group of Blocks Layer

Group of Blocks Start Code (GBSC) 16 bits

A word of 16 bits, 0000 0000 0000 0001.

Group Number (GN) 4 bits

Four bits indicating the position of the group of blocks. The bits are the binary representation of the numbers in Figure 6. Group numbers 13, 14 and 15 are reserved for future use. Group number 0 is used in the PSC.

Type Information (TYPE2) 6 bits

TYPE2 is 6 bits which give information about all the transmitted blocks in a group of blocks.

Bits 1 to 6 Spare, under study.

Quantiser Information (QUANT1) 5 bits

A fixed length codeword of 5 bits which indicates the quantiser table(s) to be used in the group of blocks until overridden by any subsequent QUANT2. The codewords are given in Appendix 3.

Extra Insertion Information (GEI) 1 bit

A bit which signals the presence of the following optional data field.

Spare Information (GSPARE) 0 or 16 bits

Sixteen bits are present if the GEI bit is set to '1'. The use of these bits is under study.

2.2.3 Macroblock Layer

Each GOB is divided into 33 macroblocks as shown in Figure 8. A macroblock relates to 16 lines by 16 pels of Y and the spatially corresponding 8 lines by 8 pels of each of C_B and C_R.

1	2	3	4	5	6	7	8	9	10	11
12	13	14	15	16	17	18	19	20	21	22
23	24	25	26	27	28	29	30	31	32	33

Figure 8 Arrangement of macroblocks in a GOB

Data for a macroblock consists of a MB Header followed by data for blocks (Figure 9). Elements are omitted when not required.

MBA	TYPE3	QUANT2	MVD	CBP	Block Data

Figure 9 Structure of macroblock layer

Macroblock Address (MBA) Variable Length

A variable length codeword indicating the position of a macroblock within a group of blocks. The transmission order is as shown in Figure 8. For the first transmitted block in a GOB, MBA is the absolute address in Figure 8. For subsequent macroblocks, MBA is the difference between the absolute addresses of the macroblock and the last transmitted macroblock. The code table for MBA is given in Appendix 4.

An extra codeword is available in the table for bit stuffing between macroblocks. This codeword should be discarded by decoders.

MBA is always included in transmitted macroblocks.

Macroblocks are not transmitted when they contain no information for that part of the picture.

Type Information (TYPE3) Variable Length

Variable length codewords giving information about the macroblock and which data elements are present. Macroblock types, included elements and VLC words are listed in Table 1.

TYPE3 is always included in transmitted macroblocks.

Table 1 TYPE3

Intra/Inter/MC	QUANT2	MVD	CBP	TCOEFF	VLC
Intra				x	0001
Intra	x			x	0000 001
Inter			x	x	1
Inter	x		x	x	0000 1
MC		x			001
MC		x	x	x	01
MC	x	x	x	x	0000 01

'x' means that the item is present in the macroblock

Quantiser (QUANT2) 5 bits

QUANT2 is present only if so indicated by TYPE3.

A codeword of 5 bits signifying the quantiser table(s) to be used for this and any following blocks in the group of blocks until overridden by any subsequent QUANT2.

Codewords for QUANT2 are the same as for QUANT1.

Motion Vector Data (MVD) Variable length

Motion Vector Data is included for all MC macroblocks. MVD is obtained from the macroblock vector by subtracting the vector of the preceding macroblock. For this calculation the vector of the preceding macroblock is regarded as zero in the following three situations:

1) Evaluating MVD for macroblocks 1, 12 and 23.
2) Evaluating MVD for macroblocks in which MBA does not represent a difference of 1.
3) TYPE3 of the previous macroblock was not MC.

MVD consists of a variable length codeword for the horizontal component followed by a variable length codeword for the vertical component. Variable length codes are given in Appendix 5.

Advantage is taken of the fact that the range of motion vector values is constrained. Each VLC word represents a pair of difference values. Only one of the pair will yield a macroblock vector falling within the permitted range.

Coded Block Pattern (CBP) Variable length

CBP is present if indicated by TYPE3. The codeword gives a pattern number signifying those blocks in the macroblock for which transform coefficients are transmitted. The pattern number is given by

$$32*P_1 + 16*P_2 + 8*P_3 + 4*P_4 + 2*P_5 + P_6$$

where P_n is 1 if coefficients are present for block n, else 0. Block numbering is given in Figure 10.

The code table for CBP is given in Appendix 6.

2.2.4 Block Layer

A macroblock comprises four luminance blocks and one of each of the two colour difference blocks.

```
 -------       -------       -------
| 1 | 2 |     |       |     |       |
|-------|     |   5   |     |   6   |
| 3 | 4 |     |       |     |       |
 -------       -------       -------
    Y            CB            CR
```

Figure 10 Arrangement of blocks in a macroblock

Data for a block consists of codewords for transform coefficients followed by an end of block marker (Figure 11). The order of block transmission is as in Figure 10.

```
 --------------
| TCOEFF | EOB |
 --------------
```

Figure 11 Structure of Block Layer

Transform Coefficients (TCOEFF)

Transform coefficient data is always present for all 6 blocks in a macroblock when TYPE3 indicates INTRA. In other cases TYPE3 and CBP signal which blocks have coefficient data transmitted for them. The quantised transform coefficients are sequentially transmitted according to the sequence given in Appendix 7.

The most commonly occurring combinations of zero-run and the following value are encoded with variable length codes. Other combinations of (RUN, LEVEL) are encoded with a 20 bit word consisting of 6 bits ESCAPE, 6 bits RUN and 8 bits level. For the variable length encoding there are two code tables, one being used for the first transmitted coefficient in INTER and MC blocks, the other for all other coefficients except the first one in INTRA blocks.

Codes are given in Appendix 8.

For INTRA blocks the first coefficient is the transform dc value linearly quantised with a stepsize of 8 and no dead-zone. The resulting values are represented with 8 bits. A nominally black block will give 0001 0000 and a nominally white one 1110 1011. The code 1000 0000 is replaced by 1111 1111.

Coefficients after the last non-zero one are not transmitted. EOB (End of Block code) is always the last item in blocks for which coefficients are transmitted.

2.3 Multipoint considerations

Both switched and continuous presence multipoint are under study. The feasibility of the latter is increased by the two formats of CIF and QCIF together with the configuration of GOBs, which permit four QCIF sources to be combined into one CIF stream.

2.3.1 Freeze Picture Request

Causes the decoder to freeze its received picture until a picture freeze release signal is received or a timeout period has expired. The transmission method for this control signal and the timeout period are under study.

2.3.2 Fast Update Request

Causes the encoder to encode its next picture in INTRA mode with coding parameters such as to avoid buffer overflow. The transmission method for this control signal is under study.

2.3.3 Picture Freeze Release

A signal from an encoder which has responded to a Fast Update Request and causes a decoder to exit from its picture freeze mode and display decoded pictures in the normal manner. The transmission method for this signal is under study. (See § 2.2.1, TYPE1, Bit 3)

2.3.4 Data continuity

The protocol adopted for ensuring continuity of data channels in a switched multipoint connection is handled by the message channel. Under study.

3. Transmission Coder

3.1 Bit rate

The bit rate including audio and optional data channels is p*64 kbit/s where p is an integer between 1 and 30 both inclusive. Some codecs may have restrictions on the available values of p. Desirable values of p are 1, 2, 6, 24 and 30. The corresponding video rates are:

46.4 kbit/s	(64-16-FAS-BAS)
62.4 kbit/s	(64-FAS-BAS)
312.0 kbit/s	5*(64-FAS-BAS)
1435.2 kbit/s	23*(64-FAS-BAS)
1809.6 kbit/s	29*(64-FAS-BAS)

The codec output clock rate source shall be switchable between either a free running internal source or a source synchronised to the received data from the network. When in free running mode the tolerance on output clock rate will be +/- 50 ppm of nominal. When in synchronised mode the synchronism should be maintained when the frequency of the received data clock is within +/- 50 ppm of nominal.

Selection of free-running or synchronised mode will be performed manually at the encoder.

3.2 Video Data Buffering

Under study. The specification will cover both post-coding and pre-coding buffers. The effect on overall system delay will be considered.

When operating with CIF the number of bits created by coding any single picture must not exceed 256 Kbits.

When operating with QCIF the number of bits created by coding any single picture must not exceed 64 Kbits. This requirement is consistent with combining four QCIF sources into one CIF stream at a continuous presence type of multipoint unit.

In both the above cases the bit count includes the Picture Start Code and all other data related to that picture. K = 1024.

Encoder buffer overflow and underflow are not permitted. Underflow can be prevented by use of dummy block in the error corrector block framing. See Figure 12.

3.3 Video clock justification

Video clock justification is not provided.

3.4 Frame structure

3.4.1 Frame structure

The frame structure is defined in Recommendations H.221 and H.222.

3.4.2 Bit assignment in Application Channel

When the Application Channel is present, bits 17 to 80 are set to '0' until agreed otherwise.

3.4.3 Timeslot positioning

According to Recommendation I.431.

3.5 Audio coding

For p > 1, Recommendation G.722 56/48 kbit/s audio, 0/8 kbit/s data and 8 kbit/s service channel is used in the first timeslot (primary rate interface) or channel (ISDN basic access).

For p = 1 the decoder may disregard the 16 kbit/s assigned for audio in the first two bits of each octet.

The delay of the encoded audio relative to the encoded video at the channel output is under study.

3.6 Data transmission

For p>2 one or more timeslots may be allocated as data channels of 64 kbit/s each. The first channel uses the fourth timeslot of a primary rate interface.

Positioning of the other channels, and possible restrictions on availability at lower overall bit rates are under study. The BAS codes used to signal that these data channels are in use are specified in Recommendation H.221.

3.7 Forward Error Correction for Coded Video Signal

3.7.1 Error correcting code

Double error correcting BCH(511,493).

3.7.2 Generator polynomial

$g(x)=(x^9+x^4+1)(x^9+x^6+x^4+x^3+1)$

3.7.3 ECC bits transmission

Independent framing is used with multiframe of 8 frames, where a 512-bit frame consists of 1-bit framing, 493-bit data and 18-bit ECC (Error Correcting Code). The frame alignment pattern is

$$(S_0S_1S_2S_3S_4S_5S_6S_7)=(0001101X),$$

where X is a reserved bit for future multiframe use and set to 1. See Figure 12 for the frame arrangement. Note that the ECC is calculated against the 493-bit including Fill Indicator.

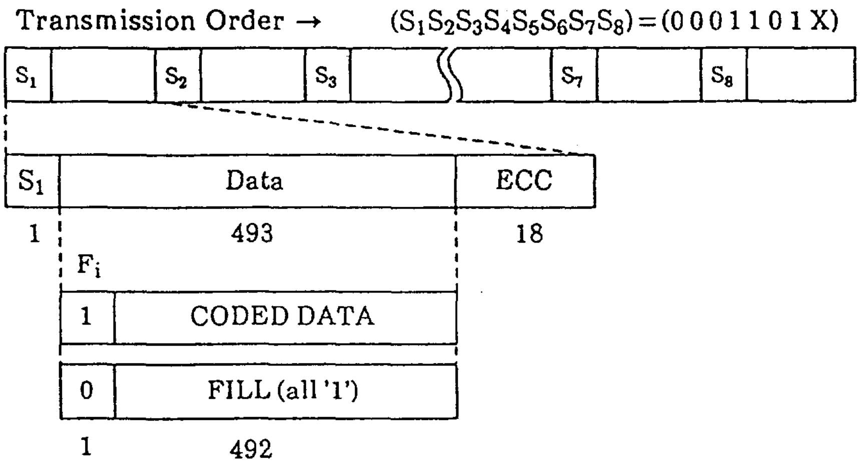


Figure 12 Error correcting frame

3.8 Encryption

3.9 Bit Sequence Independence Restrictions

3.10 Network interface

Access at the primary rate is with vacated timeslots as per Recommendation I.431.

For 1544 kbit/s interfaces the default H0 channel is timeslots 1 to 6.

For 2048 kbit/s interfaces the default H0 channel is timeslots 1-2-3-17-18-19.

Interfaces using ISDN basic access - Recommendation I.420.

END

Specification for Inverse DCT

1. Generate random integer pixel data values in the range -L to +H according to the attached random number generator (C version). Arrange into 8x8 blocks by allocating each set of consecutive 8 numbers in a row. Data sets of 10000 blocks each should be generated for (L=256, H=255), (L=H=5) and(L=H=300).

2. For each 8x8 block, perform a separable, orthonormal, matrix multiply, Forward Discrete Cosine Transform (FDCT) using at least 64-bit floating point accuracy.

3. For each block, round the 64 resulting transformed coefficients to the nearest integer values. Then clip them to the range -2048 to +2047. This is the 12-bit input data to the inverse transform.

4. For each 8x8 block of 12-bit data produced by step 3, perform a separable, orthonormal, matrix multiply, Inverse Discrete Cosine (IDCT) using at least 64-bit floating point accuracy. Round the resulting pixels to the nearest integer, and clip to the range -256 to +255. These blocks of 8x8 pixels are the "reference" IDCT output data.

5. For each 8x8 block of 12-bit data produced by step 3, use the proposed IDCT chip or an exact-bit simulation thereof to perform an Inverse Discrete Cosine Transform. Clip the output to the range -256 to +255. These blocks of 8x8 pixels are the "test" IDCT output data.

6. For each of the 64 IDCT output pixels, and for each of the 10,000 block data sets generated above, measure the peak, mean and mean square error between the "reference" and "test" data.

7. For any pixel, the peak error should not exceed 1 in magnitude.
   For any pixel, the mean square error should not exceed 0.06.
   Overall, the mean square error should not exceed 0.02.
   For any pixel, the mean error should not exceed 0.015 in magnitude.
   Overall, the mean error should not exceed 0.0015 in magnitude.

8. All-zeros in must produce all-zeros out.

9. Rerun the measurements using exactly the same data values of step 1, but change the sign on each pixel.

```
                    /*L and H must be long, ie, 32 bits*/
long rand(L,H)
long      L,H;
{
  static long   randx = 1;   /*long is 32 bits*/
  static double   z = (double)0x7fffffff;

  long   i,j;
  double x;                   /*double is 64 bits*/

  randx = (randx * 1103515245) + 12345;
  i = randx & 0x7ffffffe;                 /*keep 30 bits*/
  x = ( (double)i ) / z;                  /* range 0 to 0.99999... */
  x *= (L+H+1);                           /* range 0 to  < L+H+1 */
  j = x ;                                 /*truncate to integer*/
  return( j - L );                    /*range  -L  to  H  */
}
```

Appendix 2/Annex 4 to Doc. #499R

Quantizers

The uniform quantizer is defined by a step g and the threshold T. In this specification, T=g.

$$q_{dec}(n) = T + (n-1)\,g \quad , n = 1,2,\ldots$$

$$q_{dec}(0) = 0$$

Taking into account the negative values the expression becomes:

$$q_{dec}(n) = \frac{n}{|n|}\{T + (|n|-1)\,g\} \quad , |n| = 1, 2, 3,\ldots$$

$$q_{rep}(n) = \frac{q_{dec}(n) + q_{dec}(n + n/|n|)}{2} \quad \text{for } |n| = 1, 2, \ldots$$

$$q_{rep}(0) = 0$$

with q_{dec} the decision level

q_{rep} the representation level

g the quantizer stepsize

T threshold

The quantiser assignment table of Figure 4 is programmed so that the selected quantiser is used for all coefficients except the dc coefficient in INTRA coded blocks.

Appendix 3/Annex 4 to Doc. #499R

Codeword for QUANT1/QUANT2

Codeword for QUANT1/QUANT2 is natural binary representation of its value.

$g = 2x(1+QUANT)$

g: quantizer step size

QUANT: 1 to 31, as transmitted in QUANT1 or QUANT2

Note that '0000 0' is never used for QUANT1 or QUANT2.

Appendix 4/Annex 4 to Doc. #499R VLC Table for Macroblock Addressing

MBA	CODE
1	1
2	011
3	010
4	0011
5	0010
6	0001 1
7	0001 0
8	0000 111
9	0000 110
10	0000 1011
11	0000 1010
12	0000 1001
13	0000 1000
14	0000 0111
15	0000 0110
16	0000 0101 11

MBA	CODE
17	0000 0101 10
18	0000 0101 01
19	0000 0101 00
20	0000 0100 11
21	0000 0100 10
22	0000 0100 011
23	0000 0100 010
24	0000 0100 001
25	0000 0100 000
26	0000 0011 111
27	0000 0011 110
28	0000 0011 101
29	0000 0011 100
30	0000 0011 011
31	0000 0011 010
32	0000 0011 001
33	0000 0011 000
Stuffing	0000 0001 111
Start code	0000 0000 0000 0001

Appendix 5/Annex 4 to Doc. #499R VLC Table for MVD

MVD	CODE
-16 & 16	0000 0011 001
-15 & 17	0000 0011 011
-14 & 18	0000 0011 101
-13 & 19	0000 0011 111
-12 & 20	0000 0100 001
-11 & 21	0000 0100 011
-10 & 22	0000 0100 11
-9 & 23	0000 0101 01
-8 & 24	0000 0101 11
-7 & 25	0000 0111
-6 & 26	0000 1001
-5 & 27	0000 1011
-4 & 28	0000 111
-3 & 29	0001 1
-2 & 30	0011
-1	011
0	1
1	010
2 & -30	0010
3 & -29	0001 0
4 & -28	0000 110
5 & -27	0000 1010
6 & -26	0000 1000
7 & -25	0000 0110
8 & -24	0000 0101 10
9 & -23	0000 0101 00
10 & -22	0000 0100 10
11 & -21	0000 0100 010
12 & -20	0000 0100 000
13 & -19	0000 0011 110
14 & -18	0000 0011 100
15 & -17	0000 0011 010

Appendix 6/Annex 4 to Doc. #499R VLC Table for CBP

CBP	CODE	CBP	CODE
1	1010 0	33	1101 011
2	1011 0	34	1101 111
3	1100 10	35	1110 0011
4	0010	36	1100 01
5	1101 000	37	1111 0001
6	1101 100	38	1111 0011
7	1110 0000	39	1111 1110 1
8	0011	40	0111 1
9	1101 001	41	1110 0111
10	1101 101	42	1110 1011
11	1110 0001	43	1110 1111
12	0110 0	44	1000 1
13	1110 0100	45	1111 0101
14	1110 1000	46	1111 1001
15	1110 1100	47	1111 1101
16	0100	48	0110 1
17	1101 010	49	1110 0101
18	1101 110	50	1110 1001
19	1110 0010	51	1110 1101
20	0111 0	52	1001 0
21	1110 0110	53	1111 0110
22	1110 1010	54	1111 1010
23	1110 1110	55	1111 1111 0
24	1100 00	56	1001 1
25	1111 0000	57	1111 0111
26	1111 0010	58	1111 1011
27	1111 11100	59	1111 1111 1
28	1000 0	60	000
29	1111 0100	61	1010 1
30	1111 1000	62	1011 1
31	1111 1100	63	1100 11
32	0101		

Appendix 7/Annex 4 to Doc. #499R

Transmission Order for Transform Coefficients

1	2	6	7	15	16	28	29
3	5	8	14	17	27	30	43
4	9	13	18	26	31	42	44
10	12	19	25	32	41	45	54
11	20	24	33	40	46	53	55
21	23	34	39	47	52	56	61
22	35	38	48	51	57	60	62
36	37	49	50	58	59	63	64

The most commonly occurring combinations of zero-run and the following value are encoded with variable length codes as listed in the table below. End of Block (EOB) is in this set. Because CBP indicates those blocks with no coefficient data, EOB cannot occur as the first coefficient. Hence EOB can be removed from the VLC table for the first coefficient.

The last bit 's' denotes the sign of the level, '0' for +ve and '1' for -ve.

RUN	¦ LEVEL ¦	CODE
EOB		10
0	1	1s IF FIRST COEFFICIENT
0	1	11s NOT FIRST COEFFICIENT
0	2	0100 s
0	3	0010 1s
0	4	0000 110s
0	5	0010 0110 s
0	6	0010 0001 s
0	7	0000 0010 10s
0	8	0000 0001 1101 s
0	9	0000 0001 1000 s
0	10	0000 0001 0011 s
0	11	0000 0001 0000 s
0	12	0000 0000 1101 0s
0	13	0000 0000 1100 1s
0	14	0000 0000 1100 0s
0	15	0000 0000 1011 1s
1	1	011s
1	2	0001 10s
1	3	0010 0101 s
1	4	0000 0011 00s
1	5	0000 0001 1011 s
1	6	0000 0000 1011 0s
1	7	0000 0000 1010 1s
2	1	0101 s
2	2	0000 100s
2	3	0000 0010 11s
2	4	0000 0001 0100 s
2	5	0000 0000 1010 0s
3	1	0011 1s
3	2	0010 0100 s
3	3	0000 0001 1100 s
3	4	0000 0000 1001 1s
4	1	0011 0s
4	2	0000 0011 11s
4	3	0000 0001 0010 s
5	1	0001 11s
5	2	0000 0010 01s
5	3	0000 0000 1001 0s

6	1	0001 01s
6	2	0000 0001 1110 s
7	1	0001 00s
7	2	0000 0001 0101 s
8	1	0000 111s
8	2	0000 0001 0001 s
9	1	0000 101s
9	2	0000 0000 1000 1s
10	1	0010 0111 s
10	2	0000 0000 1000 0s
11	1	0010 0011 s
12	1	0010 0010 s
13	1	0010 0000 s
14	1	0000 0011 10s
15	1	0000 0011 01s
16	1	0000 0010 00s
17	1	0000 0001 1111 s
18	1	0000 0001 1010 s
19	1	0000 0001 1001 s
20	1	0000 0001 0111 s
21	1	0000 0001 0110 s
22	1	0000 0000 1111 1s
23	1	0000 0000 1111 0s
24	1	0000 0000 1110 1s
25	1	0000 0000 1110 0s
26	1	0000 0000 1101 1s
ESCAPE		0000 01

The remaining combinations of (RUN, LEVEL) are encoded with a 20 bit word consisting of 6 bits ESCAPE, 6 bits RUN and 8 bits LEVEL.

RUN is a 6 bit fixed length code

0	0000 00
1	0000 01
2	0000 10
.	.
.	.
63	1111 11

LEVEL is an 8 bit fixed length code

-127	1000 0001	
.	.	
.	.	
-2	1111 1110	
-1	1111 1111	
0	0000 0000	FORBIDDEN
1	0000 0001	
2	0000 0010	
.	.	
127	0111 1111	