CCITT SGXV
Working Party XV/1
Specialists Group on Coding for Visual Telephony

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SOURCE: Bellcore

TITLE: Patent Disclosure

US 4,791,598

Date: Dec 13, 1988

Inventors: M. L. Liou, M. T. Sun, and L. Wu

Two-Dimensional Discrete Cosine Transform Processor - The 2-D processor consists of a 1-D DCT processor, a transposition memory and another 1-D DCT processor. The 1-D DCT processor simultaneously computes an entire row or column of vector inner products by using distributed arithmetic and using decimation-in-frequency to reduce the amount of memory capacity (ROM) required. Partial sums may also be used to further reduce ROM size.

Bellcore Patent Application No. 221 (Allowed by US Trade and Patent Office)
Inventor: H. Gharavi

Method and Apparatus for Low Bit-Rate Interframe Video Coding - In accordance with the present invention, the two-dimensional blocks of $m \times m$ pel data at the input to the hybrid-type of encoder are subdivided, after subtracting the corresponding block data from the previous frame, into smaller sub-blocks of size $n \times n$ ($n < m$). Transformation within the loop of the hybrid coder is then performed on a sub-block basis. After transformation and quantization, the block is reconstructed and the coefficients of the block transmitted to the receiver on a block by block basis, together with the block overhead data. This overhead data includes block classification (static or dynamic block) and the block matching motion estimation of a dynamic block which are both performed on the main block basis.

Bellcore Patent Application No. 258
Inventors: K. M. Yang and L. Wu

Circuit Implementation of Block Matching Algorithm - The invention relates to a VLSI implementation of a block matching algorithm with full search capability for detecting and compensating differences between successive video frames caused by motion.