

C.C.I.T.T.
STUDY GROUP XV WP XV/1
Specialist Group on Picture Coding
Oslo 7-10 March 1989

DOC. # 488

English Version

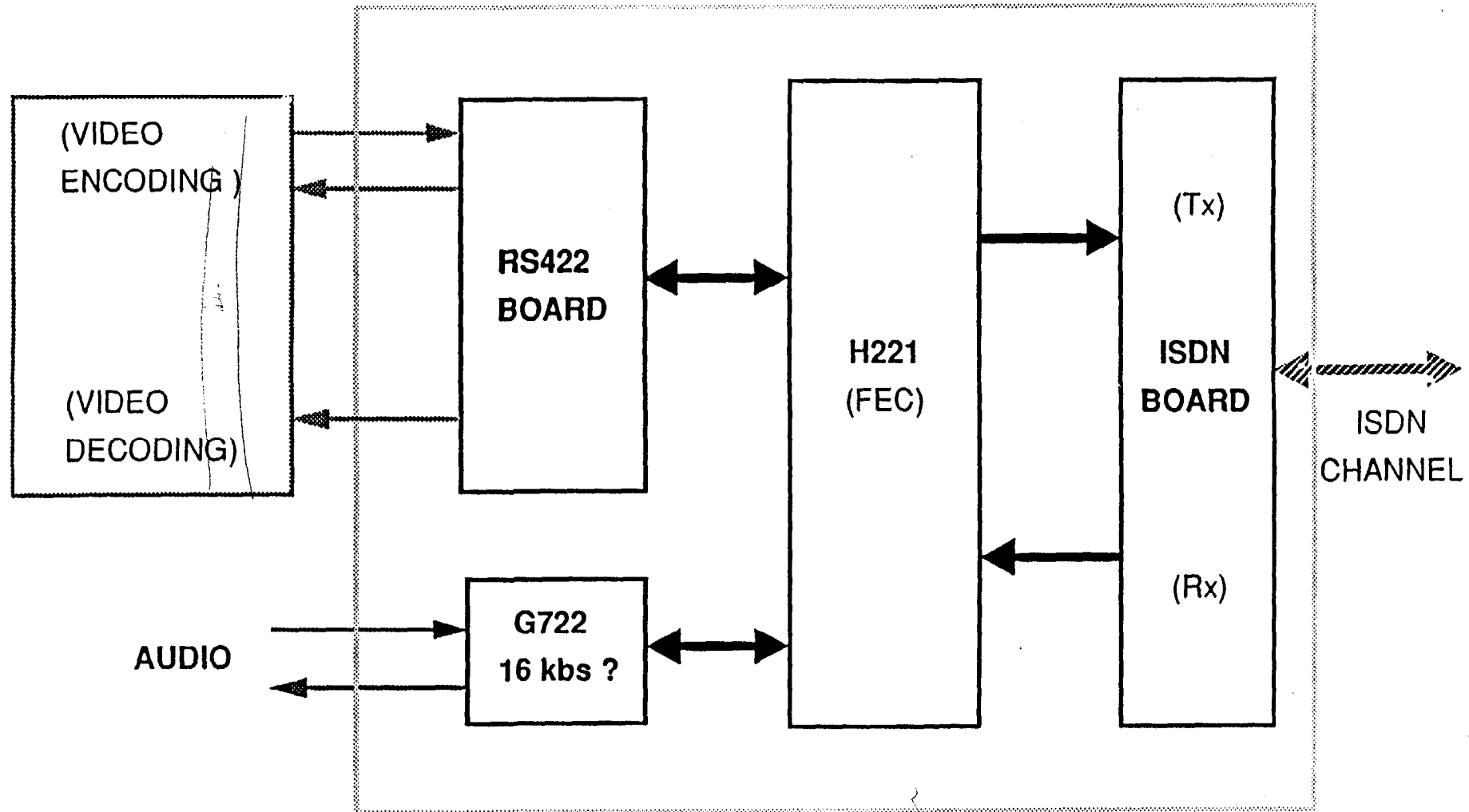
Source: AT&T Bell Laboratories, Bellcore

Title: Flexible Hardware Status and Plans

AT&T and Bellcore are collaborating in an effort to enable USA video codec manufacturers to participate in the Flexible Hardware compatibility tests to be carried out starting September 1989. Basically, we are planning to implement a PC plug-in board system (see attached diagram) that performs audio coding, framing structure, FEC and ISDN interconnectivity. This can then be placed between a video codec and the ISDN channel for inter working with other systems, either local or remote. The current state of this project is also attached.

flexible hardware

PC (80386)



Complete
Circuit Diagram

1. First priority will be QCIF, with full CIF coming later.
2. Interface to the video codec will be via RS449 under control of the PC. RS449 data clock will be substantially higher than the channel clock to enable packetized transfer to/from the PC with minimal delay. Clear-to-send can be used for data flow control.
3. Most of the data buffering occurs inside the codec. The codec is fast enough to guarantee that data is always present in its coder buffer, and that space is always available in its decoder buffer.
4. What should the RS449 packet size be? Perhaps it should be the same as the FEC packet size (128 octets). How is startup achieved?
5. Video data RS449 PC interface will be provided by AT&T. Several commercially available (25 pin plug) boards are being examined. RS449 data rates up to 1Mbps are feasible. What is the RS449 packet sync, and what data appears between RS449 packets?
6. FEC on the video data will be implemented in the PC, tentatively by AT&T. A USA paper to CCITT will argue for RS-FEC. We may have to give everyone RS software. We may have to implement someone else's BCH software. RS-FEC packet size is 128 octets. How is sync reestablished after a catastrophic error burst? There is no sync between PSC and FEC, or between H.221 and FEC. AT&T will provide information on channel bit-error characteristics. FEC can be switched off for testing.
7. H.221 (H.222?) will be implemented by Bellcore in the C-language to facilitate portability between DSP's. It will handle audio as well as video data. Other data capabilities to be negotiated. One FAS-code per B-channel will be needed.
8. Is D-channel capability required? Call setup? Other control? Initially, manual setup and start should be sufficient. Later, automatic features will be implemented.
9. Audio interface will be analog. Audio to be coded initially at 64kbs via G722. Audio delay will be matched to video by Bellcore during the H.221 multiplexing. 16kbs audio will come later, perhaps using AT&T's submission to CCITT.
10. First priority is for video coding at 63.2kbs ($p=2$), including FEC. Later, video will be coded at 46.4 and 109.6 kbs, including FEC overhead and assuming availability of 16kbs audio. Still later, 56kbs and $p=6$ will be considered. See G725 and zero-byte replacement.
11. Minimum ones density may be required for North American trials. Can this be done in the PC? Will we have time before September? Ditto for scrambling.
12. ISDN interface will be provided by AT&T. First priority is for $p=2$, Basic Rate Interface (BRI). Primary rate Interface (PRI) will come later. A few commercially available boards are being examined.
13. Data channels will be available from New Jersey to other CCITT participants in Japan (KDD) and the U.K. (BTI). AT&T is looking into connectivity to other places.