CCITT SGXV
Specialists Group on
Coding for Visual Telephony

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Magnusson

Source: AEG, BT, France, IMAGIN project, PKI

Title: Hardware status and plans

This contribution outlines the work in Europe aimed at providing hardware to verify the p*64 kbit/s recommendation.

AEG Aktiengesellschaft May

AEG has developed prototypes of 2*64 kbit/s ISDN video-telephones and delivered four items to the German PTT at the end of last year. The codecs are working with motion compensation and 16*16 DCT. The hardware is fully programmable and uses two MC68020 CPUs and sixteen (2*8) ADSP2100A DSPs from Analog Devices. At the moment AEG is developing new software according to the flexible hardware specification which will be the basis for the future H.261 recommendation. It is hoped that this software will be running in summer 1989.

The subsidiary company AEG OLYMPIA has meanwhile started the development of a new hardware with reduced size and cost compared to the above mentioned prototypes. The new codec will be able to code or decode CIF and QCIF pictures at ISDN data rates (p = 1, 2; 32-128 kbit/s).

British Telecom Can

BT intends to have fully functional flexible hardware for the encoder ready for field trials by the end of September 1989. This assumes that all major parts of the px64 kbit/s flexible hardware specification are fixed at the Oslo meeting in March. The decoder hardware will be complete by mid-October. The codec will be capable of operating at full CIF and Quarter-CIF with all values of p.

France (CNET, SAT and ALCATEL-CIT) Guicha

France now has a hardware codec able to transmit and receive moving pictures (Full and Quarter-CIF) at 64 kbit/s. The coding algorithm is RM5 based.

This codec has been implemented by SAT and ALCATEL-CIT under a FRANCE TELECOM contract (CNET) in order to test the effectiveness of the algorithm supported by the European countries and studied by CCITT.

The main characteristics of the codec are the following:

- Full and Quarter-CIF working
- Maximum Picture rate 10 Hz
- Macro-block structure (RM5 based)
- Video multiplex very close to the existing specification for p*64 kbits flexible hardware

As for the previous 384 kbit/s codecs, most of the items have been left fully programmable, allowing further optimisations of the coding scheme.

In principle, the organisation of the video multiplex can be modified to meet the final specification.

Up to now the transmission rate is limited to 48 and 64 kbit/s.

A video tape has been recorded showing:

- A videotelephone scene at 64 kbit/s FULL CIF
- A test signal generator sequence (CLAIRE) decoded by the codec
- TV and videotelephone scenes at 64 kbit/s QCIF

IMAGIN Brusmitz

The so-called IMAGIN project is a cooperation between five European administrations (FI/DBP, CSELT, CNET, PTT-RNL, STA) to develop a videophone terminal for ISDN.

One important task in the project is to develop a joint video codec prototype, which is as much as possible in line with with the p*64 kbit/s CCITT Recommendation H.261.

In IMAGIN we think that the Specialists Group is a suitable body for cooperation.

Especially, we want to express our willingness to participate in any compatibility check (or other) field trials which may be organised in the future.

Philips Kommunication Industrie AG Spiedel

PKI developed for a special customer a 64 kbit/s video codec derived from the flexible hardware by simplifying the video multiplex and including a macro-block scheme as in RM4. This codec has the capability to work at bit rates between 48 kbit/s and 2 Mbit/s with a maximum of 30 frames/s. Pictures recorded from this hardware will be shown at the Oslo meeting.

Operation with the new macroblock structure is not possible for the encoder. The decoder is based on the use of two high speed processors and is therefore adaptable to the new block structure and multiplex scheme. The filter is a hardware implementation with the fixed coefficients 1/4, 1/2, 1/4 and a DCT chip from Telettra was used for the inverse transform. This chip does not meet the specifications derived in the CCITT Specialists Group. With the availability of more suitable DCT chips, PKI is planning to redesign the board containing the filter and the inverse DCT, thus providing a decoder for the field trials in the autumn.

To test the DIS Test Pattern Generator an unmodified decoder hardware can be used yielding some mismatch error but providing a functional test-bed for the new multiplex. PKI itself does not intend to buy a test generator by itself.

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