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CCITT SGXV
Working Party XV/1
Specialists Group on Coding
for Visual Telephony

Doc# 432
December 88
Orlando

Title: Error correction scheme for p x 64kbit/s

Source: UK, FRG, France, Italy, Netherlands, Norway, Sweden

General

Documents previously presented by the UK have identified that a 511,493 BCH code is fairly well suited for error correction of H261 coding schemes when transmitted via G821 data channels. This document considers the problem of framing the error correction code into the complete data multiplex.

Requirements

A video decoder must be able to isolate active data bits from error correction parity information. There are many ways that this function can be achieved. Any proposed scheme should take account of the following requirements:-

1. The error correction block length is 511 bits.

2. The position of the 18 bits of parity information must be easily identified for all bit rates.

3. A common solution should be found for both 2B ISDN access and primary rate access video codecs.

4. The scheme should be highly efficient from a bit rate point of view.

5. The lock-up time to the data/parity phasing should be very fast, at the decoder, after a multipoint switch.

Discussion

Many different schemes have been considered during the preparation of this document. One possibility was to use a self synchronising technique. This method relies on locating the parity information at the decoder by trying sequential positions until a location occurs where sensible parity results are obtained. The method works very well for fixed point to point connections. Unfortunately, in the case of switched multipoint at 64kbit/s, the time to find the correction bits can be several seconds and this makes the method unsuitable.

Another scheme also considered employed the H221 framing as a basis for the parity code positioning. There are many

disadvantages of this scheme. The main difficulty is that the number of active bits between H221 framing bits changes with bit rate and yet the block length of the error correction scheme must be fixed at 511 bits. Another problem is that parity bits must never be inserted in the audio or framing bits.

Proposal

Provide a simple framing structure for the video data only.

For example the following arrangement could be used:-

[11100100 Framing word] [8 blocks of 511 {=493data+18parity}] [11100100 ....etc

Advantages:

1. Error correction is only applied where we need it. Only the video data is error corrected. The audio channel does not need error correction.

2. The error correction scheme is in-band as far as the video is data concerned and is therefore independent of network framing, bit rate etc.

3. Error correction can be applied to 2B ISDN access using one time-slot for audio and one for video even if the network delays for each time-slot cannot be equalised.

4. Multipoint Control Units do not have to deal with error correction. The audio can be mixed and data can be broadcast without the need to recalculate the in-band error correction parity.

5. The lock up time for decoders during switch multipoint is fairly fast.