

Source : JAPAN

Title : Proposal on Forward Error Correction and Buffer Control Scheme

1. Introduction

This document describes an extension of the proposal in Doc. #288 (Tokyo, Jan. 1988) and Doc. #325 (Hague, Mar. 1988) on forward error correction. Framing for the ECC bits transmission is clarified.

A method to cope with buffer underflow at the coder is also proposed, where the above framing for FEC is utilized. This method allows simple buffer control and its operation has been verified in a low bit rate hybrid codec.

In order to secure the decoding operation easily, it is proposed to specify the minimum coded picture interval as well as the maximum coded picture interval.

We propose the following contents would be included in the p×64 kbit/s Flexible Hardware specification as well as in the Final Recommendation.

2. Forward Error Correction

2.1 Error Correcting Code

Double Error Correcting (511,493)BCH.

2.2 Generator Polynomial $g(x)$

$$g(x) = (x^9+x^4+1)(x^9+x^6+x^4+x^3+1)$$

2.3 ECC Bits Transmission

Independent framing is used with multiframe of 8 frames, where a 512-bit frame consists of 1-bit framing, 493-bit data and 18-bit ECC (Error Correcting Code). The frame alignment pattern is $(S_0S_1S_2S_3S_4S_5S_6S_7)=(0001101X)$, where X is a reserved bit for future multiframe use and set to 1. See Fig. 1.

3. Fill Bits Insertion

If required, any of the 493-bit data fields are filled with dummy bits. Fill indicator " F_i " placed at the first bit of the 493-bit data field indicates whether the 492-bit to follow are CODED DATA ($F_i=1$) or FILL ($F_i=0$). See Fig. 1. The ECC is calculated against the 493-bit including Fill Indicator.

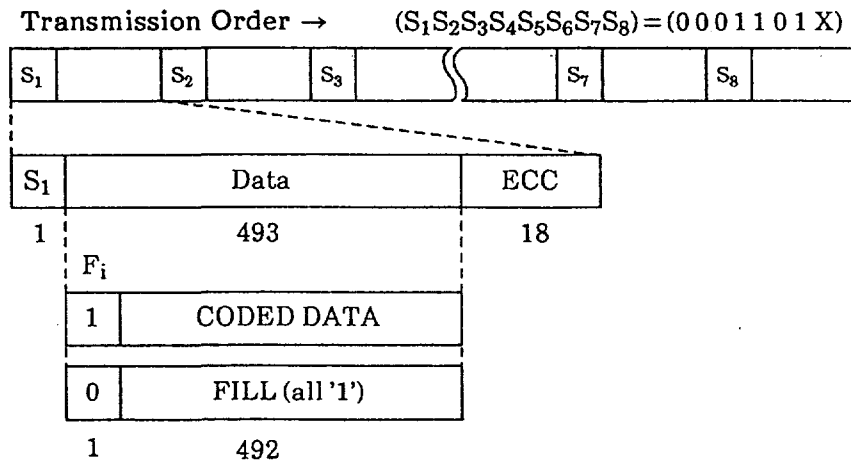


Fig. 1. Error Correcting Frame

4. Buffer Control

In order to secure stable decoder operation in various combinations of different buffer architectures, at least the following two items should be specified at the coder;

- Minimum coded picture interval (eg. $1/2/3/4 \times 1/29.97$ sec)
- Maximum coded picture interval (eg. $12 \times 1/29.97$ sec)

Specification to ensure the delay below a certain amount requires further study.

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