CCITT SGXV
Working Party XV/1
Specialists Group on Coding for Visual Telephony

Document #368

September 1988

SOURCE: NTT, KDD, NEC and FUJITSU
TITLE : RELEVANT PATENTS

In the course of CCITT standardization activities, we filed several patents. Out of them, the following two patents are considered relevant to Draft Rec. H.261 or Flexible Hardware Specification. Our patent licensing policy is "to grant non-exclusive licenses on fair and reasonable terms as far as compatibility is concerned if others do so" as stated in Doc. #161.

1. Motion vector control of the loop filter

Title : Motion compensated interframe coding scheme
Number : JP63-121374(A)
Date : May 25, 1988
Application Number: 61-267016 (Nov. 10, 1986)
Content: Interframe coding scheme including a low pass filter which reduces higher frequency components of the local decoder output and a filter control part which determines the low pass filter characteristics according to the motion vector value. (Note: In the detailed description, the loop filter is placed before the frame memory.)
Foreign applications: None

2. Multiple VLCs, last non-zero trick

Title : Encoding system capable of accomplishing a high efficiency by anterior
and/or posterior processing to quantization
Number : JP63-121321(A)
Date : May 25, 1988
Application Number: 61-267339 (Nov. 10, 1986)
Content: 1) Coding scheme where multiple VLC sets for quantization indexes are switched for each pels or group of pels.
2) Use of EOB in that scheme.
3) Different VLCs for the last pel before EOB and other transmitted pels.
4) Use of the same VLC set but different code output vs quantizer index relationships in the method 3).
Foreign applications: US, Canada, EP(DE, FR, GB)

As to implementation methods, the following three patents are considered relevant.

A. Feed-forward coding control using data generation estimation

Title : Image coding system capable of monitoring an amount of information by forming a histogram
Number : JP63-xxxxxx(A)
Date : xxxxxx
(Note: Not yet in the public domain at the time of this document submission.)

Application: 61-267340 (Nov. 10, 1986)
Content: 1) Transform coding scheme including a histogram calculation circuit for the transform coefficient levels and a coding control circuit which gives coding parameter values according to the histogram.
2) Histogram circuit in 1) consisting of two circuits; one for the maximum level for each block, and the other for levels of all the coefficients.
Foreign applications: US, Canada, EP(DE, FR, GB)

B. **Significant/insignificant and intra/inter block decision**

Title : Moving image signal coding system
Number : JP63-121372(A)
Date : May 25, 1988
Application: 61-267367 (Nov. 10, 1986)
Content: 1) Hybrid coding scheme including a prediction error estimator and a threshold circuit.
2) Use of sub-blocks in method 1).
3) Intra/inter mode selection comparing the prediction error estimator output, input signal estimator output and a threshold.
4) Intra/inter mode selection comparing the prediction error estimator output, input signal estimator output and two thresholds.
5) Intra/inter mode selection using sub-block estimation outputs.
6) Use of significant/insignificant block selection for the decision of blocksize for variable blocksize schemes.
7) Combination of 1) and 3).
Foreign applications: US, Canada, EP(DE, FR, GB)

C. **Receiving buffer control**

Title : Decoding device capable of producing a decoded video signal with a reduced delay
Number : JP63-120570(A)
Date : May 24, 1988
Application: 61-265581 (Nov. 10, 1986)
Content: 1) Decoding equipment where decoder is operated/suspended if the receiving buffer content is more/less than a predetermined value at the decoder timing.
2) Use of observed frame numbers at the input and output of the receiving buffer in the scheme 1).
Foreign applications: US, Canada, EP(DE, FR, GB)

END