CCITT SGXV Document #365
Working Party XV/1
Specialists Group on Coding for Visual Telephony September 1988

SOURCE : NTT, KDD, NEC and FUJITSU

TITLE : IDCT MISMATCH EXPERIMENT BY FLEXIBLE HARDWARE

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1. Introduction

To specify the IDCT precision is one of the most signficant problems in the standardization of n*384 video codec. The specification should prevent the visible IDCT mismatch error within the period of cyclic refresh. So we try the hardware experiment to give some border limit to the IDCT precision.

2. Experiment by Flexible Hardware

It is observed how the mismatch error becomes perceptible in the Intra started pictures. The experiment consists of next five parts.

- The first part ; The precision of the transmitter is fixed at 14 bit coefficients, 16 bit truncated transfer , that is the specification of Flexible Hardware. The loop filter is inserted and controlled by MC vector.

- The second part; The precision of the transmitter is fixed at 14 bit coefficients, 16 bit rounded transfer. The loop filter is inserted and controlled by MC vector.

- The third part ; The precision of the transmitter is fixed at 14 bit coefficients, 16 bit rounded transfer. No loop filter is inserted.

- The forth part ; The precision of both transmitter and receiver varied in the rounded transfer. The loop filter is inserted and controlled by MC vector.

- The fifth part ; The precision of both transmitter and receiver varied in the rounded transfer. No loop filter is inserted.

The details of the experiment are described in Annex. The main results of hardware simulations are demonstrated by VCR at the meeting.

3. Conclusion

As the results of our experiment, we conclude as follows;

- The coefficient precision has less influence on visible mismatch error than the transfer precision.

- At the transfer after 1-D IDCT, rounding should be chosen for the reduction of visible mismatch error.

- Supposing 6 second refresh cycle, the transfer precision should be more than 14 bits.

In the truncated transfer, the mismatch error of vertical stripe and DCT basis pattern becomes very annoying in the short term. To refer the fact to Fig.3 in Doc. #364, overall or maximum mean error seems to be very important to prevent the visible mismatch error on the first stage. The specification in Annex 3/ Doc.#346R is considered to be reasonable, according to the expriment results at present. The neccesary precision in fast algorithms is for further study.

Annex

1. Conditions of the Experiment

Considering the coding status at 1.5Mbps, we strictly adopt the conditions as follows;

- Quantizer step size is fixed at 4,
- Source coder / decoder loop back,
- All frames are coded,
- No cyclic refresh,
- Intra mode start.

2. Hardware Simulations

The experiment consists of next five parts.
And three kinds of mismatch error patterns are observed.
(a:vertical stripe,b:granular noise,c:DCT basis pattern)

1) The IDCT of the transmitter has 14bit coefficients, 16bit truncated transfer, as is the specification of Frexible Hardware.
The precision of the receiver's IDCT is changed sequence by sequence.
The loop filter is inserted and controlled by MC vector.

SEQ.	COEFFICIENT PRECISION(bit)	TRANSFER PRECISION(bit)	MISMATCH UNVISIBLE TERM(second)	MISMATCH ERROR PATTERN
1	14	16,truncate	(NO MISMATCH)	—
2	16	12,truncate	1	a
3	12	12,truncate	1	a
4	8	12,truncate	1	a
5	16	12,round	4	b
6	12	12,round	4	b
7	8	12,round	4	b
8	16	14,truncate	4	a
9	12	14,truncate	4	a
10	8	14,truncate	4	a
11	16	14,round	8	b
12	12	14,round	8	b
13	8	14,round	8	b + a
14	16	16,truncate	—	—
15	12	16,truncate	—	—
16	8	16,truncate	15	b
17	16	16,round	9	b
18	12	16,round	9	b
19	8	16,round	9	b
20	8	12,round	(COLOR BAR)	

2) The IDCT of the transmitter has 14bit coefficients, 16bit rounded transfer.
The precision of the receiver's IDCT is changed sequence by sequence.
The loop filter is inserted, and controlled by MC vector.

SEQ.	COEFFICIENT PRECISION(bit)	TRANSFER PRECISION(bit)	MISMATCH UNVISIBLE TERM(second)	MISMATCH ERROR PATTERN
1	14	16,round	(NO MISMATCH)	—
2	16	12,truncate	1	c + a
3	12	12,truncate	1	c + a
4	8	12,truncate	1	c + a
5	16	12,round	6	b
6	12	12,round	6	b
7	8	12,round	6	b
8	16	14,truncate	1	a + c
9	12	14,truncate	1	a + c
10	8	14,truncate	1	a
11	16	14,round	20	b
12	12	14,round	20	b
13	8	14,round	20	b
14	16	16,truncate	1	c
15	12	16,truncate	1	c
16	8	16,truncate	6	a
17	16	16,round	—	—
18	12	16,round	—	—
19	8	16,round	—	—

3) The IDCT of the transmitter has 14bit coefficients, 16bit rounded transfer.
The precision of the receiver's IDCT is changed sequence by sequence.
No loop filter is inserted.

SEQ.	COEFFICIENT PRECISION(bit)	TRANSFER PRECISION(bit)	MISMATCH UNVISIBLE TERM(second)	MISMATCH ERROR PATTERN
1	14	16,round	(NO MISMATCH)	—
2	16	12,truncate	1	a + c
3	12	12,truncate	1	a + c
4	8	12,truncate	1	a + c
5	16	12,round	3	b
6	12	12,round	3	b
7	8	12,round	3	b
8	16	14,truncate	1	c + a
9	12	14,truncate	1	a + c
10	8	14,truncate	1	a
11	16	14,round	13	b
12	12	14,round	10	b
13	8	14,round	8	b
14	16	16,truncate	1	c + a
15	12	16,truncate	1	c + a
16	8	16,truncate	6	a
17	16	16,round	—	—
18	12	16,round	—	—
19	8	16,round	—	—

4) The IDCT of both the transmitter and the receiver has rounded transfer.
The precision of the receiver's is transmitter's IDCT is changed sequence by sequence.
The loop filter is inserted and controlled by MC vector.

	SEND		RECEIVE			
SEQ.	COEFFICIENT PRECISION (bit)	TRANSFER PRECISION (bit)	COEFFICIENT PRECISION (bit)	TRANSFER PRECISION (bit)	MISMATCH UNVISIBLE TERM (second)	MISMATCH ERROR PATTEN
1	16	12	16	12	(NO MISMATCH)	—
2	16	14	16	12	6	b
3	16	16	16	12	6	b
4	16	12	16	14	6	b
5	16	14	16	14	(NO MISMATCH)	—
6	16	16	16	14	9	b
7	16	12	16	16	4	b
8	16	14	16	16	7	b
9	16	16	16	16	(NO MISMATCH)	—
10	8	12	8	12	(NO MISMATCH)	—
11	8	14	8	12	6	b
12	8	16	8	12	4	b
13	8	12	8	14	6	b
14	8	14	8	14	(NO MISMATCH)	—
15	8	16	8	14	9	b
16	8	12	8	16	4	b
17	8	14	8	16	7	b
18	8	16	8	16	(NO MISMATCH)	—

5) The IDCT of both the transmitter and the receiver has rounded transfer.
The precision of the receiver's is transmitter's IDCT is changed sequence by sequence.
No loop filter is inserted.

	SEND		RECEIVE			
SEQ.	COEFFICIENT PRECISION (bit)	TRANSFER PRECISION (bit)	COEFFICIENT PRECISION (bit)	TRANSFER PRECISION (bit)	MISMATCH UNVISIBLE TERM (second)	MISMATCH ERROR PATTEN
1	16	12	16	12	(NO MISMATCH)	—
2	16	14	16	12	4	b
3	16	16	16	12	4	b
4	16	12	16	14	4	b
5	16	14	16	14	(NO MISMATCH)	—
6	16	16	16	14	7	b
7	16	12	16	16	3	b
8	16	14	16	16	6	b
9	16	16	16	16	(NO MISMATCH)	—
10	8	12	8	12	(NO MISMATCH)	—
11	8	14	8	12	3	b
12	8	16	8	12	2	b
13	8	12	8	14	4	b
14	8	14	8	14	(NO MISMATCH)	—
15	8	16	8	14	6	b
16	8	12	8	16	3	b
17	8	14	8	16	6	b
18	8	16	8	16	(NO MISMATCH)	—

VCR Demonstration

SEQ.	Number in Annex/DOC.#365
1	5) — 1
2	5) — 2
3	5) — 3
4	5) — 4
5	5) — 5
6	5) — 6
7	5) — 7
8	5) — 8
9	5) — 9
10	5) — 10
11	5) — 11
12	5) — 12
13	5) — 13
14	5) — 14
15	5) — 15
16	5) — 16
17	5) — 17
18	5) — 18
19	1) — 2
20	2) — 14
21	1) — 20
22	1.5 Mbit/s No mismatch.
23	1.5 Mbit/s. F: Flex. Hard. R: 12bit Transaction
24	384 kbit/s No mismatch.
25	384 kbit/s F: Flex. Hard R = 12bit Transaction