CCITT SGXV
Working Party XV/1
Specialists Group on Coding for Visual Telephony

Document #349
21 June 1988

SOURCE: Chairman of DCT chip manufacturers meeting (Mike Carr).

TITLE: REPORT OF THE MEETING OF DCT CHIP MANUFACTURERS MARTLESHAM UK 24-25 MAY 1988.

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1. General

The meeting of DCT chip manufacturers was held at Martlesham, Ipswich UK from May 24 to 25, 1988 at the invitation of British Telecom.

The list of participants appears as annex 2 to this report.

2. Documents for the meeting

For this meeting, 15 normal documents and 2 temporary documents were made available. Annex 1 gives an outline of each document.

3. Agenda

1. Description of the IDCT problem and its impact on standards.
2. Detailed presentation of contributions.
3. Demonstration of video codec hardware.
4. Discussion of manufacturers proposals.
5. Conclusions and preparation of work plan.

4. Description of the IDCT problem and its impact on standards (Agenda item 1).

The chairman opened the meeting by giving an overview of the Inverse Discrete Cosine Transform (IDCT) problem. Temporary document No. 1 was presented. The technical details of the problem that arises in interframe codecs when there is IDCT mismatch were outlined. The timescales for introduction of standards by CCITT SG XV were described. The chairman stressed that the basis for the specification of an IDCT chip needed to be agreed by September 1988. This would allow time for performance testing in video codec hardware before final inclusion of the IDCT specification in the standard by accelerated procedure in April 1989.

Information from Mr S Okubo, the chairman of CCITT SG XV/1 Specialists Group, was presented (page 4&5 of Temorary Document No 1). This described the current status of the IDCT specification in CCITT and gave a list of relevant CCITT documents.

Doc #1 entitled "Collection of contributions concerning IDCT from CCITT SGXV" was distributed.

5. Detailed presentation of contributions (Agenda item 2).

The meeting participants gave formal presentations of their DCT chip work. A summary of each document and presentation is included as Annex 2 to this report.

Six companies (Thomson, ATT, INMOS, CCETT, Telettra, ANT) indicated that they were already in the process of making DCT chips. Only two companies designs (INMOS and CCETT) fully meet the IDCT specification distributed by Barry Haskell (Annex 3 to Doc. 346R of CCITT SGXV/1 SPECIALISTS GROUP). Telettra and Thomson had firm plans to make improved versions of their chips which would meet the current IDCT specification.

Most manufacturers indicated that the most difficult parameter to meet in the IDCT specification was the mean squared error requirement of 2%. If the mean squared error requirement could be relaxed to 6% then nearly all of the manufacturers designs could meet the IDCT specification.

J Guichard (CNET) presented Doc #3 and a video tape showing simulation results using RM5 at 64kbit/s on Miss America and Clare. An ideal transform was used at the encoder and a simulation of the Thomson chip at the decoder. Even though the Thomson chip design has a mean squared error performance of 3%, no visible mismatch error could be seen on the video tape demonstration. This supported the manufacturers proposal to relax the mean squared error requirement. J Guichard indicated that he felt the sensitive parameter in the specification was the mean error performance and not the mean squared error performance. Further work was continuing at CNET to confirm this.

It was pointed out that tests on visibility of the mismatch error conducted to date had concentrated on establishing the error at the decoder when used with an ideal transform at the encoder. In practice non ideal transforms will be used at the encoder and decoder and so the mismatch problem may in fact be rather worse than is currently seen in demonstrations. This may result in the current specification being tightened.

6. Demonstration of video codec hardware (Agenda item 3).

This presentation by Mr G Morrison (BTRL) demonstrated the British Telecom flexible codec hardware working at 384kbit/s with IDCT mismatch at the decoder. Mismatch was achieved by using the flexible hardware IDCT at the encoder and an IDCT with 12 bit coefficients (rounded) at the decoder. The inter 1D transform data was also truncated to 12 bits at the decoder during the test. With the codecs systematic update procedure switched off then mismatch could be clearly seen after only 10 to 15 seconds. Mismatch was difficult to see with systematic update switched on.

7. Discussion of manufacturers proposals and plans (Agenda items 4 & 5).

The previous day's demonstrations had clearly indicated that before an IDCT performance specification can be finalised more work needs to undertaken by video coding experts, taking into account combinations of IDCT performance from the various manufacturers. The issue of software models for the various chip designs was discussed with a view to making these available to picture coding experts so that compatibility checks could be undertaken.

All manufacturers stated that software models of their chip design could be made available if required. The following list was compiled giving the computers and languages used by the manufacturers:-

Thomson:	Fortran 77 ,	VAX
INMOS:	C,	IBM/PC
Toshiba:	Fortran,	General purpose computer.
Fujisu	Fortran,	General purpose computer.
CCETT	Pascal,	VAX
ANT	Fortran,	VAX
ATT	Fortran,C,	General purpose computer & PC
Teletra	Fortran	VAX

Difficulties concerning the transportability of the simulation code were discussed. Also, it was pointed out that picture coding simulation experts have not generally designed decoders in their software. Mismatch experiments were not immediately possible in some laboratories.

Discussion in the meeting had concentrated on the performance of the IDCT in respect of the mismatch problem. It is clear that the requirements of picture coding (without mismatch) are significantly less stringent than the performance requirement due to mismatch. If chip manufacturers could agree on one achitecture, mismatch could be reduced to zero and the complexity of chip could be significantly reduced. The chairman put this view forward to the meeting and he proposed that the chip manufacturers should collaborate and agree on single architecture for the DCT chip. This proposal generated a great deal of lively discussion. Manufacturers were in general opposed to this idea. Many views were expressed. The main points made were as follows:-

1. Differing chip manufacturers have expertise with different architectures. Fixing on one architecture would prevent some manufacturers from exploiting their existing investment in design.

2. Fixing on one architecture may prevent manufacturers from making improved DCT chip designs (eg. to meet still picture transmission requirements) which are also fully compliant with the CCITT nx384kbit/s recommendation. The CCITT design would then be very application specific (ie useful for CCITT codecs only) and this would increase the cost of the chip because the market size would be smaller.

The meeting was therefore in strong support of defining a test specification rather than a single architecture. The final 30 minutes of the meeting was used to discuss the current test specification (Annex 3 to Doc. 346R of CCITT SGXV/1 SPECIALISTS GROUP) with a view to making suggestions for improving the test procedure. Comments from several manufacturers were concerned with the generation of the random data to be used in the test procedure. The current specification merely states that a number of test blocks of random data should be generated. It does not state how this data should be done. It was also pointed out that random data was unlikely to generate sequences of critical test patterns. The test data should at least include:-

i. Arrays of 64 pels having all odd or all even data.

ii. Arrays of 64 pels having only one non zero value.

Inmos made the point that 32-bit floating point accuracy for calculation of the reference data was probably not accurate enough. Mr Morrison stated that simulation of the flexible hardware specification needed 32 bits with integer arithmetic. 64-bit floating point accuracy should therefore be used for the reference data.

In the light of the above comments it was felt that a better test procedure would be for CCITT to prepare a reference test set of data comprising several thousand blocks with known results. The test data could then be guaranteed to contain most of the special critical conditions. The reference test set method would also prevent a situation where manufacturers designs only fail with certain random sequences and thus could be argued to pass or fail the specification depending on who tested the chip.

[END]

ANNEX 1

Meeting of DCT chip manufacturers 24-25 May 1988 Martlesham

Summary of documents and presentations 24 May 1988

Name: M D Carr (chairman)
Company: British Telecom
Document: Doc #1
Summary: Collection of DCT related CCITT contributions.
Conclusions: No specific conclusion.

Name: M D Carr (on behalf of NTT)
Company: NTT
Document: Doc #2
Summary: Examines the effect of truncation and rounding of matrix multiplication IDCT.
Conclusions: One bit increase in M or N halves the mean squared error. The overall mean squared error is equal to the average number of errored pels. To meet current performance spec requires (M>12 and N>14) or (M>13 and N>13) when using truncation. Truncation gives worse results than rounding. When using rounding, the mean squared error specification is most difficult parameter to meet.

Name: J Guichard
Company: CNET
Document: Doc #3 + video tape
Summary: Examines IDCT error when using RM5 at 64kbit/s and the Thomson chip in the decoder.
Conclusions: There is no visible mismatch error when using the Thompson chip at the decoder (Miss America and Clare sequences). This is true even though the current Thomson chip design does not meet the current performance specification in respect of mean squared error. Suggests that mean squared error requirement could be relaxed.

Name: S Kritter
Company: SGS-Thomson
Document: Doc #4
Summary: Desription of the Thomson chip and performance.
Conclusions: Propose mean squared error performance should be relaxed. Current chip design available June 88. New version with improved performance available mid 89.

Name: C Smith
Company: INMOS
Document: Doc #5
Summary: IMOS chip specification.
Conclusions: Meets current performance specification. Available (1st samples) March 89. Tried rounding to evens and simple rounding - gave no difference.

Name: K Ohzeki
Company: Toshiba
Document: Doc #6
Summary: Examins fast DSP implementation of full matrix IDCT. A custom silicon design was also described.
Conclusions: Full matrix design can be implented on two very fast DSP boards (80MIPS).

Name: Y Kosugi
Company: Fujitsu
Document: Doc #7
Summary: Descibes video achitecture based on Fujitsu designed processor.
Conclusions: No specific conclusions for IDCT problem.

Name: JC Carlach
Company: CCETT
Document: Doc #8
Summary: Examines the performance of chip design based on distributed arithmetic and 16 bit accuracy. Also other accuracies are considered.
Conclusions: Current 16 bit design meets the current performance requirements. Chip will be available (samples) at the end of this year. 18 bit accuracy claims to give completely error free performance (ie no mismatch at all). Could produce 18 bit design by the end of the year.

Name: S Cucchi
Company: Telettra
Document: Doc #9
Summary: Performance of the Telettra DCT chip.
Conclusions: Simplified DCT design can be achieved but mismatch with other IDCT chips will be a problem. Have working chip now, but this does not meet current CCITT performance requirement. Will be making a new chip with improved performance available next year. This will meet the current CCITT requirements.

Name: W Jaenicke
Company: ANT
Document: Doc #10 to be distributed.
Summary: Outline of ANT chip spec.
Conclusions: This chip was designed for still picture applications and is on practical field trial at the present time. Current chip does not meet the current CCITT spec because of the tight mean squared error requirement. If were relaxed to 6% then all requirements would be met. May not be fast enough for all rates upto 2Mbit/s.

Name: V Shaw
Company: on behalf of ISO
Document: Doc #11.
Summary: Letter from ISO SC2/WG8.
Conclusions: Demands of still picture are more strict than CCITT SGXV. Require specification for IDCT by Feb 1989.

Name: V Shaw
Company: ATT
Document: Doc #12.
Summary: List of IDCT requirements.
Conclusions: No specific conclusions.

Name: V Shaw
Company: ATT
Document: Doc #13.
Summary: Letter to Mr Koga from B Haskell.
Conclusions: No specific conclusions.

Name: V Shaw
Company: ATT
Document: Doc #14.
Summary: Paper from proceedings of IEEE describing ATT DCT chip.
Conclusions: No specific conclusions.

Name: V Shaw
Company: ATT
Document: Doc #15.
Summary: ATT DCT chip specifiaction.
Conclusions: No specific conclusions.

Name: Chairman
Company: BT
Document: Temporary document No1.
Summary: Meeting agenda, notes from chairman of SG XV Specialists Group and CCITT time scales.
Conclusions: No specific conclusions.

Name: Chairman
Company: BT
Document: Temporary document No2.
Summary: Draft summary of documents presented on the first day of the meeting.
Conclusions: No specific conclusions.

ANNEX 2- List of participants

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