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C.C.I.T.T.
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Title: Progress on Inverse DCT Accuracy Specifications

This document contains copies of correspondence between parties interested in chip manufacture, algorithm simulation and flexible hardware experimentation.

From:
CCITT SGXV
Working Party XV/1
Specialists Group on Coding
for Visual Telephony

January, 1988

To: Respondents on Designs for DCT Chips

Thank you for your submissions and revisions on DCT and inverse DCT chip design information. We are endeavoring to design our videoconferencing codec and to specify requirements for transforms in such a way that all of your chips will be suitable for this application. However, we cannot at this time guarantee it.

Thus, there are several points that need some further study and clarification. In particular, we would like to run your 8 x 8 inverse DCT (12 bits in, 9 bits out, 2's complement signed) in our video codec computer simulations. Therefore, could you send computer source code that duplicates the digital input-output behavior of your 8 x 8 separable, inverse DCT chip? We would need this within two weeks to meet our very stringent deadlines. Could you send the code via PC floppy, 9-track mag tape or electronic mail to

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Holmdel, NJ 07733
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E-Mail Address: ucbvax!vax135!bgh

He will then distribute the software to those with video codec simulation capability so that we can adjust our codec parameters accordingly. Thank you in advance for your cooperation.

On a related topic...Would you be willing to participate in a standards setting procedure for DCT/IDCT chips for more general application, including till-image data compression, medical imaging, aerial photography, etc. We may be able to organize something through the IEEE Standards Committee. If so, please let Barry Haskell know.

TO: Dr. Barry Haskell
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FROM: David Hein
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DATE: February 19, 1988

Dear Barry:

You will find attached the results of the IDCT mismatch experiment run at 320 Kbps. Also attached is a possible candidate for the test vectors to be used for testing the various IDCT algorithms. Figure 1 shows the coding performance of RM4 as a function of refresh period and mismatch error. The figure gives the results for both 320 Kbps and 768 Kbps. The 768 Kbps results were also given in the CCITT document #281, excluding the N=10 case.

The following conclusions can be drawn from Figure 1:

1. The relative loss in quality is greater for 768 Kbps than it is for 320 Kbps. For the case where N=12, there is a 1.4 dB loss for 768 Kbps, and a 0.3 dB loss for 320 Kbps.

2. The optimum refresh period is shorter for 768 Kbps than for 320 Kbps. When N=12 the optimum refresh period is around 4.5 seconds for 768 Kbps, versus 8 seconds for 320 Kbps.

3. The coding performance is more sensitive to the refresh period for 320 Kbps than it is for 768 Kbps. With a MME=0 and a refresh period of 2 seconds there is a 0.5 dB loss at 768 Kbps versus a 0.9 dB loss at 320 Kbps.

Based on the above conclusions it would seem that the standard could allow for the refresh period to be a function of rate, longer for low rates and shorter for high rates. This probably complicates things a bit too much however. I would be more inclined to retain the requirement that was put forth in document #281. In document #281 the refresh period is defined in terms of actual coded frames instead of absolute time. In a simple implementation the refresh period would be 61 divided by the frame rate. At very high channel rates, such as 1.536 or 1.920 Mbps, the codec will probably run at 30 frames per second, and therefore the refresh period will be 2 seconds. However, at 384 Kbps codecs will probably be operating at 15 frames per second, and have a 4 second refresh period. If the Nx384 algorithm is applied at 64 Kbps, the codec will probably have to operate at 10 frames per second or less. The refresh period would be greater than 6 seconds.

In addition, the proposal in document #281 relaxes the refresh requirement for the uncoded blocks, since these blocks do not contribute to the mismatch error. In theory, a fixed block never requires refresh. In pratice some refresh is required to handle transmission errors. By relaxing the refresh requirements for fixed blocks we have helped the low channel rate even more, since there will be a greater percentage of fixed blocks at low channel rates than at the higher rates.

Taking a second look at the curves in Figure 1, it seems that the refresh requirement could be relaxed to 120 frames, 8 seconds at 15 frames per second, without very much loss in performance. For low MME cases there is actually an increase in performance.

Now on the subject of the IDCT test vectors. Table 1 shows my initial cut at defining the test vectors. As I mentioned over the phone, these were derived by taking a 32x32 window out of one of the frames from the Salesman sequence. The first 16 blocks in Table 1 were generated by breaking the 32x32 image up into 16 blocks, taking the FDCT, and rounding to 12 bits. Blocks 17 to 32 were generated by taking the frame difference of the 32x32 image with the next frame and then producing the 12 bit coefficients as described for the first 16 blocks.

I have generated MME's based on these test vectors and got results similar to those obtained with a random number generator. Therefore, rather than proposing the test vectors in Table 1, I would propose the following method for generating the test vectors.

1. A psuedo-random number generator is used to generate approximately uniformly distributed, uncorrelated 9 bit numbers.

2. The DCT coefficients are produced by performing a forward DCT using a 32 bit floating point implementation.

3. The coefficients are rounded to 12 bits.

Random number generators can be well defined and I would suggest using one based on the linear congruential method, which is defined as:

$$X(n+1) = (A*X(n) + C) \bmod D$$

Values of A=65539, C=0, D=2**32 and X(1)=65539 are used in the well known RANDU function. I have used values of A=21677, C=19117, D=2**15 and X(1)=31415.

If this is acceptable then the problem of defining the MME arises. The MME as defined in document #281 is simply the MSE of the 9 bit results produced by the baseline IDCT and the target IDCT. Two other potential measures could be the maximum absolute error and the mean error.

My feeling at this point is that there should be 5 parameters that are measured. Based on these measurements, the standard could then specify limits on one or more of the measurments. I suggest that the following parameters be measured:

1. The MSE averaged over all pixels.

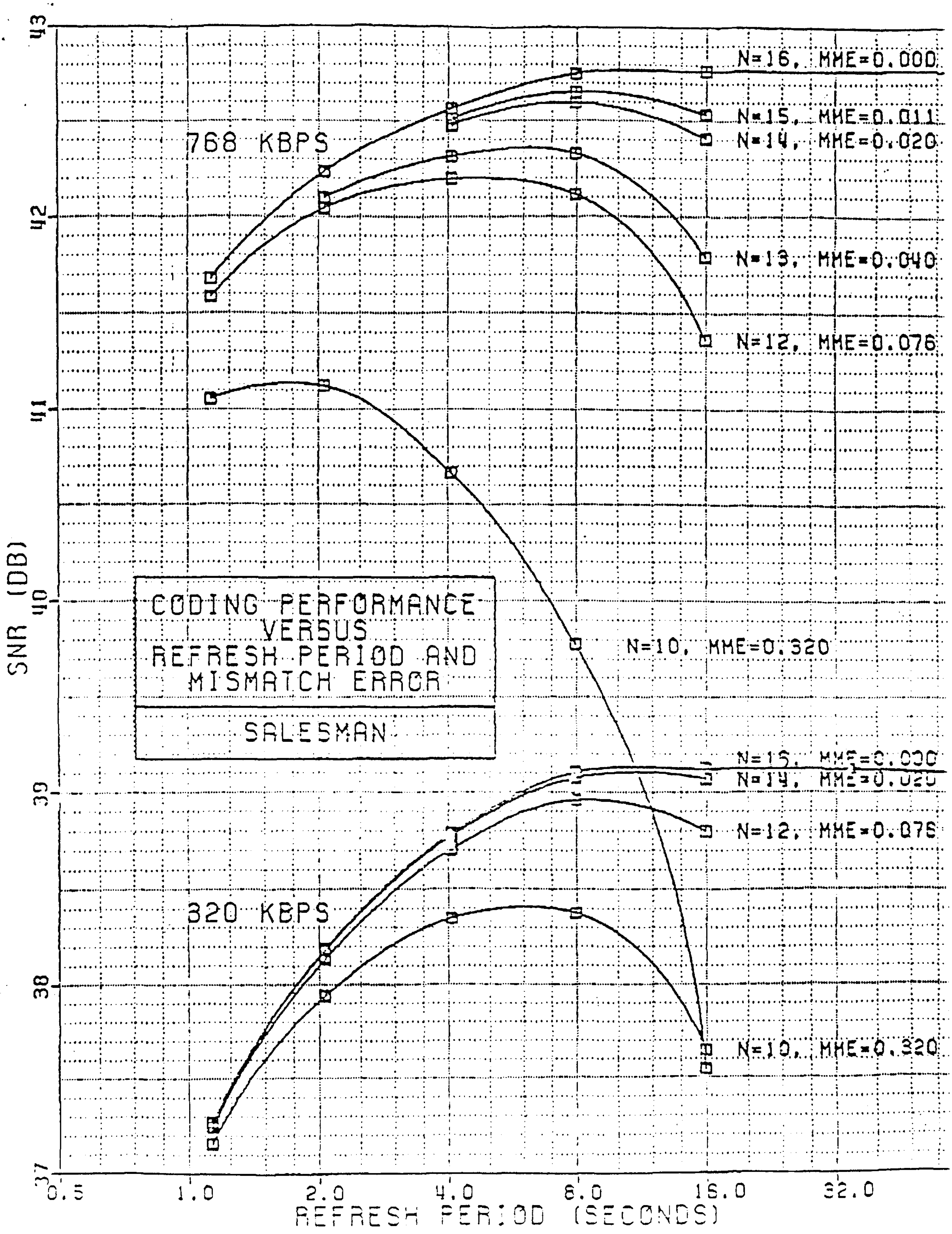
2. The maximum MSE, which is computed by measuring the individual MSEs for each of the 64 pixels, and selecting the largest MSE.

3. The mean error averaged over all the pixels.

4. The maximum mean error, which is computed by measuring the individual means for each of the 64 pixels, and selecting the one with the largest absolute value.

5. The maximum absolute error.

I would suggest using a 32 bit floating-point implementation of the IDCT as the baseline, instead of the one I proposed in document #281.



CODING PERFORMANCE VERSUS REFRESH PERIOD AND MISMATCH ERROR
SALESMAN
768 KBPS
320 KBPS
N=16, MME=0.000
N=15, MME=0.011
N=14, MME=0.020
N=13, MME=0.040
N=12, MME=0.076
N=10, MME=0.320
N=15, MME=0.000
N=14, MME=0.020
N=12, MME=0.076
N=10, MME=0.320
SNR (DB)
43
42
41
40
39
38
37
REFRESH PERIOD (SECONDS)
0.5
1.0
2.0
4.0
8.0
16.0
32.0

Figure 1

	C00	C01					C06	C07	C10	C11						C17
#1	107	00A	008	005	004	004	002	001	001	FFF	000	FFF	FFE	FFE	FFE	FFF
	000	000	000	000	001	001	000	000	001	FFF	000	FFF	000	000	000	000
	FFF	000	000	001	000	001	000	000	000	000	000	001	000	000	000	000
	FFF	000	000	001	FFF	FFF	FFF	001	000	001	000	001	FFF	000	000	000
#2	1D3	F7E	FF0	000	003	FFD	004	FFF	004	000	FFF	001	004	FFC	002	000
	002	FFD	FFD	003	003	003	FFF	003	002	FFD	002	001	FFF	001	000	001
	002	FFF	001	FFE	000	000	FFE	000	FFE	000	001	000	001	000	000	000
	FF8	005	FFF	001	000	003	FFE	007	000	001	000	000	001	000	000	000
#3	309	FD9	FF8	FF5	FFD	FFA	002	FFB	FEF	00E	002	FFF	FFE	FFE	000	FFE
	003	001	FFC	002	FFE	002	000	005	004	FFC	001	003	001	000	FFF	001
	FFD	004	001	FFF	FFF	000	FFE	001	002	000	FFF	000	001	000	001	000
	FF8	002	FFF	002	001	004	000	00B	FFE	001	FFF	000	000	000	001	000
#4	398	FDB	003	FF6	FFB	001	FFF	FFE	FE6	FFE	001	FFB	001	FFD	000	FFE
	FF7	FFD	004	FFF	FFE	001	002	006	004	FFC	002	002	001	002	000	FFF
	001	FFB	FFD	000	000	001	000	000	005	002	FFD	FFF	000	000	000	000
	FF6	005	FFE	003	001	003	000	00B	FFF	002	FFE	000	FFF	000	000	000
#5	172	04B	007	FF6	FFE	FF9	004	FFD	F9E	FD6	010	011	004	00D	001	004
	000	FE0	FE6	002	009	FFA	FFD	FFD	010	01D	007	FF3	FF5	006	006	002
	015	00B	00A	00A	002	FF6	FFD	FFE	FE7	FF0	FFA	FFF	003	006	000	001
	009	001	001	FFF	FFF	FFD	001	FFC	001	004	000	FFF	FFE	003	000	004
#6	213	FE5	FD9	FE5	FF3	FFD	001	FFD	FF5	FBB	FFC	FFC	006	002	000	004
	FFC	FEE	011	003	008	001	000	000	FF1	00F	FF6	008	004	FFD	001	FFD
	004	FFE	002	005	FFD	000	001	FFC	FFC	FFD	001	FFD	002	FFF	000	FFF
	004	FFD	000	002	000	000	002	FFC	FF9	002	002	000	000	000	FFF	005
#7	150	FF8	023	FEC	007	005	006	FFF	045	02C	FEA	01D	FF7	FFA	FFC	001
	084	FDA	008	FE5	006	002	001	001	FFB	FF0	[illegible]	007	FF0	FFD	FFF	FFC
	01E	FF3	FF7	FF8	003	FFE	000	FFD	FFD	001	002	FFF	003	FFF	001	FFF
	018	FFC	FFC	000	FFD	FFF	000	FFC	003	FFE	001	000	002	000	001	004
#8	274	F7A	030	002	FFB	FFD	008	005	03A	012	FD5	000	003	FFD	FFF	FFE
	073	02C	009	FFA	001	001	001	001	006	003	FFF	002	FFD	FFF	FFF	FFE
	010	004	006	FFD	003	000	000	FFB	009	FFF	FFA	000	FFF	FFF	001	FFE
	00E	005	001	FFF	002	FFE	000	FFC	005	006	002	003	FFE	002	FFF	007
#9	24C	00E	FF3	008	FFE	FEF	00F	004	001	022	00C	FFD	001	FF8	FFA	FFA
	014	00B	FE2	FFC	00F	FF4	FF5	FFD	FD4	FFA	00C	00C	002	FF8	FFC	000
	FFD	009	005	FFF	FFC	FFA	000	FFA	FFE	FFC	FF5	000	001	000	FFF	002
	00B	001	FF9	FFE	001	FFE	000	FFC	FFF	FFE	002	FFE	FFE	FFE	001	FF0
#10	[illegible]	[illegible]	[illegible]	FFF	FFE	FFE	001	FFF	FD7	024	000	FF8	FFF	FFF	000	000
	FE5	014	001	FFD	FFD	002	001	FFE	[illegible]	[illegible]	[illegible]	[illegible]	FFC	000	[illegible]	[illegible]
	FFB	002	001	000	FFC	001	000	FFB	FFA	002	000	001	FFF	001	FFF	003
	005	FFF	001	FFE	FFF	000	FFF	FFB	007	FFD	000	000	000	FFD	000	FF0
#11	34D	FF6	00E	FFC	002	004	FFF	003	FBB	FE4	012	FF3	006	005	FFF	000
	FF0	FDF	008	FF3	003	002	003	FFF	FFE	FE4	FFF	FF2	001	006	002	004
	FFE	FF3	001	FF1	002	FFF	003	FFB	FF1	004	005	FF7	001	002	000	003
	FF8	006	004	FFB	002	FFE	000	FFC	FFF	004	001	FFA	001	FFD	000	FFB

Table 1 IDCT Test Vectors

#12	320	FC5	063	FED	FFD	006	002	FFD	FDB	002	002	FF2	006	006	FFA	002
	001	FF2	00D	007	009	FFC	002	002	000	FFE	007	002	FFE	FFD	007	001
	FFE	000	004	005	002	003	000	FFD	FF8	FFF	000	001	FFD	FFF	002	003
	001	FFC	001	002	FFF	FFF	001	FFC	003	FFF	000	FFF	FFF	FFE	001	FFA
#13	27B	01B	FE4	FF3	004	FE9	FFE	00A	FF3	FF7	012	019	006	FFC	00B	002
	FF5	FF8	FFA	FFF	FFD	FFC	FFF	006	010	00A	004	005	004	005	FFF	FFF
	00C	000	FF2	FF7	003	003	000	000	005	002	FFB	FFC	FFF	000	FFF	001
	FF3	002	004	002	FFD	002	FFD	008	FFC	FFF	FFF	FFF	FFF	000	001	001
#14	296	FCA	015	FF7	000	000	001	000	017	FE9	000	005	000	004	FFF	000
	007	FFA	FFD	005	000	003	FFE	003	006	FFD	001	000	FFF	000	001	000
	003	FFE	002	001	FFF	000	000	000	000	002	FFF	000	FFF	FFF	000	000
	FF5	002	FFF	002	000	003	FFF	009	FFF	000	001	000	000	000	FFF	000
#15	354	001	FE9	006	FF4	001	FFF	000	025	FFB	00D	FFC	007	FFE	FFF	FFF
	FF7	000	002	001	FFE	FFF	002	006	004	FFE	003	000	002	001	FFF	000
	002	001	FFF	FFF	001	000	000	FFF	FFF	FFF	FFF	000	000	FFF	000	000
	FF6	002	000	004	000	003	000	00A	001	FFF	000	000	000	FFF	000	001
#16	32B	F7C	02E	010	002	013	FEC	00B	009	016	018	001	FFD	006	007	004
	FEF	00C	007	001	FFC	FFB	008	FFF	00D	FFD	FFF	002	001	004	FFC	001
	FF9	005	FFE	FFF	002	FFF	001	FFF	003	FFE	000	FFF	000	000	000	FFF
	FF8	001	000	002	000	005	FFF	00A	FFF	000	002	000	000	FFF	001	FFF
#17	000	FFF	000	001	002	001	001	000	FFE	FFF	FFF	001	000	FFF	FFF	FFE
	000	000	FFE	FFF	000	000	000	FFF	002	001	FFF	FFF	FFF	001	FFF	001
	FFF	FFF	001	002	000	001	000	000	000	001	000	001	000	000	000	000
	001	001	000	000	FFF	FFF	FFF	001	000	001	000	001	FFF	000	000	000
#18	012	000	FF9	FFF	FFF	FFD	001	000	00F	FFB	FF9	FFE	008	FFB	004	000
	FFC	FFA	005	003	000	025	FFD	001	007	FFE	000	FFE	FFF	001	FFE	000
	004	020	001	FFE	000	000	FFE	001	FFD	000	003	FFF	001	000	000	000
	FFF	001	FFE	000	001	000	002	000	FFE	000	001	001	001	000	000	000
#19	017	FFE	004	FFF	002	FFE	002	FFD	FE4	01C	008	000	FFE	FFC	002	FFC
	022	FE6	FFC	004	FFF	001	FFF	000	FF2	005	007	003	FFF	FFE	FFF	FFF
	003	003	FFE	FFE	FFE	000	FFE	002	FFC	002	FFF	000	001	000	001	000
	004	001	FFE	FFF	001	001	000	000	FFE	000	FFF	001	000	000	000	000
#20	010	000	004	FFB	FFC	[illegible]	001	[illegible]	FE0	FF4	[illegible]	FFB	FFF	FFF	001	FFA
	023	001	007	FFD	000	000	001	003	FF1	FF6	004	004	000	001	000	FFF
	008	FFB	FFB	001	000	000	000	000	002	FFE	FFD	FFE	001	001	000	000
	001	005	FFD	000	000	000	001	000	FFF	001	FFE	FFF	FFF	002	000	FFF
#21	FCF	FFE	00D	FFF	006	006	002	003	0CE	FE3	FF6	00E	002	FFC	FFE	FFC
	002	004	FE1	FEC	003	007	001	FFE	027	02D	022	FFC	FEE	003	004	003
	004	003	008	015	006	FF2	FFB	000	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	000	001
	00E	007	000	000	FFD	FFC	001	000	00B	00C	003	FFB	FFB	001	001	FFF
#22	FE9	FFC	005	004	FFD	001	002	003	01A	FD8	015	FFF	000	00C	000	001
	FE0	010	000	002	000	FFD	FFC	FFF	000	010	FEF	010	FFE	FFF	000	FFF
	FFD	003	002	001	FFA	004	FFE	001	000	000	001	FFC	001	FFC	FFF	001
	FFE	004	FFF	004	FFF	002	001	000	FFD	001	FFE	000	003	000	000	FFF

Table 1 (continued)

	FFE	FFC	FFC	001	FEB	003	004	001	0C1	FF7	FF4	008	007	FF9	FFE	000
#23	025	FC6	010	FDA	014	006	001	003	FF9	003	FEF	016	FE3	000	FFA	FFD
	005	FE8	FEE	FF2	00A	000	004	000	FED	00E	006	004	004	FFE	001	FFE
	021	FEA	FFD	FFE	FFB	003	FFE	FFF	FF4	009	FFF	FFF	003	FFE	000	000
	027	FCC	FD7	00E	FEA	FF1	FFA	009	0AB	058	FED	FF3	013	FFE	003	FFE
#24	051	027	023	FFF	002	00F	007	002	FE5	FF3	FF1	FFB	FFA	FF9	FFB	002
	FFF	005	00F	FFF	006	004	001	FFF	001	FFD	FF8	FFF	FFF	000	000	000
	00D	009	003	001	003	001	001	000	000	FFF	003	000	FFE	001	000	001
	FF6	00C	000	FFB	00C	FF5	FF7	001	00B	00B	FF1	001	009	FF4	FFD	000
#25	FED	FFB	FF7	006	00A	FFC	FFC	FFE	FC4	FFE	02A	00E	FFA	FFC	001	FFF
	008	004	FF2	FF8	FFE	001	003	001	00E	FFD	FF1	002	004	001	002	000
	00D	001	FF2	FFA	001	004	002	001	FFE	002	001	FFD	FFF	003	001	000
	000	00E	FF6	003	000	FFF	003	001	FD0	021	005	FF9	001	002	FFE	002
#26	FF2	007	000	FFF	FFA	003	000	000	FF3	009	FFF	002	FFA	000	002	000
	FFD	FFD	003	002	FF9	003	FFE	001	FFE	001	FFF	000	001	001	001	000
	004	FFD	001	FFF	FFE	001	FFF	001	001	FFE	001	001	FFF	FFF	FFF	000
	FD6	FF0	00C	FFD	009	007	001	006	FD5	FD4	009	FF2	003	006	001	002
#27	00C	FD9	002	FF3	004	004	005	001	00E	FDC	FF9	FF0	005	006	003	002
	006	FF2	FFD	FF1	000	001	003	000	FFA	003	001	FF4	001	003	000	001
	FF8	00A	003	FF6	002	000	000	000	FF8	006	003	FFA	001	FFF	000	002
	FFF	FD3	00D	00F	FEF	00A	002	FFF	FEB	FF4	014	000	003	003	000	FFE
#28	012	FFB	00F	005	FFF	003	000	001	008	FFA	008	000	000	004	006	001
	FF3	007	006	008	004	005	FFE	002	FFB	FFC	001	002	FFB	FFD	003	001
	FFC	FFF	000	002	FFD	001	001	002	FF9	001	FFF	002	001	000	001	001
	009	00B	009	003	001	FFD	FFB	004	FF1	FE9	FEF	FFD	011	003	004	002
#29	015	012	000	001	FF9	FF9	FFC	003	008	FFD	FF5	FFE	00D	00B	FFD	FFE
	010	FFF	FE8	FEE	FFF	001	000	001	000	001	001	FFF	FFD	000	FFF	000
	FF7	FFE	009	002	FFC	000	000	002	FFA	002	004	000	FFD	FFE	000	000
	015	FEC	006	005	FFC	004	FFE	001	013	FEB	FFC	005	FFF	005	FFE	FFF
#30	005	000	FFB	002	FFC	002	000	001	005	FFD	002	000	FFD	FFF	001	FFF
	002	FFE	002	001	000	000	000	000	FFE	001	FFF	FFF	FFF	000	000	000
	FFF	FFF	FFF	000	000	000	000	000	FFE	FFF	000	000	000	001	FFF	001
	010	012	000	008	000	FFD	001	000	004	004	007	FFD	002	001	000	FFF
#31	FFB	FF6	007	FFD	FFF	FFE	000	001	001	000	002	000	004	FFF	FFF	FFF
	002	003	FFD	FFF	001	000	000	000	000	FFD	FFE	000	001	FFF	000	FFF
	000	001	000	003	FFF	000	000	FFF	000	FFF	FFF	000	FFF	000	001	000
	051	FE3	FDA	00C	FF5	024	FDE	009	FB2	021	019	004	FE9	008	006	006
#32	024	FF0	FFA	003	003	FF6	005	FFD	004	FFC	005	006	005	001	FFD	001
	FEF	008	FFB	FFF	001	FFE	003	FFF	008	001	FFF	FFE	002	000	000	FFF
	FFE	FFD	002	FFF	000	000	FFF	000	FFF	303	001	FFF	FFE	FFF	001	FFF

Table 1 (continued)

From: Barry G. Haskell
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To: Mr. T. Koga
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Dear Mr. Koga,

Recall our lengthy discussions on the problem of mismatch between the coder and decoder inverse transform. You said you might be able to carry out some mismatch experiments on the flexible hardware. In particular, the decoder inverse transform coefficients could be altered or truncated somewhat to simulate a mismatch. Then the effect on picture quality of various refresh rates could be studied.

Have you been able to make any progress on this problem? We would only need to know what you did to the inverse transform coefficients and what refresh rate you needed to maintain good picture quality. We could then compute the Mean Square Mismatch error using random data and specify the allowable MME for 384 kbs.

I have talked with David Hein, and his preliminary results are encouraging. Some mismatch at 384 kbs seems allowable, as long as refresh occurs at a reasonable rate. However, it would be much more satisfactory to have some real-time hardware results to back it up.

Operation at 64 kbs seems to be no problem.

I await your reply, and thank you in advance.

Sincerely,

Barry Haskell

To Mr. B.G. Haskell
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From Toshio Koga (22-3130)
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Subject IDCT Mismatch Problem (~~Three~~ Two pages including this.)
Date March 1, 1988

Dear Mr. Haskell:

Thank you for your facsimile letter on the problem of mismatch between the coder and decoder inverse transform.

Using our Flexible Hardware, we observed reproduced sequences when the accuracy of IDCT in the decoder loop was changed. As seen from the attached bit diagram, truncation at ① (2**-5), ② (2**-4), and ③ (2**-1) was carried out. The first two approximations were made to the out put data between the first and the second 1D-IDCT. According to the current Flexible Hardware specification, it has a 16-bit(11.5) accuracy.

Truncation at 2**-5(①) hardly produces visible degradation for teleconference video sequences even ten seconds after the truncation gets started. Although truncation at 2**-4(②) affects picture quality about several seconds after, rounding at 2**-4 will produce no visible distortion within ten seconds according to our previous simulation work. Rounding at 2**-4 will be simulated soon to make it sure. Truncation at 2**-1(③) gives no good result.

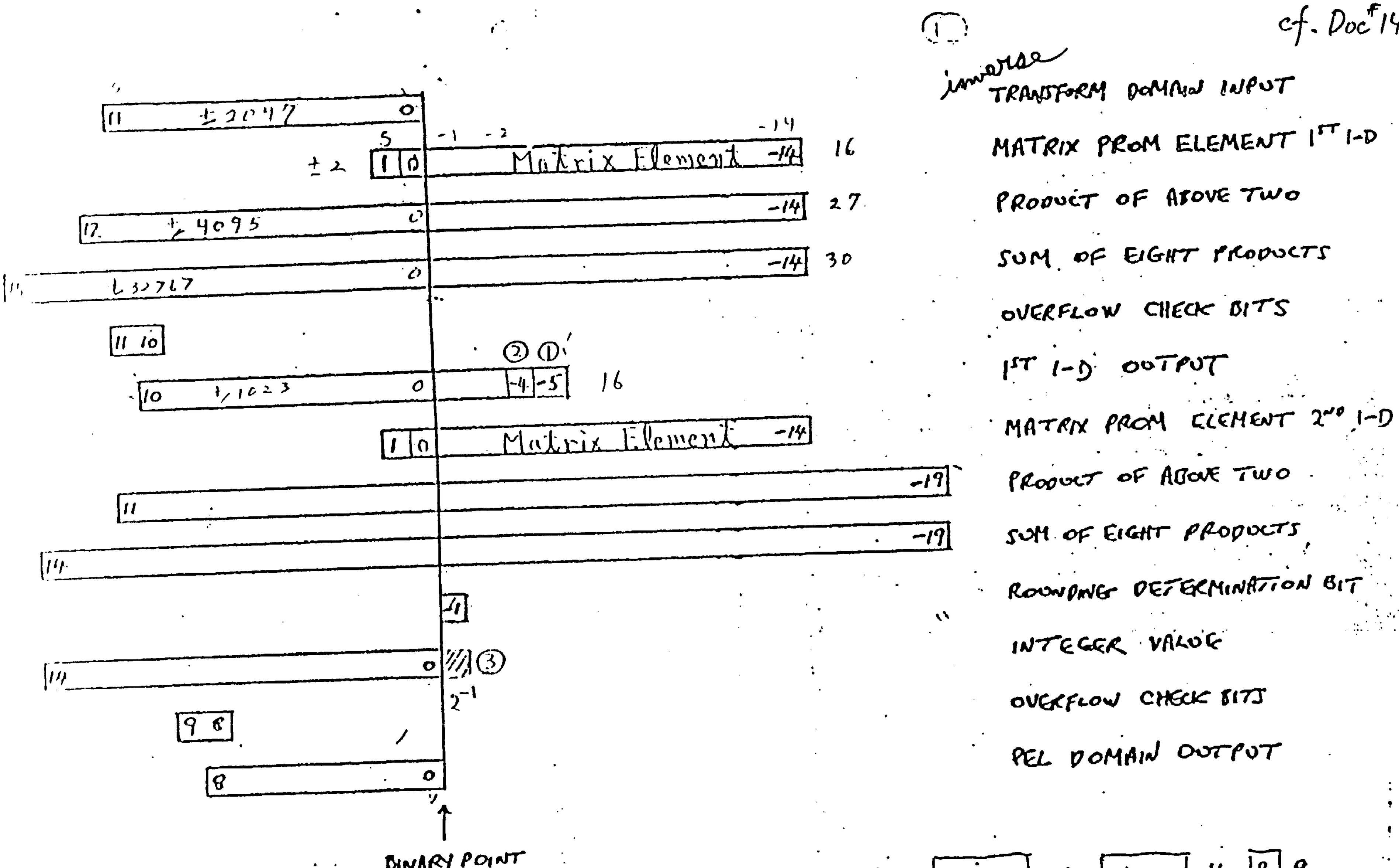
In this experiment, we did not change matrix element values, since they do not affect the experimental results as long as their accuracy is higher than, for instance, 12 bits (currently 16 bits)

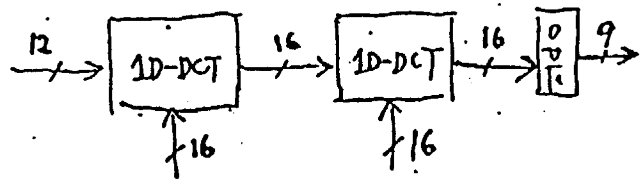
At the moment, the experimental results give us a feeling that truncation at 2**-5 for the output data from the first IDCT or its equivalent approximation accuracy by some IDCT algorithms other than the matrix approach will be possible, and in addition rounding gives a better result.

Refresh cycle may be about ten seconds or longer.

Note : Approximation should carefully be made to sequences with highly saturated color, for instance, Color Bar.

cf. Doc# 142





2-D INVERSE TRANSFORM BIT SPANS

From: Barry G. Haskell
AT&T Bell Labs
Holmdel, NJ 07733
USA

phone: +1 201 949 5459
fax: +1 201 949 3697

To: Mr. T. Koga
Second Development Department
Transmission Division
NEC Cporporation
1753, Shimonumabe, Nakahara-ku
Kawasaki City 213 JAPAN

phone: +81 44 433 1111
fax: +81 44 433 5214

Dear Mr. Koga,

Thank you for your results on mismatch experiments.

We did corresponding computer simulation noise measurements using random pel data, and got the following results:

Operation	Maximum pel MME	Overall MME	
1. Truncation to 15-bits	0.083	0.011	OK
2. Truncation to 14-bits	0.116	0.026	Not OK
3. Rounding to 14-bits	0.066	0.021	OK

I assume your studies were using 320 kbs for the video. Was there any systematic refresh during the measurements? We assume not.

On the basis of information from you and David Hein, I sent the attached letter to chip manufacturers. We will hear their response. If you have any further thoughts or results, please let me know.

I await your reply, and thank you in advance.

Sincerely,

Barry Haskell

To Mr. B.G. Haskell
AT&T Bell Labs
Holmdel, NJ 07733
Tel +1 201 949 5459
Fax +1 201 949 3697

From Toshio Koga (22-3130)
Second Development Department
Transmission Division
NEC Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki City, 211
Tel +81 44 433 1111 Ex3134
Fax +81 44 433 5214

Subject IDCT
Date March 16, 1989

(~~pages including this.~~) This page only.

Thank you for your letter on Proposed Specifications.
I would like to make a few comments on that.

1. In our hardware measurements, transmission bit rate for video was 320kb/s. Reproduced sequence was obtained without cyclic refresh. Immediately after fast updating sequence in Intra-mode, truncation was carried out and then reproduced picture was observed until visible distortion appeared.
   Your assumption is correct.

2. Distortion is much more visible for highly saturated pictures or parts of picture such as Color Bar.
   We should be careful about this result.

3. In practical IDCT calculation, we can distinguish two kinds of distortion, one being due to the approximation (rounding to 9 bits) and the other being due to mismatch. Base-line approach corresponds to a certain approximation.
   This will lead us to use real number computation to obtain "reference" as you did.

4. Two examples of truncation to 14 and 15 bits will be demonstrated using VTR in the Hague meeting.

Unfortunately, I can not attend at the Hague meeting. Mutsumi Ohta, who participated in the Tokyo meeting last January, will act for me.
I hope we can have happy results.

Best regards.

Toshio Koga

Toshio Koga

From: Barry G. Haskell
HO 4C-538
AT&T Bell Labs
Holmdel, NJ 07733
USA

phone: +1 201 949 5459
fax: +1 201 949 3697
telex: 219879 BTLH UR

To: Respondents to CCITT Request for DCT

Dear Sirs and Mesdames:

Thank you for your responses so far to the CCITT request for DCT chip information. Based on software received as well as computer simulations and hardware codec studies, we think we are near to a performance specification that would work for ISDN video codecs. We are thinking of a procedure (see attached) that would be suitable for computer simulation.

Could you examine the proposed method and let us know your thoughts? The peak error constraint is fairly firm, whereas the mean-square error constraints may possibly be relaxed slightly as we gain more experience with the codecs.

We will need your responses by March 18 at the latest. If I do not yet have your fax number, could you send it? Thank you.

Sincerely yours,

Barry Haskell

CCITT Specialists Group on Visual Telephony

Proposed Specification for Inverse DCT Chips

1. Generate random integer pixel data values in the range -256 to +255. Arrange into 8x8 blocks.
2. For each 8x8 block, perform a separable, orthonormal, matrix multiply, Forward Discrete Cosine Transform (FDCT) using at least 32-bit floating point accuracy.
3. For each block, round the 64 resulting transformed coefficients to the nearest integer values. Then clip them to the range -2048 to +2047. This is the 12-bit input data to the inverse transform.
4. For each 8x8 block of 12-bit data produced by step 3, perform a separable, orthonormal, matrix multiply, Inverse Discrete Cosine Transform (IDCT) using at least 32-bit floating point accuracy. Round the resulting pixels to the nearest integer, and clip to the range -256 to +255. These blocks of 8x8 pixels are the "reference" IDCT output data.
5. For each 8x8 block of 12-bit data produced by step 3, use the proposed IDCT chip or an exact-bit simulation thereof to perform an Inverse Discrete Cosine Transform. Clip the output to the range -256 to +255. These blocks of 8x8 pixels are the "test" IDCT output data.
6. For each of the 64 IDCT output pixels, measure the peak and mean square mismatch error between the "reference" and "test" data.
7. For any pixel, the peak error should not exceed 1 in magnitude.
   For any pixel, the mean square error should not exceed 0.06
   Overall, the mean square error should not exceed 0.02

Bell Communications Research

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FAX: 949-3697

March 15, 1988

Dr. B. G. Haskell
AT&T Bell Labs
HO 4C-538
Crawfords Corner Road
Holmdel, New Jersey 07733

Dear Dr. Haskell:

Thank you for sending us the "Proposed Specification for Inverse DCT Chips." Following are our comments to the enclosed document

1. Item 7, line 2 - Shouldn't the "pixel" be "block"?
2. Shouldn't the random number generator algorithm be specified?
3. How many blocks of random numbers should be simulated?
4. Shouldn't the speed requirements of the chip be specified?
5. The mean-square error specification may be relaxed a little bit

Please call me if you have any further questions.

Sincerely,

Ming-Ting Sun

Ming-Ting Sun
Member of Technical Staff
Signal Processing Systems Group

Attachment

CNTR NO: 2632

To: B G Haskell
AT&T Bell Labs
Holmdel, NJ
USA

From: Colin Smith, Inmos, Bristol, UK
cc Peter Cavill

Date: 18th March 1988.

Subject: **Proposed Specification for Inverse DCT chips**

Dear Mr. Haskell,

Thank you for your specification of a procedure for the DCT coding. Our simulations are broadly in line with the proposed method and any minor differences will be corrected in line with your fax, so that we can estimate the error values for the random integer pixel data input.

However in order to compare resultant error rates it is important to know if any scaling has been applied to the coefficients when performing the DCT. We think that this information should be added to the proposed specification.

Regards,

Colin Smith

Manager, DSP Products.

FAX to: +1 201 949 3697

Dr. B. G. Haskell
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Video Sys. & Tech. Lab.
R & D Center TOSHIBA
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Saiwai-ku Kawasaki 210
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phone: +81 044 511 2111
fax: +81 044 555 2074

March 18 1988

Dear Dr. Haskell:

Thank you for your last letter. We examined our Inverse DCT algorithm according to the method specified in your letter and found that our algorithm meets the specified conditions. The algorithm is described on page 2. On a pixel-by-pixel basis, the peak error is consistently 1.0, and no mean squared error value exceeds 0.06. Overall, the mean square error is 0.02. The test was conducted for 20000 blocks of independent, uniformly distributed random data.

Sincerely yours,

Sadao Takahashi

FAX to: +1 201 949 3697

Dr. B. G. Haskell
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USA

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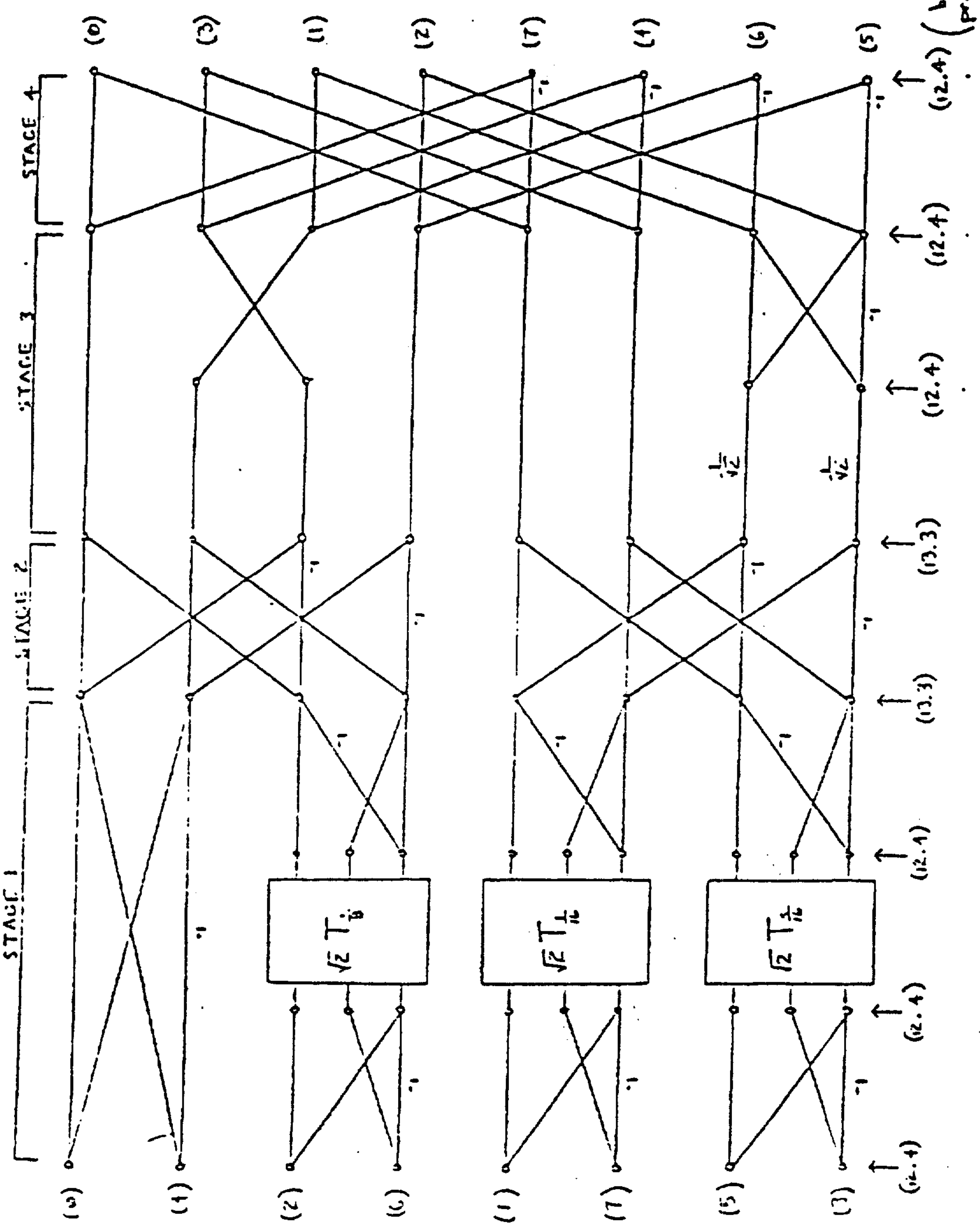

FIGURE 1: FAST INVERSE COSINE TRANSFORM (1-DIM)

FAX to: +1 201 949 3697

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USA

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Saiwai-ku Kawasaki 210
JAPAN

NUMBER OF INPUT DATA BLOCKS: 20000

PEAK ERROR

1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

MSE (PIXEL-BY-PIXEL BASIS)

0.04	0.02	0.02	0.02	0.02	0.02	0.02	0.02
0.05	0.02	0.02	0.02	0.02	0.02	0.02	0.02
0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02
0.01	0.02	0.02	0.02	0.02	0.02	0.02	0.02
0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02
0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02
0.06	0.02	0.02	0.02	0.02	0.02	0.02	0.02
0.04	0.02	0.02	0.02	0.02	0.02	0.02	0.02

OVERALL MSE = 0.02

Three of Three

IEEE

CIRCUITS AND SYSTEMS SOCIETY

Ming L. Liou
President

PLEASE REPLY TO:
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331 Newman Springs Road
Red Bank, NJ 07701 USA
Telephone: (201) 758-2949
Telex: 275 318
FAX: (201) 758-0889

March 14, 1988

Dr. B. G. Haskell
AT&T Bell Labs
Crawfords Corner Road
Holmdel, New Jersey 07733

Dear Barry:

In response to the CCITT Specialists Group on Coding for Visual Telephony's inquiry to encourage manufacturers and IEEE to contribute to making an industry standard for DCT chips, the IEEE Circuits and Systems Society has agreed to undertake such a task.

A Standards Committee, chaired by Dr. Ming-Ting Sun of Bellcore, has been established within the Circuits and Systems Society. The committee will first submit a Project Authorization Request (PAR) to the IEEE Standards Board for approval. After approval of the project, various organizations within IEEE expressing interests will be asked to participate.

Since the CCITT, ISO, and other organizations have already done some work on DCT standards, the Circuits and Systems Standards Committee will rely heavily on these results during the standardization process.

Sincerely yours,

Ming L. Liou

From: Barry G. Haskell
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fax: +1 201 949 3697
telex: 219879 BTLH UR

To: F. Molo
Telettra Vimercate

Dear Mr. Molo

Thank you for sending your software for simulating your DCT chip. Unfortunately, I was unable to get it to work properly, I think.

We really only need the inverse transform. Perhaps you could change the software slightly to provide a subroutine

INVDCT(BLOCCI, BLOCCO)

where BLOCCI is an 8x8 input matrix of DCT integer coefficients in the range -2047 to +2047, and BLOCCO is an 8x8 output matrix of pixel integer values in the range -255 to +255.

I am concerned about your statements ...

"sine and cosine of angles different from canonical ones"

"line and column DCT are not exactly the same"

Any chip to be used in a standard codec would have to work with other codecs that do use the canonical, seperable, orthonormal Discrete Cosine Transform.

If you have any more advice, please let me know. Thank you.

Sincerely yours,

Barry Haskell

February 22, 1988

From: Barry G. Haskell
AT&T Bell Labs
Holmdel, NJ 07733
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phone: +1 201 949 5459
fax: +1 201 949 3697
/6172

To: Mr. Richard C Nicol
British Telecom Research
Martlesham Heath, Ipswitch IP5 7RE
UNITED KINGDOM

phone: +44 473 642710
fax: +44 473 643791

Dear Richard,

I got your Telex of February 19! Our letter (copy attached) went out on February 2 to NCR, INMOS, Thomson, Bellcore, Siemans, Telettra, Philips and AT&T. It went out to Plessy on Feb. 17.

We have received software from Telettra, Bellcore and AT&T. INMOS called two weeks ago and said they would send it. Could you see if that is still their intention? Call Peter Cavil (0454 616616).

I talked with David Hein and sent a fax (copy attached) to Koga at NEC.

I think we'll be able to converge on something fairly quickly.

Thanks,

Barry Haskell

Nachrichtentechnik

ANT Nachrichtentechnik GmbH · Postfach 1120 · D-7150 Backnang

Dr. B.G. Haskell
AT&T Bell Laboratories
HO 4C-538
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	MX/V,Bö/kl / Börner	2589	11.03.88

CCITT Video Coding Experts Group
Solicitation of information about DCT chips

Dear Sir,

We have been informed about your a.m. request, and we are pleased to address you in this matter.

Our company is engaged since years in advanced techniques for image processing, including elaboration of coding/decoding algorithms allowing transmission bit rates of n x 64 kbit/s. In the context of this work, DCT has been used, and a pertinent semicustom chip is under realisation which could be a candidate solution for a CCITT Video Coding standard. Whilst sample quantities are available on short term, volume production will depend upon market request and could be envisaged for 1989.

As we are interested in video conferencing techniques, we are prepared to support the realization of CCITT standards. Consequently, we very much would appreciate to have your indication along which terms CCITT intends to identify a standard solution out of various candidates. We are willing to consider adequate arrangements including patent and licencing aspects.

We will appreciate your advice how to pursue this matter further. You are kindly invited to contact us if we can assist in CCITT standardisation.

Sincerely yours,

Dr.Welzenbach Börner