CCITT SG XV
Specialists Group on Coding for Visual Telephony

Doc#332
Hague March 88

Source: UK, FRANCE

Title: Network Synchronisation - clarification of document #293 presented in Tokyo

1. Summary

This document attempts to explain in more detail the purpose of our proposal concerning codec line clock generation (doc.#293) which was presented at the last CCITT SG XV meeting in Tokyo.

2. The Problem

Some digital networks are synchronous and sourced by very high stability clocks. Codecs on these networks need to lock their network transmit line frequency to the incoming clock from the network.

Other networks are asynchronous and expect the clock to be sourced by the terminal codec equipment. Terminal equipment should be inexpensive and so codec clock sources are allowed to operate within a fairly wide 2.048Mbit/s$\pm$ 50ppm frequency range when connected solely by an asynchronous network.

For correct operation it is necessary to know whether a codec is connected to an asynchronous or synchronous network and thus the H.120 2Mbit/s codec hardware specification uses bit 3 of timeslot zero (TS0) to indicate whether internal or receive line clock should be used for the transmit path.

There are a number of potential problems with this arrangement. These are:-

1. Synchronous networks do not usually generate a TS0 framing. TS0 is merely passed from the distant terminal equipment transparently through the network to the receive equipment. Synchronous networks cannot always set bit 3 in TS0 and therefore codecs have to be set manually to synchronous operation.

2. Synchronous networks which can intercept and modify TS0 often do not adopt the rule of TS0 bit3 being set.

3. TS0 is sometimes removed by multiplexing equipment in the network and then re-inserted further along the transmission route. Thus even if the network did set bit 3 TS0 correctly there is no guarantee that the terminal codec would receive bit 3 set.

4. When international connection are achieved asynchronous networks have to interwork with synchronous networks. Thus codecs which

normally derive their clock internally have to switch to synchronous operation on per connection basis. For the reasons described above this will probably have to be done manually.

5. 64kbit/s X.21 interfaces provide only one bit clock which is assumed to be phased with both the send and receiving data. Therefore, in all cases where a codec equipment has X.21 ports provided, correct operation can only be guaranteed if the send and receive clocks on the 2Mbit/s network are identical. It is therefore necessary to have the two codecs locked together even when operating on an asynchronous network. This means that a master slave arrangement has to achieved by manual intervention on a per connection basis.

Manual switching of clocks on a per connection basis is highly undesirable. Apart from the inconvenience, inevitably the wrong selection will be made occasionally and service will not be reliable. The technique described below attempts to overcome all of the problems described above by automatically locking codec send and receive frequencies without using bit 3 in TS0.

3. Solution

The proposed method facilitates the following:-

1. Codecs on asynchronous networks lock together and permanently remain within a frequency range of 2.048Mbit/s ± 50ppm.

2. Codecs on asynchronous networks lock to synchronous sources when inter-network connections are made.

This is achieved by including in the codec design a phase locked loop which attempts to lock the transmit oscillator to the incoming clock frequency providing it is within the frequency tolerance limit of ± 50ppm.

Codecs will therefore either lock together OR in the case of synchronous networks, lock to the network frequency .

To achieve this the clock of the transmission encoder of the codec must be designed to adjust towards the incoming 2Mbit/s data clock, but at all times remain within the ± 50ppm frequency tolerance limit.

Only three aspects of the interface need be specified:

1. The encoder clock frequency should adjust towards the receive frequency and have a range of at least 2.048MHz ± 1ppm. The ±1ppm range is wide enough to allow locking to all synchronous high accuracy sources and narrow enough to allow for crystal ageing etc. (Note. This is a minimum range and therefore ±1ppm is easier to achieve than say ±2ppm). Greater ranges are allowed up to 2.048MHz ± 50ppm.

2. The encoder clock must not operate outside the range ± 50 ppm.

3. The receiving port will accept and decode bit rates of 2.048Mbit/s ± 50ppm.

The voltage controlled oscillator employed in the design can have a fairly relaxed specification with a nominal range of say ± 25ppm. Taking into account ageing, temperature stability and supply voltage variation operation within 1ppm of nominal can be guaranteed without the source being able to drift outside of the ±50ppm limit.

The method may also be suitable for 1.544Mbit/s networks.

4. Proposal

The technique described theoretically overcomes the problems which arise from mixed asynchronous and synchronous environments. It is proposed that trials should be made to establish if the idea is practical.