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TITLE : A DOUBLE ERROR CORRECTION BCH ENCODER/DECODER LSI

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1. INTRODUCTION

An error correcting code allows to secure the reliability of serial data communication system. A BCH code for double error correction is very popular in the fields of high efficiency transmission of audiovisual information. In this document, a VLSI chip of the BCH Encoder / Decoder is briefly introduced.

A major specification and a functional block diagram are shown in Table 1 and Fig.1, respectively. A 2-bit control input selects one of four BCH code variations, (63,51), (127,113), (255,239) and (511,493). And, another 9-bit control input programs shortened length for one of these BCH codes. Moreover, additional function enables to handle following 1 extension bit : overall parity bit or external framing bit. Therefore, this BCH-LSI can program variable word length up to 512 bits. Two peripheral components are required for decoding operation : a data ROM for syndrome mapping and the shift register with programmed word length for decoding delay compensation. The VLSI chip can only be delivered as a test sample since it is not a commercial version.

2. ENCODER

The BCH encoding operation is carried out by using the linear feedback shift registers(LFSRs) and systematic code blocks are sequentially generated. The LFSRs can select a type of the following four generator polynomials :

(63,51)BCH : $g(x) = (x^6 + x^5 + 1)(x^6 + x^5 + x^4 + x^2 + 1)$
(127,113)BCH : $g(x) = (x^7 + x^3 + 1)(x^7 + x^3 + x^2 + x + 1)$
(255,239)BCH : $g(x) = (x^8 + x^4 + x^3 + x^2 + 1)(x^8 + x^6 + x^5 + x^4 + x^2 + x + 1)$
(511,493)BCH : $g(x) = (x^9 + x^4 + 1)(x^9 + x^6 + x^4 + x^3 + 1)$

Since the LFSRs can generate the shortened word of the above BCH codes, this BCH-LSI enables to select variable word length and to encode information data block by block. Furthermore, this BCH-LSI has bit extension options, which can be alternatively selected : (1) The overall parity bit generation and (2) Addition of the external framing bit to indicate the head / tail of encoded BCH code block. The start of each BCH encoding operation is controlled by frame synchronization mode or data handshake mode.

3. DECODER

This BCH-LSI consists of a parity checker, two syndrome generators, an error position detector, and internal shift registers for decoding delay compensation. In the decoding operation, two syndromes S1 and S3 are generated for each BCH code block by the two syndrome generators. Then, in the error position detector, the two syndromes S1 and S3 are transformed into the discrete logarithms of themselves and mapped into the external data ROM. Finally, the error positions of each BCH code block are detected from this external ROM and error correcting operation is carried out according to the results.

The above error correcting operation requires only 32 clocks and can be performed successive decoding operation by pipeline technique. The total delay time of the decoding operation is "A block period of single BCH code + 32 clocks". Furthermore, the decoder can also generate the optional data status: channel status and decoding status. The channel status indicates that an error of up to 3 bit has been detected in each BCH code block. The decoding status indicates that a 3-bit error or a uncorrectable error has been appeared in the block. A typical frame structure of the BCH code block is shown in FIG.3.

REFERENCE : A. YAMAGISHI, et al. ,"A CODEC LSI for 2-bit Error Correction BCH Code with Variable Code Word Length", National Conf. Record, 1986, IECE Japan, No.1408 (1986).

TABLE1. THE FEATURES OF THE BCH ENCODER/DECODER LSI (Test sample)

Master Slice/Package	CMOS 8k-Gate Gate Array/128-pin Ceramic PGA(Overview is illustrated in Fig.2)
Max. Operating Bit Rate	Max 6.3 Mbps(Max Clock Rate: 6.3 MHz)
I/O Interface	TTL Compatible
Selectable BCH codes	(63,51), (127,113), (255,239), (511,493) Double Error Correction BCH
Optional Functions	1. Allover Parity Checker(Odd/Even) 2. Framing Bit Extension(Head/Tail)
Peripheral Components for Decoding Operation	1. Shift Registers(delay length = "A Single BCH Code Block") 2. Syndrome Mapping ROM(Up To 2k-Byte x2)

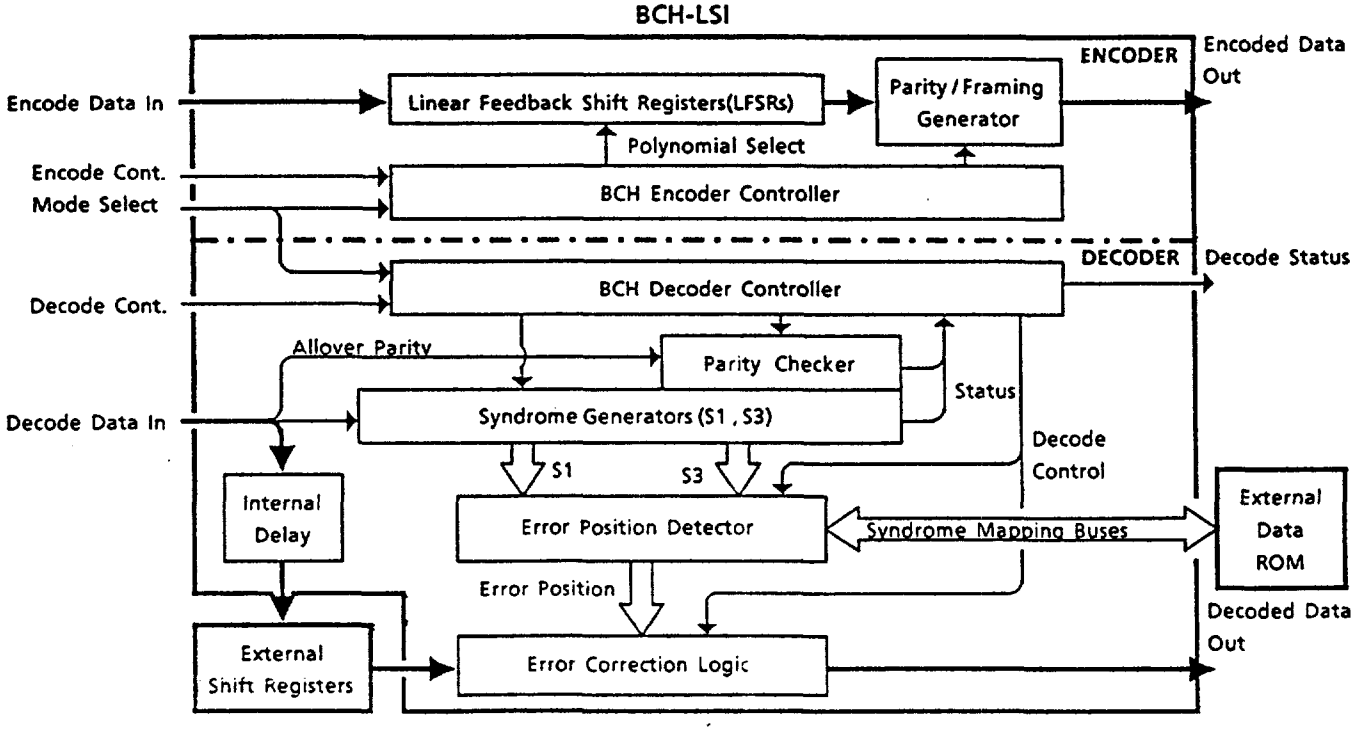
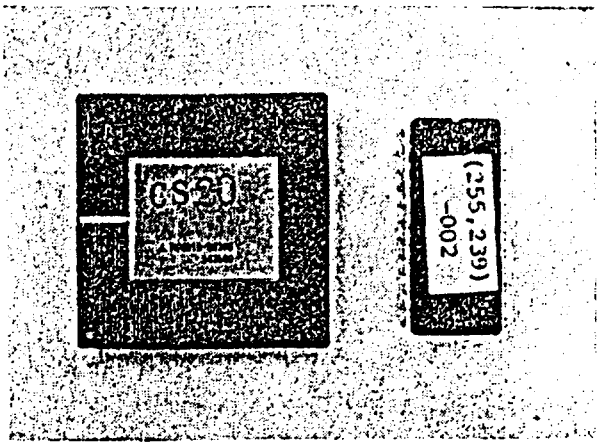


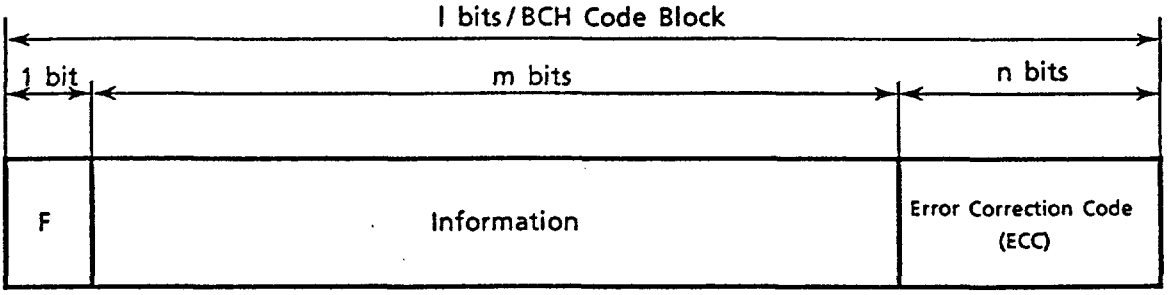
FIG1. THE FUNCTIONAL BLOCK DIAGRAM OF THE BCH ENCODER/DECODER LSI



BCH ENCODER/DECODER LSI
(128-Pin Ceramic PGA Package)

EXTERNAL DATA ROM
for BCH DECODER
(2KByte P-ROM)

FIG2. An OVERVIEW OF THE BCH-LSI



BCH-LSI : Internal Framing Mode
F : BCH Framing Bit (User Programmable)
I = 1 + m + n

(63,51) BCH and Its Shortened : m = 51 - s, n = 12
(127,113) BCH and Its Shortened : m = 127 - s, n = 14
(255,239) BCH and Its Shortened : m = 255 - s, n = 16
(511,493) BCH and Its Shortened : m = 511 - s, n = 18
[s : Shortened Length (9-bit Control Input : 0~Max. 511)]

FIG3. A TYPICAL FRAME STRUCTURE OF THE BCH CODE BLOCK