CCITT SG XV
Specialists Group on Coding
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Doc#293

Source: UK, FRANCE

Title: Network Synchronisation

1. Summary

At the CCITT SG XV meeting in Stockholm, document 243 (source France) described a method for allowing codec equipment to operate synchronously over an asychronous network. The method involved using a phase locked loop design with a very tight specification.

Further work in France and UK has led us to believe that the proposed method should be tested during field trials of the flexible hardware. A modification of the original specification is suggested which will allow the crystal performance to be relaxed.

2. The Problem

Some digital networks are synchronous and sourced by very high stability clocks. Other networks are asynchronous and expect the clock to be sourced by the terminal codec equipment. Terminal equipment should be inexpensive and so codec clock sources are allowed to operate within a fairly wide 2.048Mbit/s± 50ppm frequency range when connected solely by an asychronous network.

64kbit/s X.21 interfaces provide only one bit clock which is assumed to be phased with both the send and receiving data. Therefore, in all cases where a codec equipment has X.21 ports provided, correct operation can only be guaranteed if the send and receive clocks on the 2Mbit/s network are identical.

In the case when a codec on an asynchronous network inter-works with a codec on a synchronous network the asynchronous codec must lock to the synchronous source.

A method must therefore be found which automatically allows:-

1. Codecs on asynchronous networks to lock together and permanently remain within a frequency range of 2.048Mbit/s ± 50ppm.

2. Codecs on asynchronous networks to lock to synchronous sources when inter-network connections are made.

3. Solution

The transmission encoder of the codec must be designed to adjust towards the incoming 2Mbit/s data clock, but at all times remain within the ± 50ppm frequency tolerance limit.

Only three aspects of the interface need be specified:

1. The encoder clock frequency should adjust towards the receive frequency and have a range of at least 2.048MHz ± 1ppm.

2. The encoder clock must not operate outside the range ± 50 ppm.

3. The receiving port will accept and decode bit rates of 2.048Mbit/s ± 50ppm.

The voltage controlled oscillator employed in the design can have a fairly relaxed specification with a nominal range of say ± 25ppm. Taking into account ageing, temperature stability and supply voltage variation operation at ± 1ppm of reference can be guaranteed without the source being able to drift outside of the ±50ppm limit.

4. Proposal

The technique described theoretically overcomes the problems which arise from mixed asynchronous and synchronous environments. It is proposed that trials should be made to establish if the idea is practical.