CCITT SGXV
Working Party XV/1
Specialists Group on Coding for Visual Telephony

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SOURCE: NTT, KDD, NEC and FUJITSU
TITLE : CONSIDERATIONS ON FORWARD ERROR CORRECTION

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1. Introduction

Video coding strategy is intended in the Flexible Hardware Specification which is error resilient without internal or external error corrector (see §3.7/Doc. #249). In a hardware without special care for error resilience, however, random error rate of 3.8x10E(-6) gave unacceptable performance to suggest the necessity of forward error correction (cf tape demonstration associated with Annex 2/Doc. #254).

This document discusses several aspects of the forward error correction (FEC) in preparation for the case that it becomes necessary.

2. Adoption in the Recommendation

Experimental results of the error resilience approach will determine whether FEC is required or not as follows;

1) FEC is mandatory if the error resilience approach is not satisfactory.
2) FEC is optional if the error resilience approach is satisfactory but with complex implementation.
3) FEC is unnecessary if the error resilience approach is satisfactory with simple implementation.

For the first and second cases, FEC should be defined in Recommendation H.12x. Furthermore, control and indication method for usage/non-usage of FEC should also be defined in the second case.

3. Error Correcting Code

3.1 Items to be considered

Well experienced BCH code is a strong candidate. The following parameters should be specified;

- Block length: 255, 511, 1023 or 4095 is practical,
- Number of corrected bits in the block,

by evaluating the following items;

1) Error correcting capability,
2) Processing delay,
3) Transmission efficiency, and
4) Hardware complexity.

3.2 Error correcting capability

Mean time between error (MTBE) is plotted against bit error rate in Fig. 1. If we apply a measure of MTBE longer than 4 hours for 320 kbit/s (around 1

hour for the primary rate, no errors are seen in an ordinary length videoconferencing session), single error correction is not sufficient. For double error correction, the block length must not be longer than 1023.

Figure 1 shows that the (4095,4035)BCH which has been implemented in a Japanese flexible hardware may provide better than required performance for the random error.

3.3 Processing delay

Minimum necessary decoding delay is shown in Fig. 2 for 320 kbit/s transmission. More delay is required in the real hardware. For the block length of 4095, delay time becomes comparable of one CIF picture time.

3.4 Transmission efficiency

Relationship between transmission redundancy and error correcting code is shown in Fig. 3. It can be said that the redundancy of (255,239)BCH is too much compared to various improvements tried in the source coding.

3.5 Hardware complexity

Problems are in the decoder whose hardware quantity increases according to the block length.

4. Where to Place Parity Bits

It should be decided whether transmission framing or independent framing is used for inserting parity bits.

1) Use of transmission framing

If we use the multimedia multiplex framing and transmit parity bits in appropriate bit positions such as AC, we can save extra framing bits. Since we can not choose block length identical to the transmission frame length, however, some transmission efficiency is lost due to shortening the code.

It is noted that about 120 parity bits are required for a 10 ms frame in case of the double error correcting (511,493)BCH, which obviously can not be transmitted through AC in the service channel of draft H.221 frame structure.

2) Use of independent framing

Error protection is assumed to be carried out outside the frame structure in draft H.221 according to the necessity of each medium. Hence it is more natural to do error correction before the transmission frame structure, namely at the video coder side in the transmission coder. Another advantage of independent framing is that FEC can be switched on/off in cae of being optional without affecting other parts of the codec.

An example of framing for FEC is described in the draft Part 3/H.120, where a 256 bit frame is made of 1 framing bit and 255 information and/or parity bits and 16 such frames make a multiframe (see Fig. 4). The number of frames in a multiframe may be reduced to 8.

5. Experience

We have experience of implementing (255,239)BCH, (511,493)BCH and (4095,4035)BCH in existing codecs (Note). The decoding hardware quantity is significantly different between the second and the third. It is noted that the first one is specified in draft Part 3/H.130, while the third one is specified as an option in Part 1/H.130.

Note:

BCH	Generating Polynomial
(255,239)	$g(x) = (x^8+x^4+x^3+x^2+1)(x^8+x^6+x^5+x^4+x^2+x+1)$
(511,493)	$g(x) = (x^9+x^4+1)(x^9+x^6+x^4+x^3+1)$
(4095,4035)	$g(x) = (x^{12}+x^{11}+x^6+x^4+x^2+x+1)(x^{12}+x^{11}+x^{10}+x^9+x^7+x^6+x^5+x^4+1)$ $(x^{12}+x^{11}+x^{10}+x^8+x^6+x^4+x^3+x^2+1)(x^{12}+x^{10}+x^9+x^6+x^5+x^3+x^2+x+1)$ $(x^{12}+x^{11}+x^{10}+x^9+x^8+x^6+x^5+x^2+1)$

6. Conclusion

The following specification is provided for discussion, assuming that FEC may be necessary in the final Recommendation.

1) Handling in the Recommendation: Optional or mandatory according to the experimental results of the error resilience approach.

2) Code: Double error correcting (511,493)BCH.

3) Parity transmission: Independent framing with multiframe of (16 or 8) frames, where a frame is (255 information/parity bits + 1 framing bit).

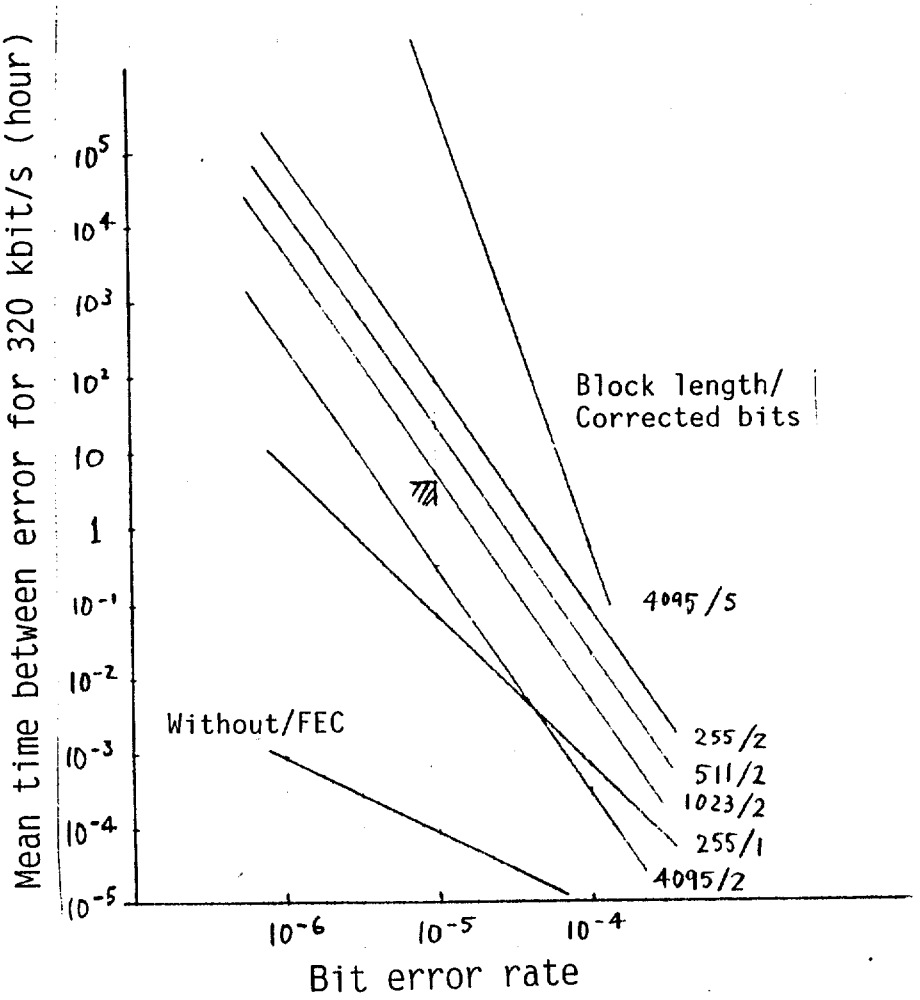
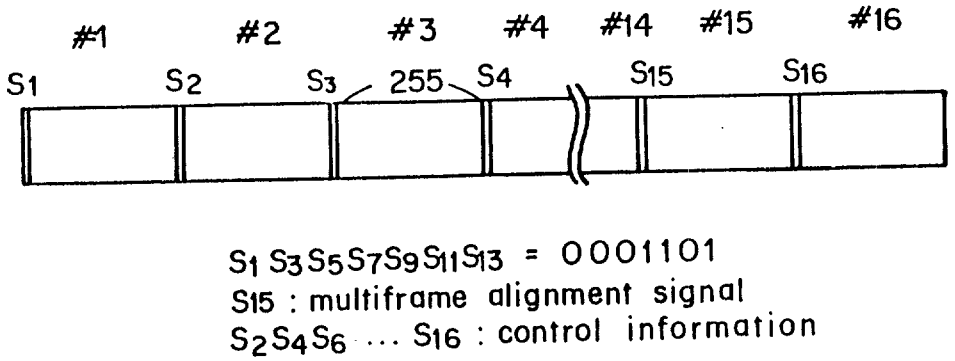


Figure 1 Error correcting capability of BCH codes



$S_1 S_3 S_5 S_7 S_9 S_{11} S_{13}$ = 0001101
S15 : multiframe alignment signal
$S_2 S_4 S_6 \cdots S_{16}$: control information

Figure 4 Example of framing for FEC (Draft Part 3/H.130)

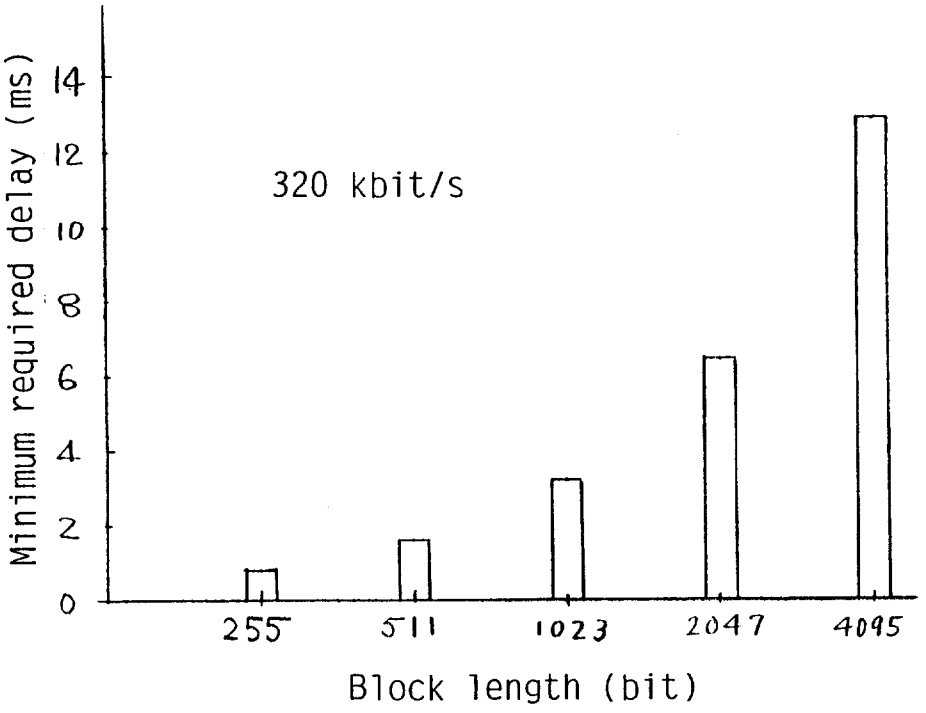


Figure 2 Processing delay vs block length

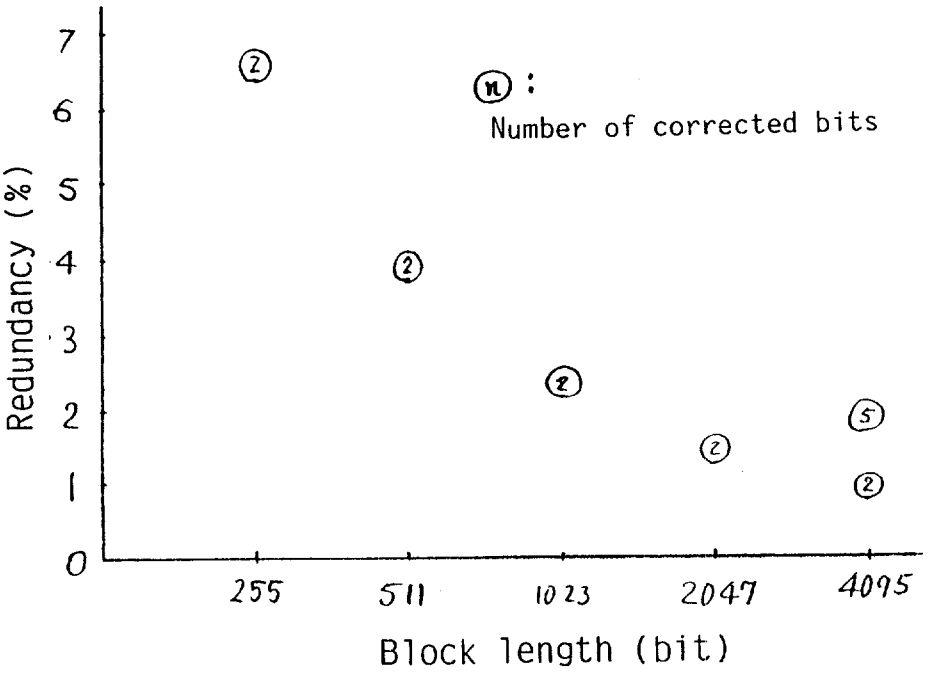


Figure 3 Redundancy of BCH codes