CCITT Study Group XV
Working Party XV/1
Specialists Group on Coding for Visual Telephony

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Title: The Transform - the realities.

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Introduction

The adoption of the part of the flexible hardware specification covering the transform allowed the specialists group to temporarily dodge some difficult questions. The group must not forget the existence of these issues, or under-estimate how serious they are.

The issues are revisited in this discussion document. Unfortunately no clear solutions can be identified.

Background

The key reason for the matrix multiplier approach was that it offered a 'safe' route for hardware construction to begin. It satisfied the following criteria:

1. It could be specified simply.

2. It permitted compatibility, theoretically at least, between inplementations, thereby evading the question of whether exact tracking of inverse transforms is necessary.

3. It could be constructed with standard catalogue devices.

4. A decision on which transform to use could be deferred.

5. Any need for decisions on accuracy, rounding etc could be minimised by incorporating 'overkill'.

6. It could be used for experiments and investigations to obtain information for a final specification to go into the recommendation.

Current Situation

The question of compatibility between the inverse transforms at coder and decoder has not been satisfactorily tackled. Obviously the loops can become out of step if the inverse transforms do not give the same numerical results, but the quantitative consequences are not known.

It could be argued that if the errors are small and randomly distributed then forced updating might occur frequently enough to prevent them accumulating to some critically visible stage. This is extremely difficult to tackle analytically with confidence, as the possible number of combinations of input

data, computational mistracking, predictors (motion vectors, filtered or not) and update periods are vast. Some factors are complex. For example, working to fewer bits in the result lowers the frequency of differences from nominal but they become more significant. There is also the practical problem that the update period is outside the scope of the specification. Thus the designer of an 'approximate' inverse transform has no guarantee what the update period of another designer's coder may be.

The implementations of the transform part of the flexible hardware specification are not viable for final products as opposed to laboratory test-beds.

It has been hoped that LSI will solve the compatibility and implementation cost issues together. However the realities of getting chips and a recommendation must be faced.

No chip, available or rumoured, complies with the flexible hardware specification. Therefore a chip must be designed to the specialists group specification (probably considerably changed from the flexible hardware one) or an available chip is deemed suitable and adopted. The group could spend much time and effort trying to agree a specification optimally suited to the n*384kbit/s codec, but the chances are small that a chip manufacturer would be enthusiastic to produce the device since the potential market for 384kbit/s codecs is relatively small. Prospects are gloomier when second sourcing is considered.

The alternative is to use what becomes avaiable in the market-place at the time the recommendation must be finalised. Contact is already being established with European manufacturers by the CEPT but this is not expected to produce a standardised solution quickly. Known activities include Thomson Semiconductors, AT&T Bell Labs and Telettra, but only the latter is said to have working samples at the moment. Details are scant with no hard information on the internal algorithms and accuracies. The commercial future of the devices is not certain either. Thomson's present schedule includes a decision on manufacturing in mid 1988 and final product definition in the third quarter of that year. The AT&T and Telettra activities seemingly were started for internal company projects only. Similarly, BT has collaborated with a university in the design of a chip and could obtain some just for the experience, but has no plans for them to become commercially available.

Industry standards are not emerging yet. Even supposing that one manufacturer did have firm commercial plans, would the members of the specialists group agree to that proprietary device being embedded in the n*384kbit/s recommendation?

One glimmer of hope is that graphics chips for computers are receiving much attention from IC manufacturers. To ride on the back of these developments would certainly bring low prices together with favourable chances of industry standards and multiple sourcing. One vendor has indicated that a general purpose matrix multiplier will be available, intended for rotation of images etc as well as arbitrary transforms. His view, also echoed by other LSI experts, is that multipliers are

no longer a problem and matrix multipliers may be as easy to produce as fast algorithms and the extra flexibility gives higher sales volume.

A related topic is compatibility with m*64kbit/s. It would be desirable to have the same transform for both, if indeed a transform approach is optimum for that rate, not just for connectability but also commonality of equipment and enhanced chip volumes. This might lead to conflict between hardware 64kbit/s codecs with matrix multiplier chips and DSP based ones running a fast algorithm in software.

Conclusion

There is little that the specialists group can do except encourage and await developments elsewhere.