

Source : NTT, KDD, NEC and FUJITSU

Title : PROGRESS REPORT OF JAPANESE HARDWARE PROJECTS

In Japan, two types of flexible hardware are being produced, and experiments are being carried out on each.

One type has already shown expected behaviour in checks at local mode and in digital circuit transmission tests via optical fibres and satellites. These codecs are due to be exhibited at TELECOM '87. Parameter checks for initial compatibility test, evaluation of quantization characteristics and so forth have also been carried out: the results are given in Annexes 1-3 to this contribution and Doc. #255 - #257. It should be noted that the results are presented in the form of parameters to be displayed at TELECOM '87 because of the time reason. Annex 4 summarizes discrepancies between these parameters and parameters for initial compatibility checks.

In the case of the other type of flexible hardware, the NTSC/CIF convertre has already been completed, and signals from the video source coder are now being inputted directly to the source decoder. Work is going ahead with a view to overall completion in November. A picture from the source decoder of this codec will be presented at the meeting.

Annexes and List of Related Contributions

- Annex
1. Overall picture
 2. Effect of transmission error
 3. Picture in higher bit rate operation
 4. Experimental parameters
 5. Pictures processed by the other type of flexible hardware

Topics of related contributions

- #255 Effect of mismatch due to precision of DCT calculation
- #256 Quantization characteristics
- #257 Transmission coefficient range discarding, variable block size processing
- #258 CIF picture

Effect of Transmission Errors

In the flexible hardware, a forward error correction (FEC) coding is introduced to ensure wide range of application. To reduce the error correcting code information, (4095,4035) BCH code is applied to our hardware. Transmission efficiency is then 98.5%. Figure 1 shows the capability of error correction coding. Demonstration on a VCR tape shows the decoded pictures which are affected by transmission errors and effect of FEC.

It can be pointed out that the codec is robust to maintain the picture synchronization without FEC and the FEC is quite effective when the transmission error rate is higher than 10^{-6} .

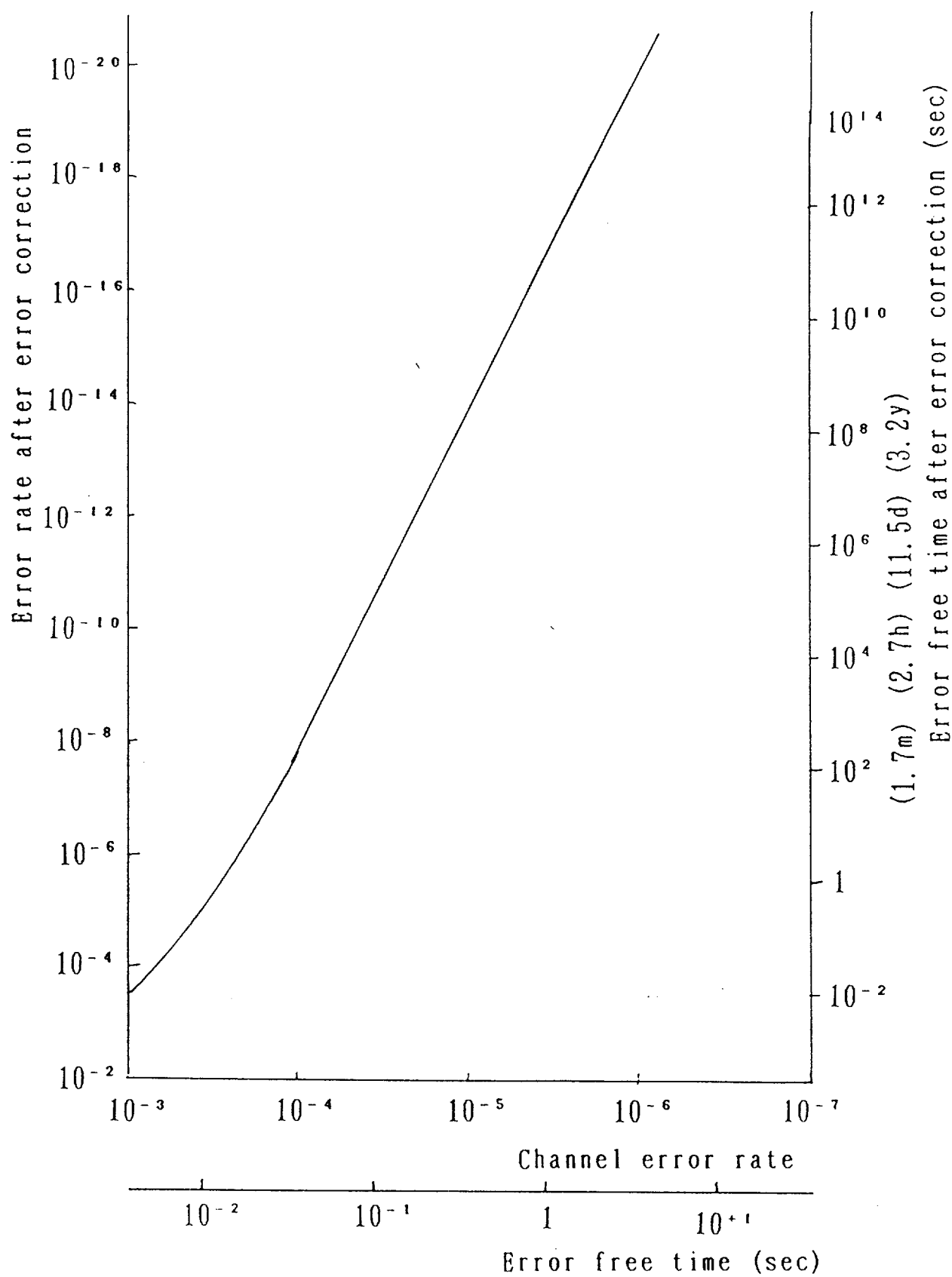


Fig. A.2 Capability of FEC

EXPERIMENTAL PARAMETERS

Discrepancies between Experimental Parameter and Parameter for initial compatibility checks (based on Doc. #249) are summarized as follows:

(1) VLC length for scanning pattern

	Initial compatibility check parameter (#249)	Experimental parameter
Zigzag	1	1
Horizontal	2	2
Vertical	3	4
Fourth	4	3

(bit)

(2) Quantiser for AC and inter mode DC components

Initial compatibility checks:

- . Table 4/#249
- . Step size $Q = 1 \dots 31$

Experimental parameters:

- . Table 1/Annex 4/#254

Level into quantiser	Quantiser index No.	Reconstruction level into inverse transform
$D < -T_{69}$	-69	-R69
\vdots	\vdots	\vdots
$\begin{matrix} -T_{2i+2} \\ -T_{2i+1} \end{matrix} \begin{matrix} \wedge \\ \vee \end{matrix} D \begin{matrix} \wedge \\ \vee \end{matrix} \begin{matrix} -T_{2i+1} \\ -T_{2i} \end{matrix}$	$\begin{matrix} -(2i+1) \\ -2i \end{matrix}$	$\begin{matrix} -R_{2i+1} \\ -R_{2i} \end{matrix}$
\vdots	\vdots	\vdots
$\begin{matrix} -T_3 \\ -T_2 \\ -T_1 \end{matrix} \begin{matrix} \wedge \\ \vee \\ \wedge \\ \vee \\ \wedge \\ \vee \end{matrix} D \begin{matrix} \wedge \\ \vee \\ \wedge \\ \vee \\ \wedge \\ \vee \end{matrix} \begin{matrix} -T_2 \\ -T_1 \\ T_1 \end{matrix}$	$\begin{matrix} -2 \\ -1 \\ 0 \end{matrix}$	$\begin{matrix} -R_2 \\ -R_1 \\ R_0 \end{matrix}$
$\begin{matrix} T_1 \\ T_2 \end{matrix} \begin{matrix} \wedge \\ \vee \end{matrix} D \begin{matrix} \wedge \\ \vee \end{matrix} \begin{matrix} T_2 \\ T_3 \end{matrix}$	$\begin{matrix} 1 \\ 2 \end{matrix}$	$\begin{matrix} R_1 \\ R_2 \end{matrix}$
\vdots	\vdots	\vdots
$\begin{matrix} T_{2i} \\ T_{2i+1} \end{matrix} \begin{matrix} \wedge \\ \vee \end{matrix} D \begin{matrix} \wedge \\ \vee \end{matrix} \begin{matrix} T_{2i+1} \\ T_{2i+2} \end{matrix}$	$\begin{matrix} 2i \\ 2i+1 \end{matrix}$	$\begin{matrix} R_{2i} \\ R_{2i+1} \end{matrix}$
\vdots	\vdots	\vdots
$T_{69} < D$	69	R69

where

$$\begin{aligned}
 R_0 &= 0 \\
 R_1 &= [(q+1)/2 * 3/2]t \\
 R_{2i} &= [R_1 + q * (2i - 1)/2]t \quad \left. \vphantom{\begin{aligned} R_0 \\ R_1 \end{aligned}} \right\} \text{ for } i = 1 \dots 17 \\
 R_{2i+1} &= R_1 + q * i \\
 R_{2i} &= R_1 + q * (2i - 18) \quad \left. \vphantom{\begin{aligned} R_0 \\ R_1 \end{aligned}} \right\} \text{ for } i = 18 \dots 39 \\
 R_{2i+1} &= R_1 + q * (2i - 17)
 \end{aligned}$$

$$\begin{aligned}
 T_1 &= [(q+1)/2]t \\
 T_{2i} &= [(R_{2i-1} + R_{2i})/2]t \quad \left. \vphantom{\begin{aligned} R_0 \\ R_1 \end{aligned}} \right\} \text{ for } i = 1 \dots 39 \\
 T_{2i+1} &= [(R_{2i} + R_{2i+1})/2]t
 \end{aligned}$$

[]t : truncation

$$\begin{aligned}
 &\text{. Step size } Q = 7/2 \dots\dots\dots 43/2 \text{ (example values)} \\
 &\quad \left(\begin{array}{ll} \text{Step size } Q = [(q-1)/2]t \text{ or } [(q+1)/2]t & : \text{ if } q \text{ is odd} \\ \text{or } Q = [(q+1)/2]t & : \text{ if } q \text{ is even} \end{array} \right)
 \end{aligned}$$

(3) VLC length for Tcoeff

Initial compatibility checks:

. Table 5/#249

Experimental parameters:

- . Length for V6 and V-6 of Tcoeff (a) and V-6 and V7 of Tcoeff (b) are 6 bit instead of 16bit.
- . Maximum Tcoeff level is V+69 insted of V+101.

(4) Video data buffer size

Initial compatibility checks:

- . Maximum size of the transmission buffer at the transmitter side is 64 kbits for 1 * 384 kbit/s transmission rate.

Experimental parameters:

- . 256 kbits data buffering is available even for 1 * 384 kbit/s transmission rate. These buffer storage state will occurred when scene is changed or rapid motion scene appeared.
- . For the ordinal scene the amount of the buffer storage quantity at the transmitter side is controlled to hold around 20 kbits.

(5)VLC length for Type 3 mode indication

	Type 3	Initial compatibility check parameter	Experimental parameter
Lumiance	1	5	2
	2	2	2
	3	4	8
	4	5	8
	5a	5	8
	5b	5	8
	5c	5	5
	5d	4	3
	6a	5	8
	6b	3	8
	6c	5	4
	6d	3	2
	7	6	8
Chrominance	1	4	2
	2	1	1
	3	3	8
	4	2	8
	7	-	8

(bit)

Annex 5 / Document #254

Pictures Processed by the Other Type of Flexible Hardware

Demonstrated pictures are processed under the condition as bellow.

- a) Intra/inter(no MC) is adaptively selected on block by block basis.
- b) Periodical refreshment is done by intra GOB.
- c) Frame rate is fixed at 15 frames per second.
- d) Step size of quantizer is also fixed except intra frame DC coefficient:
 - 1) at 4 in Sequence 1 , and
 - 2) at 31 in Sequence 2 .