CCITT SGXV Working Party XV/1 Specialists Group on Coding for Visual Telephony

SOURCE: NTT, KDD, NEC and FUJITSU TITLE: INTELLECTUAL PROPERTY

## I. Formal statement on patent policy

In response to the request (Section 8/Doc. #216R) made at the previous meeting, the four organizations in the source are ready to submit signed documents to the CCITT secretariat according to the proforma in Annex 4/Doc. #216R, if other members also do so.

## II. Disclosed patent on loop filter

JP 61-288678(A) was disclosed December 1986, which is relevant to the loop filter. It was originally invented to reduce quantization noise with non-linear temporal filter in the loop, which is controlled by the vector quantization index. In the claims, however, the filter is expressed in a more general term 'means to reduce quantization noise' and motion vector control of that means is also described.

(54) QUANTIZING NOISE SUPPRESSING SYSTEM IN INTERFRAME CODING

(11) 61-288678 (A)

(43) 18.12.1986 (19) JP

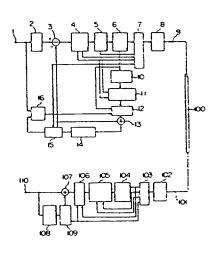
(21) Appl. No. 60-131526 (22) 17.6.1985

(71) NIPPON TELEGR & TELEPH CORP < NTT > (72) HIDEO KURODA(1)

(51) Int. Cl. H04N7/137

PURPOSE: To improve the S/N by controlling suitably the non-linear circuit to suppress the quantizing noise to the television signal including the quantizing noise by using the index information and the optimum dynamic vector information

CONSTITUTION: To a digitalized input television signal 1, a forcasting signal is constituted by using before one field or above, and a forcasting error signal to the input signal is coded and transmitted by the processing or the block unit. By applying the coding data sent at the receiving side to a forcasting signal, the signal is reproduced and the quantizing noise of the reproducing picture is suppressed. Then, a dynamic vector detecting circuit 16 supplies the optimum vector information to show the optimum block to a coding allotting circuit 7, a non-linear circuit 12 and a variable delaying circuit 15. The output of the non-linear circuit 12, to which the output of a variable delaying circuit 15 is applied in an adder circuit 13, comes to be a local decoding signal, is stored in a frame memory 14 and next, comes to be the forcasting signal of the frame.



2: delaying circuit. 3: arithmetic circuit. 4: average value separating/regularizing circuit. 5: block identifying circuit. 6.10.104: vector quantizing/coding circuit. 5: buffer memory. 11.105: weighted average value adding circuit. 103: code decoding circuit