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Title : PSEUDOSYNC CODE

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1. Introduction

In designing a practical video multiplexing coder in motion video transmission, we have to be careful to avoid difficulty in detecting sync codes, in particular, PSC codes immediately after power is turned on and/or after switch-over has occurred when switched multipoint connection is introduced. [1]

2. Requirements for Sync Code Detection

In general, requirements for the sync code detection in low bit rate transmission are:

a. Quick detection of first PSC code.
(No serious difficulty or no impossible-to-decode state in transition period.)
b. Stable detection of sync codes after the first PSC is detected.
c. Use of highly efficient VLC code sets.
d. Simple detector hardware.

When decoding operation is in steady state, every code word can be interpreted properly without remarkable hardware complexity increase. However, it is often very difficult to interpret it properly in the transient period.

Quick update is of paramount importance in switched multipoint mode operation. Quick update is realized by quick detection of PSC. Without this capability, one has to allow a full refresh cycle time e.g. 10 seconds for the first picture build-up. Failure in the detection of the first PSC will result in unbearably slow response.

3. Points for Consideration

Currently, sync codes are defined as 15 consecutive zeros followed by a bit '1' with a GOB number taking VLC code words for transform coefficients into consideration. If we assume, in addition to this definition, that no combination of code words for TYPE3, (QUANT2), CLASS, etc. emulates PSC by careful consideration, following two problems are still left for further study.

- Extra Information in Picture Header.
- TCOEFF in Intraframe.

A. Extra Information in Picture Header or GOB Header

If we assume that video frame is recovered whenever a PSC is found, Picture Header preceding the Forced Update frame data should be detected without failure in switched multipoint connection.(cf. Fig. 1) We also assume here that once a PSC or GBSC is detected, detection circuit is switched off for predetermined intervals to cope with that PSC or GBSC is not unique.

If change-over to a new location is made at MCU between PSC and PEI or PEI and Extra Information bits just preceding the Intra-mode frame, the new Picture Header would not be found due to protection capability i.e. skipping of PSC detection during 19 bits after PSC or (3+m)x8 bits after PEI.

In order to avoid this difficulty, frame dropping should be at first evoked possibly with some amount of bits enough to prevent the protection capability from affecting the next PSC detection.

Following points are left for further consideration.

- Whether or not addition of the frame dropping above is automatically evoked at the transmitter, when emptying the transmission buffer as specified with respect to FUR.

- Whether or not detection of the first PSC for Intra-mode is ensured by designing appropriate time differences for FPR, switching, and FUR at MCU.

B. TCOEFF in Intra-mode

Pseudosync codes will frequently appear when DC component is expressed in Intraframe mode with a 9-bit PCM word and possibly followed by an AC component code word with a prefix code (0 0000 0001).

To avoid this difficulty, it is proposed that restriction is imposed on some of FLC words for DC.

For example, following four code words are discarded in the expression of DC components.

0 0000 0000 (no corresponding video level)
0 1000 0000
1 0000 0000
1 1000 0000

Correspondence between code words and DC values should be modified. However, since the input signal dynamic range is limited within 16 and 240, the number of FLC words is enough for representing DC level with 9 bits in Intra-mode if Intra-mode DC component is quantized with step size of 4.

[1] Annex 3/Document #140R (REPORT OF THE SIXTH MEETING IN MONTREAL (JUNE 17-20,1986)

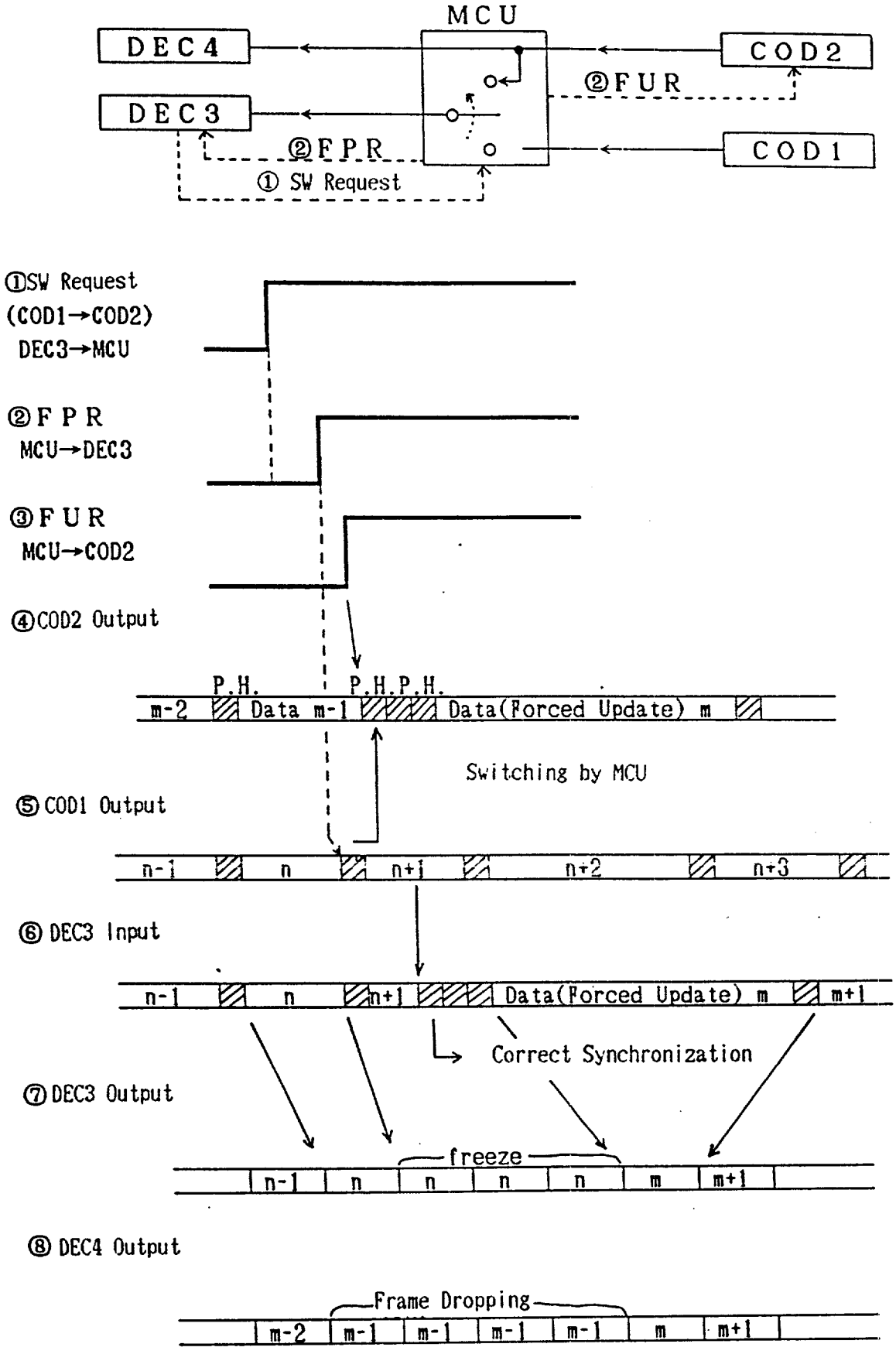

Fig. 1 Switching by MCU