CCITT Study Group XV
Working Party XV/1
Specialists Group on Coding for Visual Telephony

Doc #166
November 1986

Source: UK, Japan, France, FRG, Italy, Netherlands, Sweden

Title: Proposal for the Specification of the Transformer in the Flexible Hardware

At the Montreal meeting in June 1986, the UK and Japan were actioned to finalise the detail of the specification of transform to be used in the flexible hardware. The following proposal is made by Japan and the European members.

Transformer

The forward and inverse transformers shall be implemented in a flexible manner so that a number of different transforms, or configurations of a particular transform in terms of bits per stage, can be investigated. All hardware should be equivalent in performance to classical matrix multiplication.

The 2-D transform is implemented as the equivalent of two independent 1-D transforms.

For the purposes of compatibility it is necessary to specify the inverse transform in sufficient detail that all implementations produce identical numerical output values when given the same input data.

The 64-point 2-D inverse transform is implemented as two independent 8-point 1-D transforms in series. The first 1-D inverse transform operates on the eight vertical sequency components pertaining to a particular horizontal component. The output of the second 1-D inverse transform is pel domain data for eight pels in a horizontal line of the picture.

Each 1-D output point value is formed by multiplying each of the eight input point values by a coefficient and summing the results. The multiplications and accumulation are performed with full precision two's complement arithmetic. The sixty-four coefficients required for all eight ouput points shall be programmable independently and with 16 bits representing values in the range -2 to +32767/16384.

The first inverse 1-D transform operates on 12 bit numbers (from the inverse quantizer) which represent sequency coefficient amplitudes in the range -2048 to +2047.

The 16 bits representing values in the range -1024 to +32767/32 are carried between the output of the first and the input of the second inverse 1-D transforms, the least significant bits being discarded by truncation. Results outside the range of -1024 to +32767/32 are clipped.

The pel domain output of the second 1-D inverse transform is rounded to the 9 bits corresponding to values in the range -256 to +255. The rounding is performed by incrementing the 20 bit of the two's complement value if the 2-1 bit is a '1'. Results outside the range of -256 to +255 are clipped.

End