CCITT SGXV
Working Party XV/1
Specialists Group on Coding for Visual Telephony

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SOURCE: NTT, KDD, NEC and FUJITSU
TITLE : JAPANESE PATENTS RELEVANT TO FLEXIBLE HARDWARE SPECIFICATION

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1. Introduction

At the last meeting in Montreal, each core member was charged to search patents covered by Flexible Hardware Specification and to obtain a statement from holders of those patents.

In Japan, CCITT member organizations were asked to reply the relevant patents they hold by September 30. This document provides a list of such patents and the patent policy of their holders.

2. List of Relevant Patents

2.1 Patents covered by Flexible Hardware Specification

1) JP 57-041069(A) TELEVISION SIGNAL ENCODING EQUIPMENT - NTT
is concerned with the demand refresh method, relevant to Section 3.7 of Specification.

2) JP 60-029068(A)/EP 135255(A) TRANSMISSION ERROR DETECTION SYSTEM - NEC, NTT, FUJITSU
is concerned with the parity check of frame memories between coder and decoder intended for use in demand refresh, relevant to Section 3.7 of Specification.

3) JP 57-199379(A) VECTOR ENCODING DEVICE - NEC
4) JP 60-186180(A) TWO-DIMENSIONAL CODE ALLOCATION SYSTEM FOR DYNAMIC VECTOR - FUJITSU, NTT
are concerned with two-dimensional variable length coding of motion vectors, relevant to Section 2.2.5 of Specification.

2.2 Information on patents concerning motion compensation

The following patents are relevant to motion compensation implementation which is not essential in Specification (Section 1.2.2).

1) JP 55-158784(A) INTER-FRAME CODING DEVICE - NEC
is concerned with a multi-step vector detection method.

2) JP 56-143776(A) INTERFRAME ENCODER - NEC
is concerned with the above + use of the previous-frame vector for prediction.

3) JP 57-037988(A) TELEVISION SIGNAL ENCODING EQUIPMENT - NEC
is concerned with matching error accumulation method using quantized values.

4) JP 58-107785(A)/US 4460923(A)/CA 1175557(A) ENCODER BETWEEN MOVEMENT COMPENSATION FRAMES - NEC
is concerned with the use of forced simple interframe mode.

5) JP 60-146588(A)/EP 150935(A) SYSTEM AND DEVICE FOR ENCODING ANIMATION PICTURE SIGNAL - NEC
is concerned with the halting of motion compensation in case of update operation.

2.3 Abstract of each patent

See Annex. They are reproduction from a data base.

3. Patent Policy

The patent policy of the organizations in the source of this document is as follows;

As far as compatibility is concerned, they can grant non-exclusive licenses on fair and reasonable terms.

4. Precise Terms of Licensing

We discussed how to reply Question 3 ' If yes to 2, what will be the precise terms of such license (royalty fees, initial payments etc.)?'. Difficulty was felt, however, to declare such terms in a one-sided way.

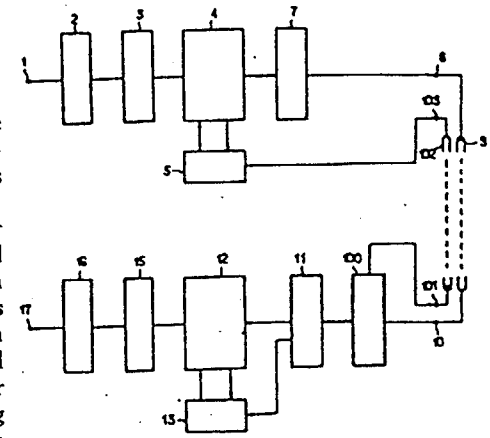
End

Annex

(54) INTER-FRAME ENCODING SYSTEM
(11) 57-41069 (A) (43) 6.3.1982 (19) JP
(21) Appl. No. 55-116571 (22) 25.8.1980
(71) NIPPON DENSHIN DENWA KOSHA (72) HIDEO KURODA(1)
(51) Int. Cl³. H04N1/00,H04N1/40//H04B12/04,H04L1/00

PURPOSE: To get rid of influence by a code error without transmitting a true value of a picture element, by setting the contents of both frame memories at the transmission and receiving sides, to the same prescribed value, in case a code error has been detected by a code error detecting circuit provided at the receiving side.

CONSTITUTION: A code error detecting circuit 100 detects whether a code errier exists or not in a digital signal sequence which is inputted through a digital signal input terminal 10, and sends out its detection signal to the transmission side. As a result, the transmission side executes the inter-frame encoding, setting the contents of a frame memory 5 to a prescribed value, in the next 1 period, and applies a frame memory setting signal to the head of an encoding data of this 1 frame, and sends it out to the receiving side. When it is detected by an output stage of a buffer memory 11 that this frame memory setting signal has been received, the receiving side makes the contents of a frame memory 13 of the 1 frame period coincide with those of the frame memory 5.

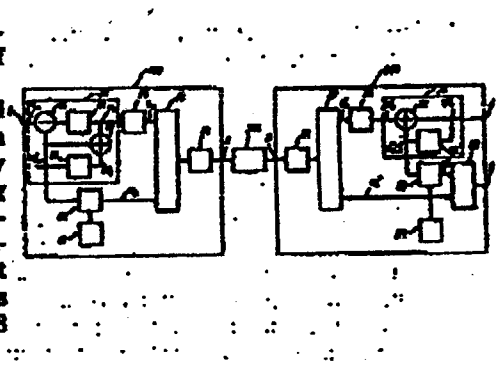


2: low band three-wave circuit, 3: A/D converting circuit, 4: inter-frame encoding processing circuit, 7: buffer memory, 12: inter-frame decoding processing circuit, 15: D/A converting circuit, 16: low band three-wave circuit

(54) TRANSMISSION ERROR DETECTION SYSTEM
(11) 60-29068 (A) (43) 14.2.1985 (19) JP
(21) Appl. No. 58-106806 (22) 16.6.1983
(71) NIPPON DENKI K.K.(2) (72) MITSUO NISHIWAKI(5)
(51) Int. Cl⁴. H03M13/00,H04B14/06

PURPOSE: To securely detect transmission errors by adding redundant bits, collating and comparing the surplus of a forecast encoder between frames with that of a forecast decoder between frames.

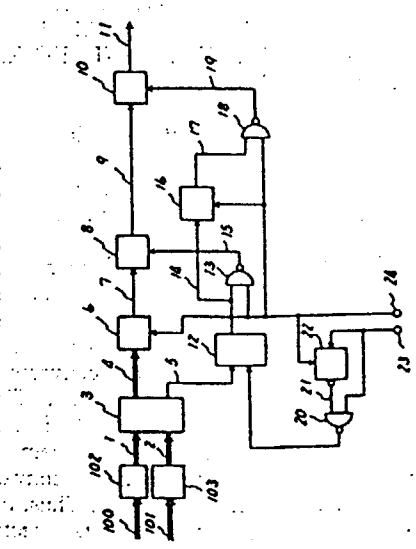
CONSTITUTION: A digital TV signal a_n is inputted from an input terminal 1, and a substracter 11 calculates the difference of a_{n-1} stored in a memory 14. An arithmetic circuit 15 sorts forecast values which are read out from the memory 14 into the prescribed bit group, divides numbers of bits of the logic 1 existing in each bit group by the prescribed value and calculates the surplus r_k. This surplus r_k is multiplied by forecast errors and transmitted to a forecast decoder between frames 200. The decoder 200 separates the surplus r_k in a separate circuit 22. On the other hand, an arithmetic circuit 26 calculates r_k from forecast errors stored in a memory 25 in the same manner of the circuit 15. A comparator 28 compares r_k' with r_k'', thereby detecting transmission errors.



(54) VECTOR ENCODING DEVICE
(11) 57-199379 (A) (43) 7.12.1982 (19) JP
(21) Appl. No. 56-84028 (22) 1.6.1981
(71) NIPPON DENKI K.K. (72) AKIRA HIRANO
(51) Int. Cl³. H04N7/13//H04B12/04

PURPOSE: To efficiently encode a two-dimensional signal displayed by a vector, by giving a code having code length corresponding to magnitude of the vector, to the vector converted to a prescribed vector.

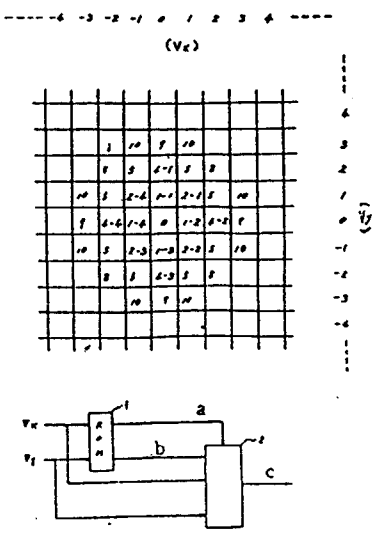
CONSTITUTION: An input vector is inputted to a vector transducer 102 and 103, is converted to a differential signal against a vector value inputted in the past, and is provided to a transducer 3. In the transducer 3, a code of short code length and a code of long code length are provided to a vector whose absolute value is small, and a vector whose absolute value is large, respectively, and are provided to a series/parallel transducer 6. A variable length code output converted in parallel in the transducer 6 is written in a buffer memory 10, after a dummy bit has been removed by a timing pulse for removing the dummy bit provided from an NAND gate 13 in a register 8. In this way, a vector signal can be encoded efficiently.



(54) TWO-DIMENSIONAL CODE ALLOCATION SYSTEM FOR DYNAMIC VECTOR
(11) 60-186180 (A) (43) 21.9.1985 (19) JP
(21) Appl. No. 59-42709 (22) 6.3.1984
(71) FUJITSU K.K.(1) (72) KIICHI MATSUDA(3)
(51) Int. Cl⁴. H04N7/137

PURPOSE: To improve the transmission efficiency of an optimum dynamic vector transmission system during motion compensation predictive encoding operation by assigning and transmitting variable length codes with code length which is made shorter according to arrangement points where dynamic vectors converge more.

CONSTITUTION: When the horizontal vector Vx and vertical vector Vy of a dynamic vector are inputted, norm values are detected in memory 1 and a corresponding transmission code is transmitted by a multiplexing circuit 2. Norm values of the dynamic vectors are arranged around a reference point (norm value "0") in two dimensions and variable codes having shorter bits according to closeness to the reference point are assigned as transmission codes, so information on the dynamic vector is transmitted with less bits.

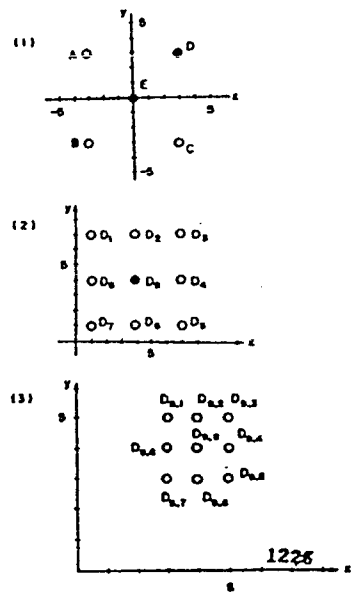


a: control signal, b: transmission code, c: transmission code output

(54) INTER-FRAME CODING DEVICE
(11) 55-158784 (A) (43) 10.12.1980 (19) JP
(21) Appl. No. 54-65853 (22) 28.5.1979
(71) NIPPON DENKI K.K. (72) AKIRA HIRANO
(51) Int. Cl³. H04N7/12,H04N7/13

PURPOSE: To reduce the necessary amount of operation by carrying out the detection of the dynamic vector in multiple steps.

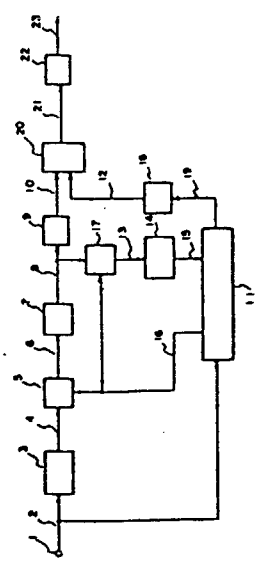
CONSTITUTION: The evaluating function is obtained at the 1st step for the 1st shift vector group which is displayed in A, B, C, D and E each, and then the shift vector featuring the minimum evaluating function is obtained among those in the vector group. Here if D is the vector to be obtained, the evaluating function value is obtained in the same way at the 2nd step for 2nd shift vector groups $D_1 \sim D_9$ which are distributed near D. And then the shift vector featuring minimum evaluating function is obtained among the 2nd shift vector groups. And if D_9 is minimum, the evaluating value is obtained at the 3rd step for 3rd shift vector groups $D_{9.1} \sim D_{9.9}$ which are distributed near D_9. Then the shift vector featuring the minimum evaluating function is obtained. And if $D_{9.5}$ features the minimum value, $D_{9.9}$ is decided as the dynamic vector to the block. In this case, the signal of the preceding frame is shifted by vector $D_{9.5}$ to be used as the predicting signal. Thus the differential signal of this predicting signal and the present-frame signal plus shift vector $D_{9.5}$ are coded in the form of the dynamic vector to be transmitted.



(54) INTERFRAME ENCODER
(11) 56-143776 (A) (43) 9.11.1981 (19) JP
(21) Appl. No. 55-46666 (22) 9.4.1980
(71) NIPPON DENKI K.K. (72) AKIRA HIRANO
(51) Int. Cl³. H04N7/13

PURPOSE: To reduce arithmetic quantity of an estimating function by detecting dynamic vectors, showing the motion of a TV picture, in multiple steps.

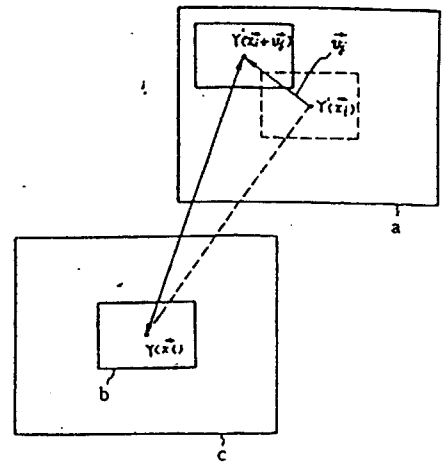
CONSTITUTION: A TV signal inputted from terminal 1 is supplied to subtracter 5 to get its difference from a forecast signal outputted from forecast signal generation part 11, and this difference (forecasted error signal) is inputted to quantitizer 7, encoder 9 and adder 17. Forecast signal generation part 11 detects dynamic vectors from the input TV signal and a one-frame preceding signal inputted from frame memory 14 and then outputs the forecast signal to signal line 16. The dynamic vectors outputted to signal line 12 and encoded are multiplexed at encoded forecasted error signal 10 and multiplexer 20 and the resulting signal is sent to signal line 21.



(54) TELEVISION SIGNAL ENCODING EQUIPMENT
(11) 57-37988 (A) (43) 2.3.1982 (19) JP
(21) Appl. No. 55-111265 (22) 13.8.1980
(71) NIPPON DENKI K.K. (72) AKIRA HIRANO
(51) Int. Cl³. H04N7/12,H04B12/00

PURPOSE: To perform efficient adaptive forecasting encoding by comparing levels of the picture element of the previous frame and that of existing frame and numerically expressing the difference.

CONSTITUTION: The levels of the picture element of the previous frame and that of existing frame of television signals are compared and degree of the difference is divided into ≧3 groups. Degrees having small difference are seperated into small groups and those having large difference are seperated into large groups. Then, one value is given to respective group according to the magnitude. That is to say, small values are given to small groups and large values are given to large groups. In this way, the numerically expressed values are integrated for picture elements within each block to obtain the evaluated values. Encoding is performed by obtaining optimum forecasting signal based on the evaluated values. Therefore, efficient adaptive forecasting encoding can be performed.

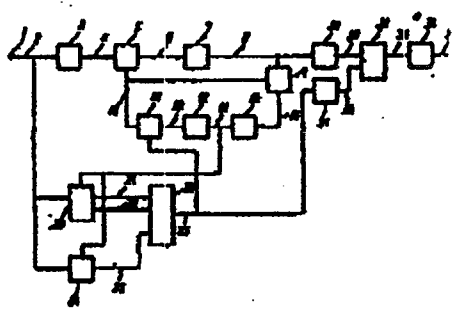


a: previous frame, b: block of existing frame, c: existing frame

(54) ENCODER BETWEEN MOVEMENT COMPENSATION FRAMES
(11) 58-107785 (A) (43) 27.6.1983 (19) JP
(21) Appl. No. 56-206624 (22) 21.12.1981
(71) NIPPON DENKI K.K. (72) AKIRA HIRANO
(51) Int. Cl³. H04N7/12

PURPOSE: To reduce the deterioration of picture quality generated from the movement compensation remarkably, by comparing an evaluation value to a dynamic vector detected once with an evaluation value to a shift vector, and estimating inter-frame when the difference is a prescribed value or below.

CONSTITUTION: A TV signal inputted to a terminal 1 is applied to a delay circuit 3, a dyanmic vector detector 20 and an inter-frame evaluation operator 24. An output of the delay circuit 3 is subtracted from an estimation signal from a variable delay circuit 14 at a subtractor 5 and an estimation error signal is given to a quantization device 7. An estimation error signal quantitized is encoded at an encoder 30 and applied to a terminal of a multiplexer 34. An evaluation value of a dynamic vector detected at a dynamic vector detector 20 is applied to a discrimination circuit 36 together with an evaluation value to a shift vector detected at the device 24, and the difference of the both is discriminated and a corrected dynamic vector is obtained. This signal is encoded 31 and applied to the multiplexer 34, and multiplexed with the estimation error signal for output.



(54) SYSTEM AND DEVICE FOR ENCODING ANIMATION PICTURE SIGNAL
(11) 60-146588 (A) (43) 2.8.1985 (19) JP
(21) Appl. No. 59-2913 (22) 11.1.1984
(71) NIPPON DENKI K.K. (72) JIYUNICHI OOKI
(51) Int. Cl⁴. H04N7/137

PURPOSE: To rewrite a screen securely regardless of whether motion occurs or not and its direction by performing interframe predictive encoding while regarding information on the motion as "0" for a predetermined time as to a part where the screen is rewritten.

CONSTITUTION: A digital television signal is supplied from an input signal line 1 to an interframe encoder with motion compensation. A refreshing circuit 2 generates a refreshing execution signal and a motion compensation inhibiting signal and supplies them to the interframe encoder 5 to control the execution and stop of refreshing and motion compensation. Lines for which refreshing is designated are encoded without interframe prediction and once the refreshing is carried out, predictive encoding is carried out with the motion compensation inhibiting signal while it is considered that there is not any motion at all for a prescribed period, e.g. N-line period. Consequently, the movement and expansion of an error occurring in the endocing are removed.