CCITT SGXV
Working Party XV/1
Specialists Group on Coding for Visual Telephony

Document #115

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SOURCE: NTT, KDD, NEC and FUJITSU
TITLE : COMMENTS ON DIGITAL INTERFACE FOR n x 384 kbit/s CODEC

Frame structure and user-to-network interface for 2048 kbit/s was proposed by Document #77 (F.R.G.) at the last Tokyo meeting, and corresponding proposals were requested of countries using 1544 kbit/s.

This document discusses only

- time slot assignment for H0 channels, and
- indication bit for remote synchronous/asynchronous switching

for 1544 kbit/s. The other aspects should conform to existing Recommendations G.703, G.704 and I.431.

1. Time Slot Assignment for H0 Channels

The following assignment described in ANNEX A/I.431 is used.

H0 channel	a	b	c	d
Time slots used	1 to 6	7 to 12	13 to 18	19 to 24 *

* This fourth H0 channel is available if time slot 24 is not used for a D or an E channel.

For the case of $n \geq 2$ operation, the following proposals made in Document #77 are supported.

- A group of n adjacent H0 channels is used.
- Only the leftmost channel of the group can carry an audio/service signal.

2. Indication Bit for Remote Synchronous/asynchronous Switching

Though Document #77 proposed the use of outslot signalling for this purpose, we propose to start with the inslot signalling approach, which was also suggested in that document, because

- there is no capacity room in the 'F' bit of 1544 kbit/s, and
- use of 'F' bit, especially 'm' bit is being studied in SG XVIII.

We will have a chance to reconsider this point when the matter will be settled in SG XVIII.

3. Consideration on Compatibility Check at Laboratories

A typical international connection is illustrated in Figure 1. Since different interfaces are used in two regions, the two codecs can not be interconnected directly at laboratories.

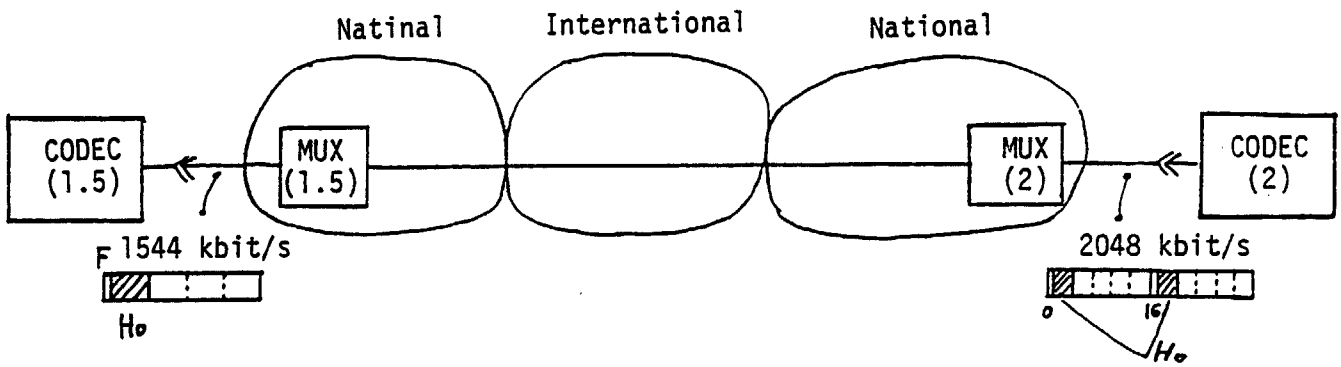
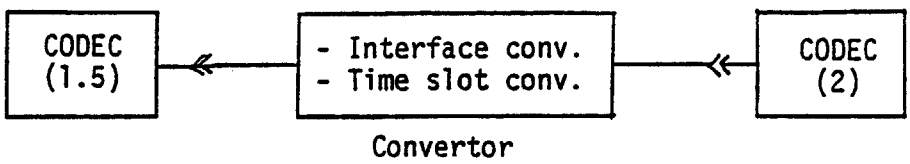
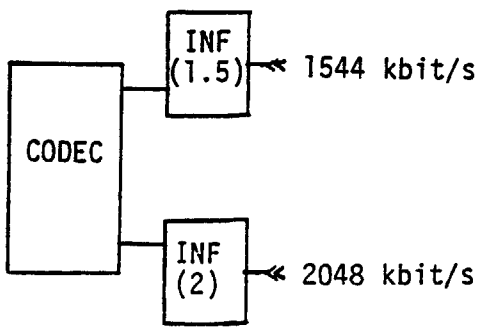


Figure 1 An interregional connection

To cope with this problem, we should take either of the two measures shown in Figure 2.



A) Provision of an interface and time slot convertor simulating MUX(1.5) - MUX(2) in Figure 1



B) Provision of two interfaces at the codec

Figure 2 Compatibility check at laboratories