ITU Telecommunication Standardization Sector
Study Group 15
Experts Group for Video Coding and Systems
in ATM and Other Network Environments

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Title: Transfer rate for H.310 terminals
Purpose: Discussion

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1. Introduction

One of the open issues for the specifications of H.310 is the transfer rate of the terminal, which is currently specified as "nx64 kbit/s" where n is a 16 bit natural number (1 - 65535) [1]. The question is whether further quantization is required from implementation point of view [2].

This contribution reviews some methods to reproduce multiple rate clocks in a step of 64 kHz in the receiving terminal and concludes that though the current representation of the transfer rate is appropriate, further study is needed for whether any value of n be mandatorily supported by the H.310 terminal.

2. Model for the receiving terminal

CBR service and use of the adaptive clock method for reproducing transmission clock are assumed here. A model for the receiving terminal is shown in Figure 1 [3].

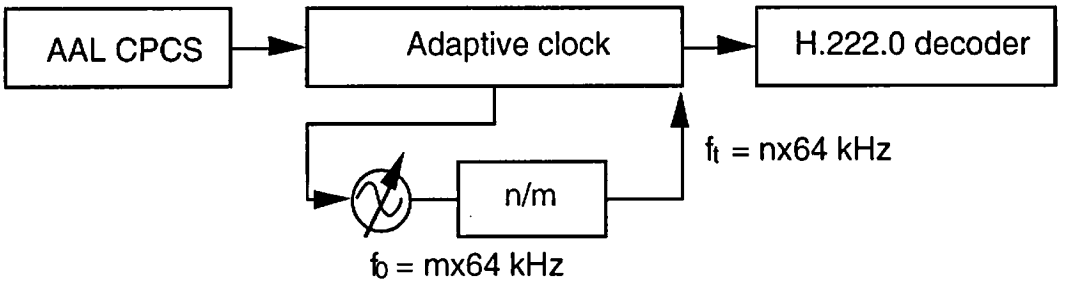

Figure 1 Model for the adaptive clock decoder

The VCXO has its frequency of f_0 = mx64 kHz which gives a desired ft = nx64 kHz through the "n/m" multiplier circuit. If the VCXO has frequency of 36864 kHz (m=384), foe example, the "n/m" processing can be simple dividing for

n=1, 2, 3, 4, 6, 8, 9, 12, 16, 18, 24, 32, 36, 48, 64, 72, 96, 144, 192, 288, 576,

but intermediate values need some more processing. If the transfer rate of H.310 terminals is restricted to such numbers, then the decoder implementation can be simpler.

3. Implementation of "n/m" processing

There are some methods to obtain any value of n.

1) Phase comparison at 64 kHz

Figure 2 shows a circuit which produces n/m f_0 = nx64 kHz by carrying out phase comparison at 64 kHz. Though the VCO needs to generate a wide range of oscillating frequency, this method can produce any frequency of n multiples of 64 kHz.

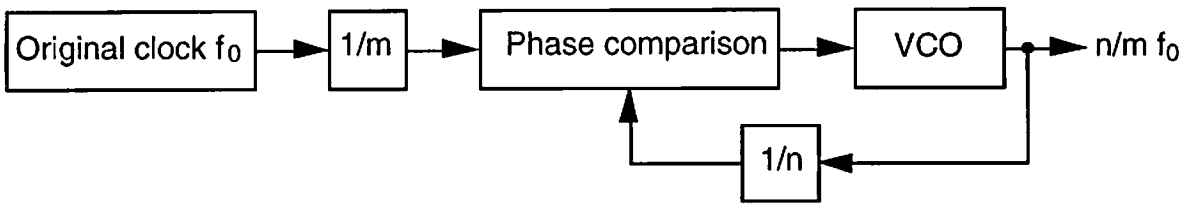

Figure 2 Phase comparison at 64 kHz

2) Allowing some jitter at the clock output

In the example described in Section 2 (m=576), such a value as n = 94 (6016 kHz) cannot be produced by simple dividing. If we allow some jitter at the clock output, however, it can be produced by using an original pulse which is closest to the desired time position as shown in Figure 3. The jitter is within the original clock pulse interval, 27 nanosecond in this example. This value is significantly smaller than the +/- 25 microsecond jitter of the RTI-LJ specification. It is expected that this low value of jitter does not cause problems for the PCR reproduction.

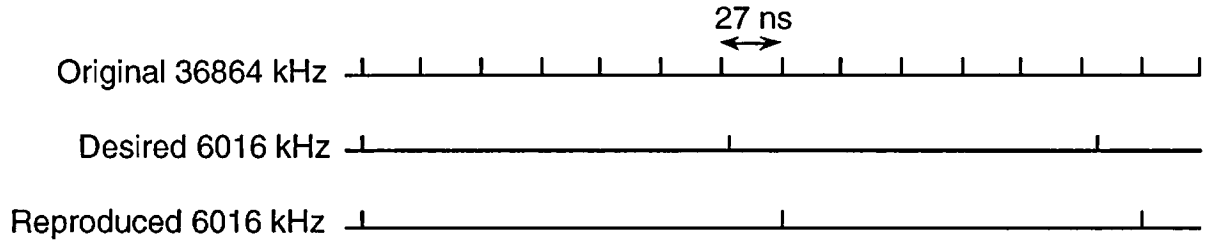

Figure 3 Allowing some jitter at the clock output

3) Using multiple VCXOs

If the range of desired values of n is small, use of multiple VCXOs might be possible.

4. Conclusion

It is considered possible to implement a clock recovery circuit which accommodates any values of n, and appropriate to represent the H.310 transfer rate in terms of nx64 kbit/s. From service definition point of view, we should not place unnecessary restrictions to the transfer rate for future possibilities. However, further study is needed whether H.310 specify that all values of n be mandatorily supported. It is also suggested to study the upper bound of the transfer rate (maximum value of n) for each type of the H.310 terminal.

References

[1] AVC-746 "Draft H.32X (Editor)", March 1995.
[2] AVC-752 "Open Issues towards the Stockholm Meeting (Rapporteur)", March 1995.
[3] AVC-743R "Report of the eighteenth Experts Group meeting in Kamifukuoka, 24-27 January 1995 (Rapporteur), Annex 7, January 1995.

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