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Title: SIMULATION OF PHASE-LOCKED LOOP FOR PROCESSING JITTERED PCRs

Introduction

The problem of recovering a clock which is suitable for composite video reconstruction from the MPEG Transport Stream PCRs when the Transport Stream is carried on a network that introduces jitter (cell delay variation) has been a concern for some time. Now that the MPEG-2 standards work is in its final stages, it is becoming urgent that this problem be addressed thoroughly. There have been only two contributions which address the problem in a quantitative manner [1,2]. This contribution supplements those two by giving more detailed results for a different PCR processing circuit.

The contribution contains simulation results of a second order phase-locked loop with phase error averaging. The parameters tracked are loop output frequency, changes in the loop output frequency (i.e. frequency change step size), and total phase error between the reconstructed and incoming PCRs. The last parameter gives a measure of how much extra buffering is needed to absorb loop transients.

Simulation Description

The PLL is a standard second order digital phase-locked loop with phase error averaging (see Figure 1). Phase-locked loops will not be described here - they are well covered in the literature [3,4,5]. When the averaging is disabled (i.e. N=1 in Figure 1), the damping factor is 0.706. Also when N=1, the proportional time constant is 25.65 seconds, and the integral time constant is 51.2 seconds. For Figures 2 to 4, N=256. For Figure 5, N=128. Phase error averaging tends to reduce the effective damping factor below the value for N=1.

The simulation uses floating point calculations. The large jitter should swamp loop truncation errors. Results are in normalized units; all frequency differences are given in parts per million (ppm) and all phase measurements are given in fractions of seconds. Each simulation run was

for 1000 seconds, with variables plotted every second. Maxima were monitored every cycle. The simulation loop runs at 10 Hz (simulation time). A PCR arrives and the output frequency is updated every cycle (i.e. the PCR rate and oscillator update rate are both 10 Hz).

Input Parameters

Network performance requirements for at least one major network type (ATM) are still under discussion. Various frequency accuracy requirements apply to different applications. The inputs chosen for this simulation are intended to present a moderately severe test of the performance of the PCR processing circuit. A maximum frequency offset of 50 ppm is used, and the jitter is assumed to be 1 millisecond peak-to-peak, uniformly distributed. Initial phase error can be up to one half the peak-to-peak jitter i.e. 500 microseconds.

Results

The various test runs are shown in Figures 2 to 4, which are annotated with the input conditions. Figure 2 has combined phase offset, frequency offset, and jitter. Figure 3 has phase offset and jitter only. Figure 4 has negative phase offset and frequency offset. The figures show that:

Major pull-in transients are over after about two minutes.
Frequency deviation after pull-in is generally less than 2 ppm.
Frequency excursions due to overshoot or initial phase offset can be as large as 25 ppm.
Frequency steps during pull-in are less than 0.3 ppm, and after pull-in are less than 0.2 ppm.
Maximum total phase error is about 1.3 milliseconds.

Discussion

These results are encouraging. The phase-locked loop design is simple and almost standard. The major addition is the phase error averaging, which is easily implemented. All divisions are by powers of 2, so they can be implemented with bit-shifts. The extra buffering required is about 3 milliseconds (for +/- 1.5 ms), plus the buffering needed to accommodate the jitter (+/- 0.5 ms).

The major deficiency of this PLL is that it has a low damping factor, so pull-in transients are fairly large. The PLL can easily be designed to use a higher damping factor, longer time constants, or less averaging, but more buffering will be required to absorb pull-in transients. This is shown in Figure 5, where the same input conditions as in Figure 2 are processed by a PLL with proportional time constant 51.3 seconds, integral time constant 204.8 seconds and damping factor of 0.999 (all for N=1). N was set to 128 to produce Figure 5. The frequency overshoot in Figure 5a is less than half that in figure 2a even though the frequency step sizes in Figure 5b are slightly smaller than those in Figure 2b. However, the phase error in Figure 5c is 50% larger than that in Figure 2c, and the non-oscillatory transient response in Figure 5 takes much longer to settle out.

More contributions on the expected performance of networks and the needed purity of the recovered clock are required to allow design of an optimized PLL.

References

1. MPEG93/956, M. Perkins and T. Lookabaugh, *Comments on Clock Recovery in the Presence of Jitter*, November 1993.
2. MPEG93/697, J Tiernan and F. Harris, *Clock Recovery Using Timestamps*, October 10, 1993
3. William C. Lindsey, *A Survey of Digital Phase-Locked Loops*, Proc. IEEE, April 1981, vol. 69, no. 4, pp. 410-431.
4. Floyd M. Gardner, *Phaselock Techniques*, 2nd ed. 1979, John Wiley and Sons.
5. Roland E. Best, *Phase-Locked Loops*, 2nd ed. 1993, McGraw-Hill.

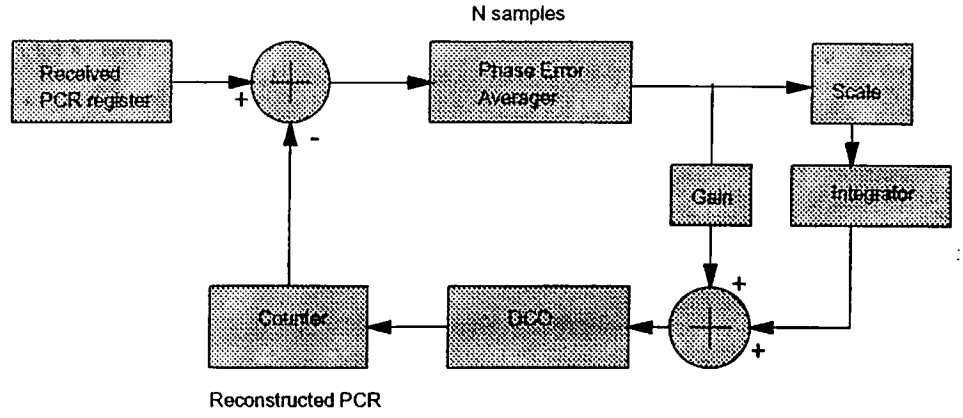

Figure 1. PLL with phase error averaging.

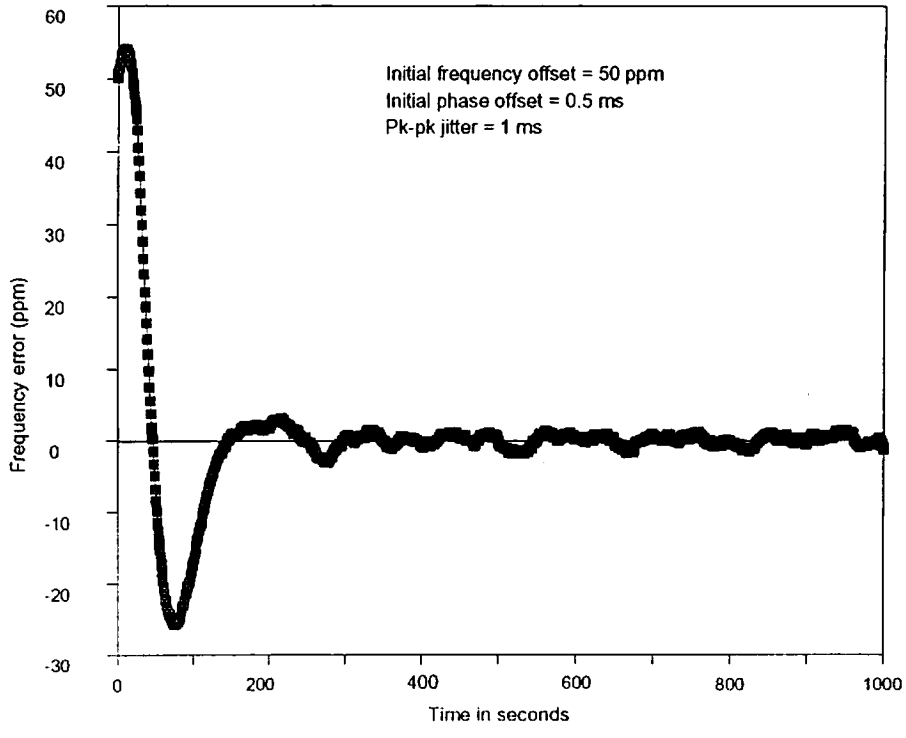

Figure 2a. Frequency response

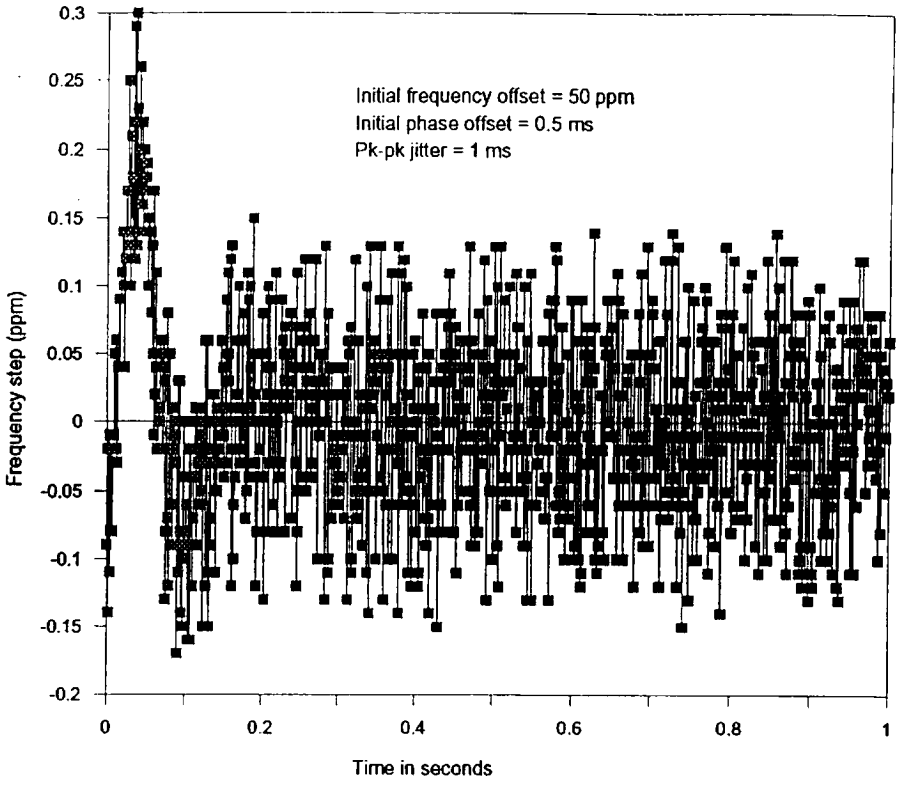

Figure 2b. Frequency change step size

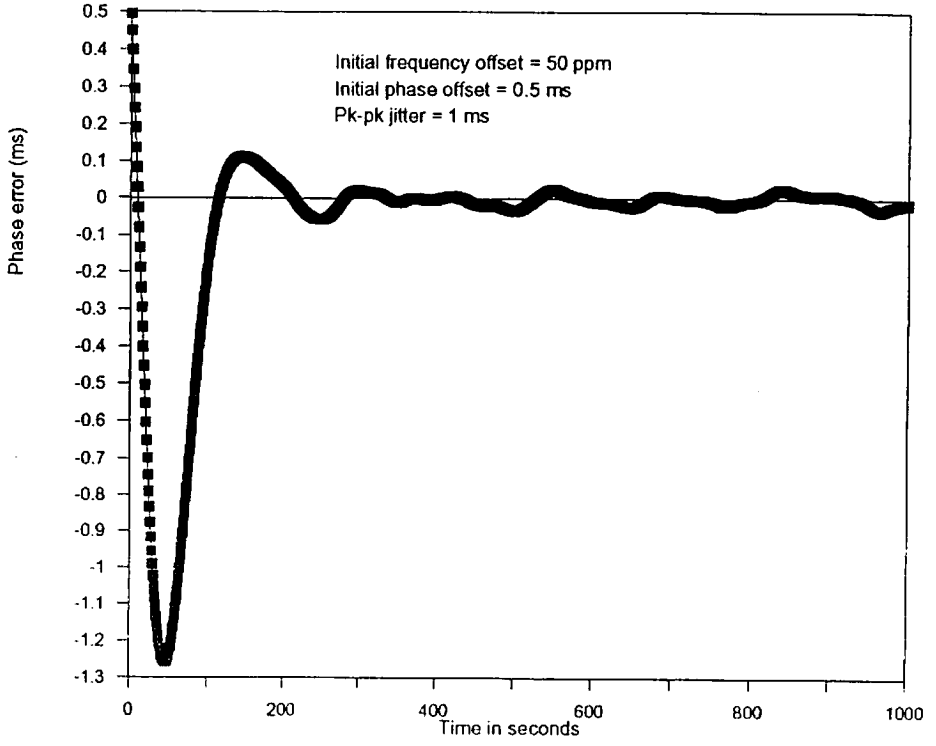

Figure 2c. Phase error

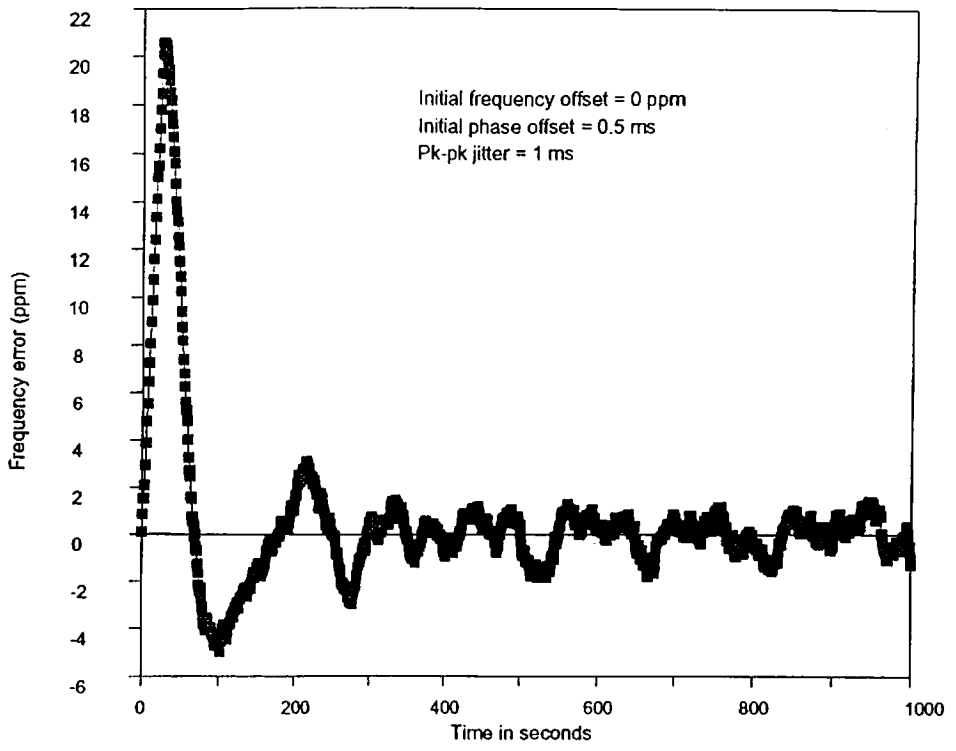

Figure 3a. Frequency response when no initial frequency offset

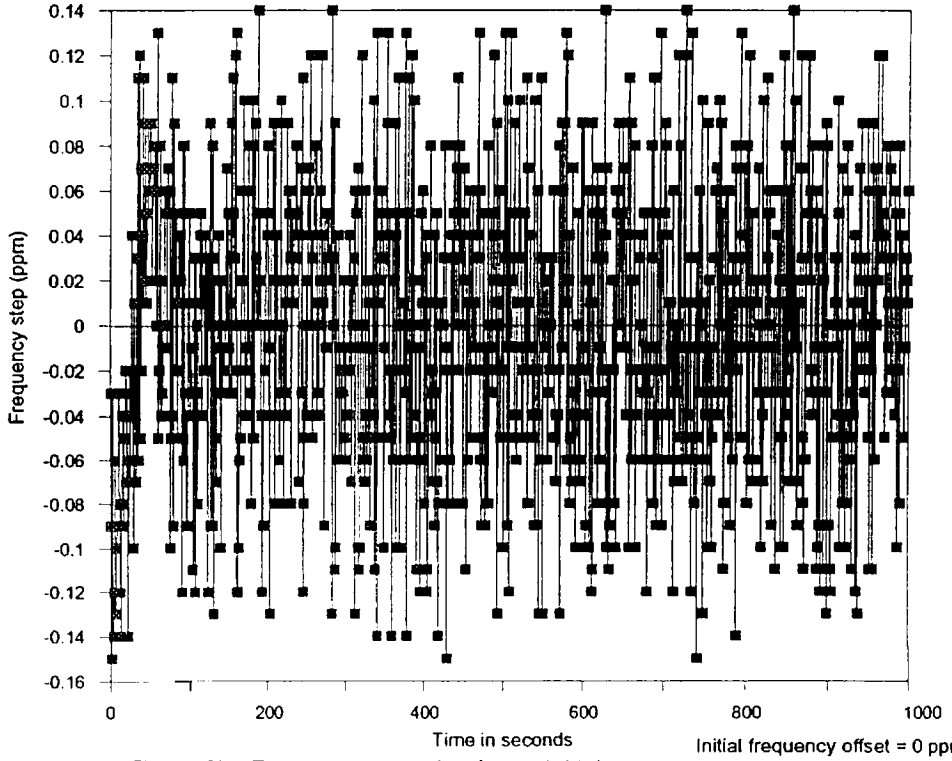

Figure 3b. Frequency step size for no initial frequency offset

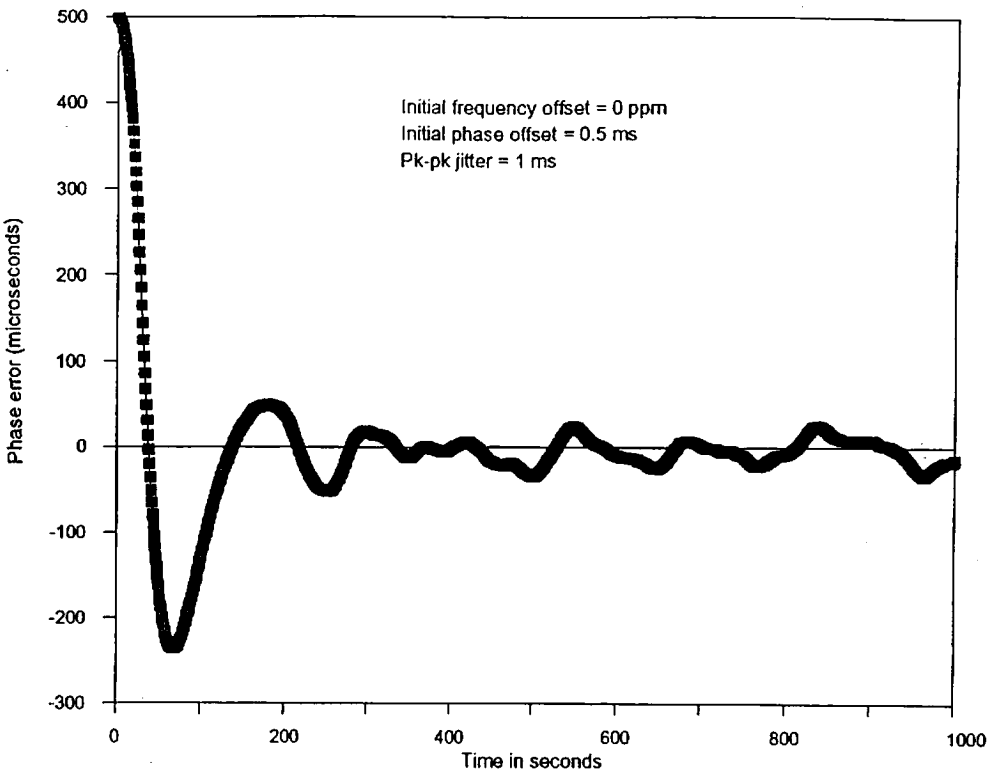

Figure 3c. Phase error for no initial frequency offset

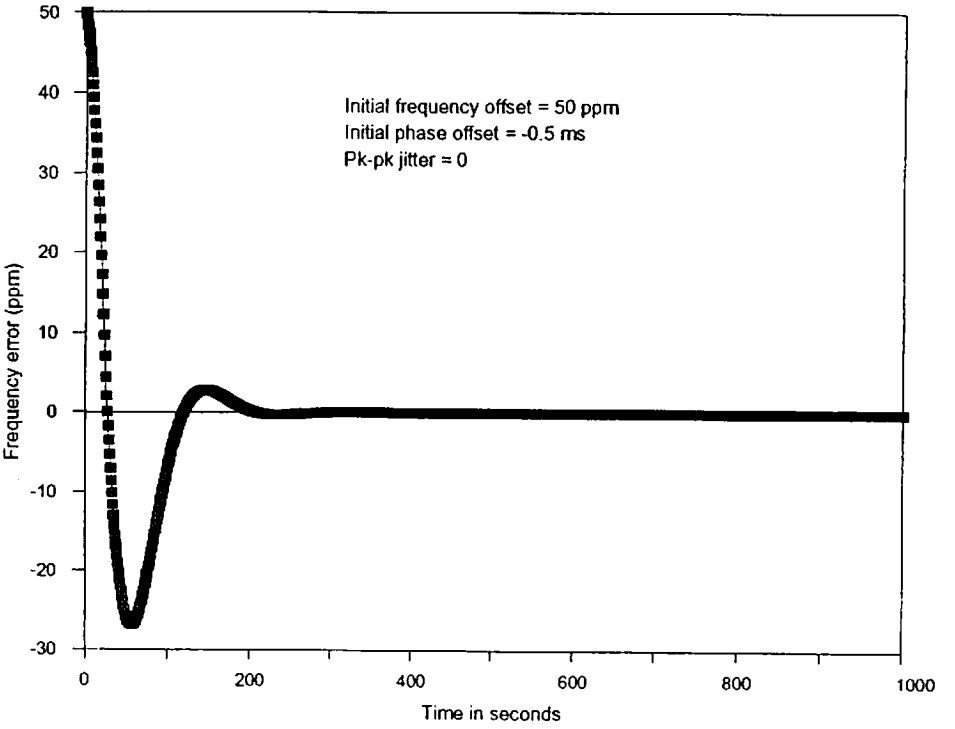

Figure 4a Frequency response for negative phase offset

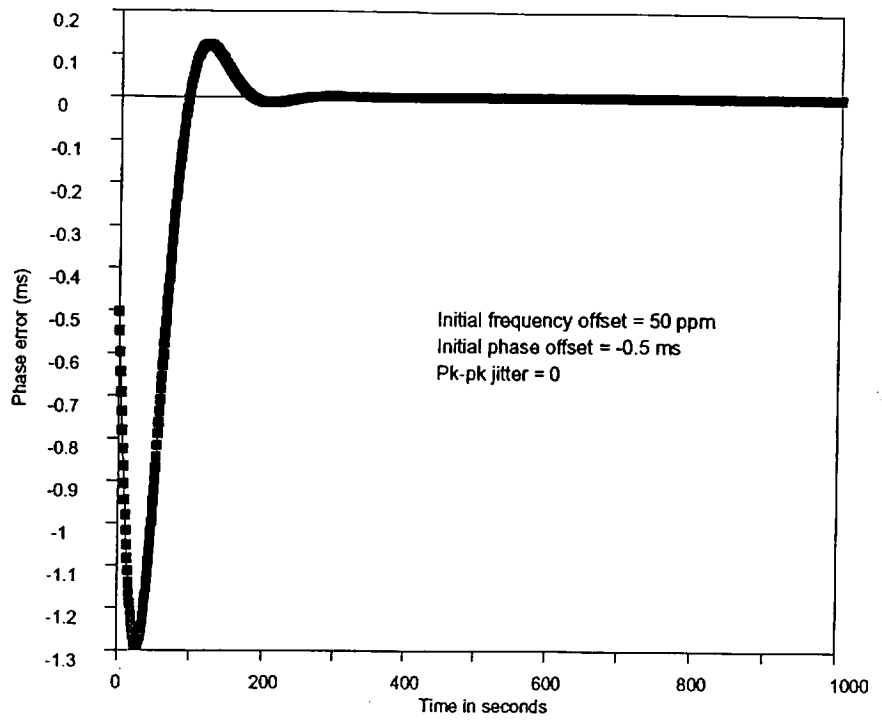

Figure 4b. Phase error for negative phase offset

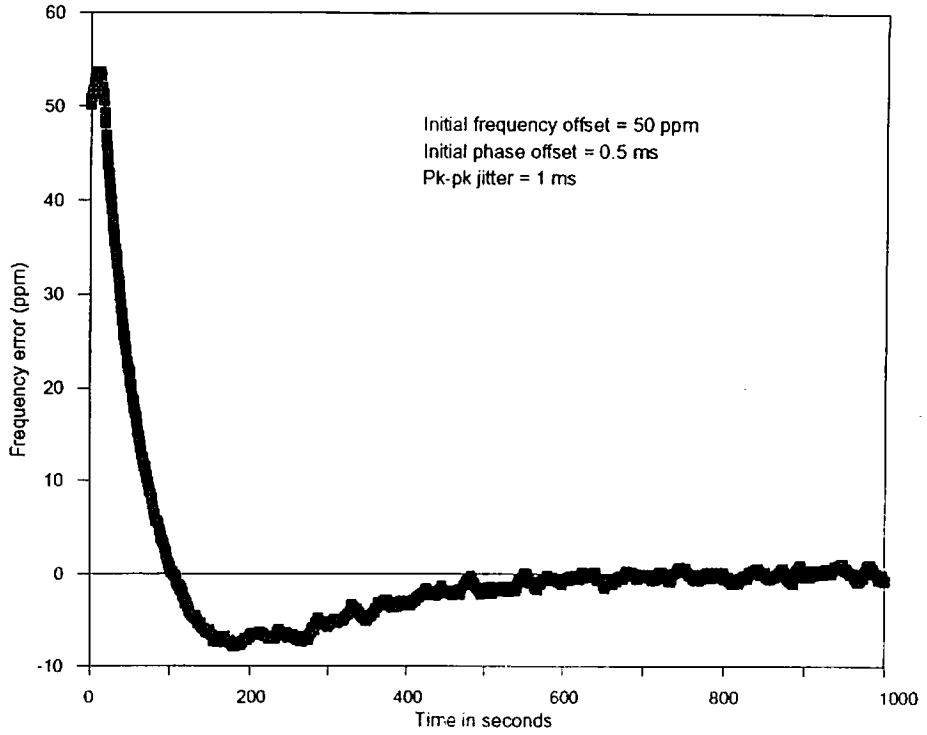

Figure 5a. Frequency error for loop with higher damping factor

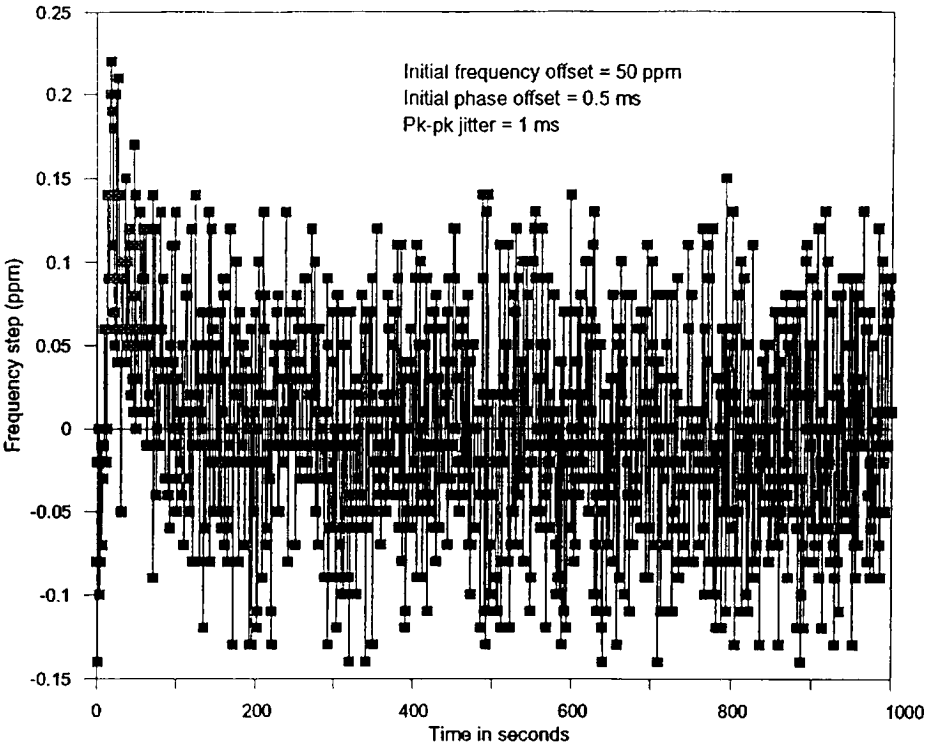

Figure 5b. Frequency change step size for loop with higher damping factor

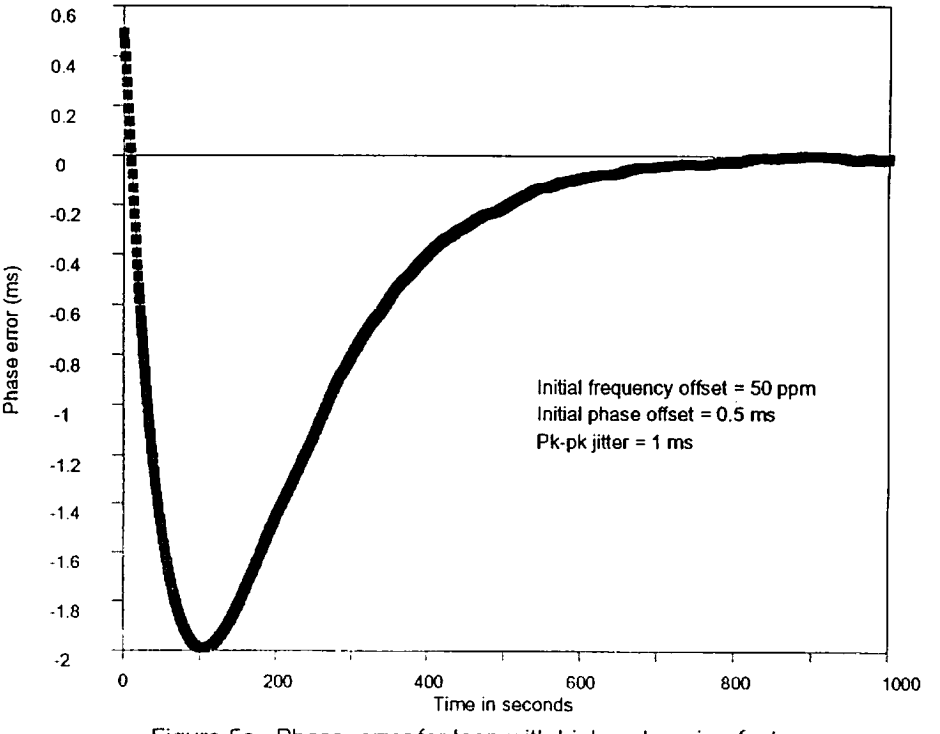

Figure 5c. Phase error for loop with higher damping factor