ISO/IEC JTC/SC29/WG11 MPEG93/747 September 1993

Telecommunication Standardization Sector Study Group 15 Experts Group for ATM Video Coding (Rapporteur's Group on Part of Q.2/15) Document AVC-562 September 1993

Source : JAPAN

Title : Experiment on Asynchronous Video Clock

Purpose: Information

1. Introduction

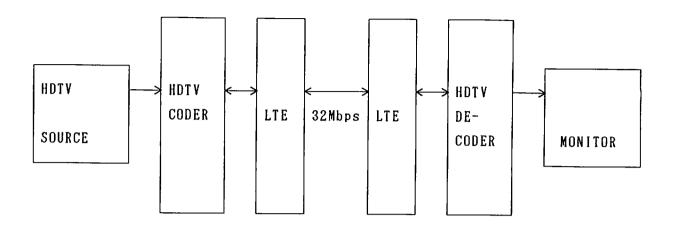
In relation to the video clock, this Experts Group's effort has been concentrated in studying on how to synchronize on both ends with use of time stamp. However, among various applications, synchronization is not always required and seems not to be a serious probolem. It mainly comes from the fact that the precision degree of crystal oscillator has been remarkably improved in recent years. It is especially true for HDTV instruments. Therefore, related mesuremets have been done with a prototype HDTV codec.

2. Experiments

Fig.1 illustrates the block diagram of experiment system. Video sources used are test-pattern generator, camera and video tape recorder. The video signals are encoded and compressed down to 32 Mbps and decompressed on receiving end. The video clock on receiving end is set to the value slightly higher than that of standard. If a field slip takes place on receiving end, the field just prior to that is put out and display order follows Fig.2. When a next field slip occurs, display order returns to normal. Chart 1 shows average field slip values for each signal source and receive—clock setup. Visually, field slips can be noticed under very careful observation in the computer simulation of this motion when a short and repeating source signal is used. But they can be seldom noticed with the experiment system.

3. Conclusion

The HDTV transmission has tried under asynchronous condition of video clock on both ends. As a result of careful visual observation and measurement of field slip interval, asynchronous mode can be satisfactorily a method of some practical use.



LTE: Line Terminating Equipment

Figure 1 Experiment System

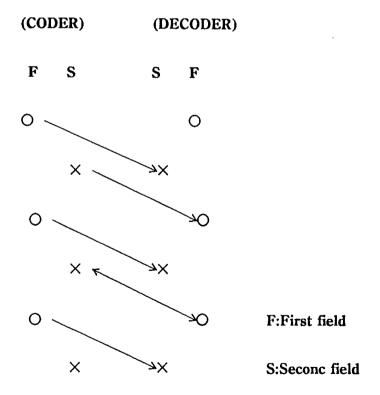


Figure 2 Display Order on a Field Skip

Chart 1 Average Field Slip Interval

source		SIGNAL GENERATOR	CAMERA	FRAME MEMORY
source clock deviati	on	± Зррш	± Зррш	± Зррш
·	+10ppm	26.1 min	28.9 min	27.0 min
decoder clock set-up	+20ppm	14.0 min	13.7 min .	14.0 min
	+30ppm	9.5 min	9.1 min	9.5 min