ITU Telecommunication Standardization Sector
Study Group 15
Experts Group for ATM Video Coding
(Rapporteur's Group on Part of Q.2/15)

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Source: SG13
Title: LIAISON STATEMENTS TO SG15 EXPERTS GROUP FOR ATM VIDEO CODING
Purpose: Report

This document contains the following liaison statements from SG13 which met during 5-16 July 1993 in Geneva;

END

ANNEX 18

(to the report of SG 13)

Q.6/13

SOURCE : Q.6 (AAL1/2) /SG13 (WP 2/6; Geneva meeting, 5-16 Feb 96)

TITLE : Proposed Liaison to SG 15 (ATM Video Group), CMTT/3 and ISO/IEC MPEG ; for information

SUBJECT : AAL Type 1 timing recovery issues

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1. Introduction

The AAL type 1 agreements in I.363 provide two methods of asynchronous clock recovery for the support of CBR services with clocks not locked to a network clock. The two methods are:

- Synchronous Residual Time Stamp (SRTS)
- Adaptive Clock

This Liaison identifies open issues involving the two methods.

2. Synchronous Residual Time Stamp Issues

The SRTS method is designed for the recovery of clocks with restrictive jitter requirements, such as the 2.048 Mbit/s hierarchy requirements in Rec. G.823 or the 1.544 Mbit/s hierarchy requirements in Rec. G.823. The SRTS method assumes a common reference clock is available to the transmitting and receiving AAL1-entities through the B-ISDN SDH physical layer. To allow for degradation or failure of the common clock, SRTS requires a backup method of operation, referred to as Plesiochronous Network Operation, be available to support clock recovery.

Issues associated with further development and extensions of the SRTS method are:

- extending the SRTS method to physical layer access based on existing PDH (i.e., 2.048 Mbit/s and 1.544 Mbit/s) networks;

- developing an understanding of options available for Plesiochronous Network Operation;

- interworking of PDH-based and SDH-based SRTS.

The extension of SRTS to PDH networks is required to support early deployment of B - ISDN technology. Plesiochronous network operation requires study to identify the options available (e.g., adaptive clock) for backing up SRTS operation in the event of reference clock problems. If B-ISDN network connection scenarios in which one physical layer access is SDH and the other physical layer access is PDH are to be supported with SRTS, then methods for interworking PDH-based SRTS with SDH-based SRTS need to be developed.

3. Adaptive Clock Issues

The adaptive clock method of asynchronous clock recovery utilizes the fill level of a receiving buffer as an indicator for the adjustment of a local clock. The main issues associated with the use of the adaptive clock approach are the control of jitter (particularly low frequency jitter below 10 Hz) and buffering delays. These issues can be addressed in the context of specific CBR services.

4. Network Issues

Network level concerns with asynchronous clock recovery also need to be taken into account. The primary concern is to identify how asynchronous clock recovery will be performed for connection scenarios in which a common clock is not available. For example, an international connection where the two national administrations do not share a common clock. This concern leads to two related issues:

- the performance of SRTS clock recovery under the assumption of plesiochronous operation with two different, but accurate and stable network clocks (e.g., assume a difference on the order of 1 in 10^{-11} as given in Rec. G.811 for primary network reference clocks);

- the limits of performance feasible with the adaptive clock method, particularly with regards to control of wander.

The concerns of CBR service needs in the context of clock recovery impairments (e.g., slips, wander) are pivotal to determining which method or combination of the two methods is appropriate.

ANNEX 20

(to the report of SG13)

SOURCE : Q.6 (AAL1/2) / SG13 (WP2) 2, Geneva mtg, 5-16/6/1993

TITLE : [redacted] Liaison to SG 15 (ATM Video Group) (for action), CMTT/3 (for action), and ISO/IEC MPEG (for information)

SUBJECT : An error correction method for delay sensitive signal transport of AAL Type 1

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The AAL1/2 group of Q.6 / SG13 has been studying an error correction method for delay sensitive signal transport. Based on a contribution submitted and Liaison documents received from SG 15 (ATM Video Group) and CMTT/3, the group produced a description of such a method, as attached, that utilizes a short interleaver with diagonal processing and FEC (Reed-Solomon code).

The method provides a common technique for both interactive video signal transport, e.g., H.320 (px64kbit/s) video codecs, and high quality audio signal transport for interactive applications. SG13 has the objective of enhancing this method (as well as the interleaver method for loss sensitive signal transport, described in section 2.5.2.4.1 of Rec. I.363), so that it can be used simultaneously with both the Synchronous Residual Time Stamp (SRTS) and Structured Data Transfer (SDT).

The processing delays introduced by the method, including both the transmitter and the receiver delays, are 14.7 ms (384 kbit/s), 3.67 ms (1536 kbit/s) and 2.93 ms (1920 kbit/s). The overhead is 6.38 %. The method can correct one cell loss within 16 cells or three errored octets within a row of 94 octets.

With regards to requirements received from SG15 (ATM Video Group) and CMTT/3, the following provides additional information:

- SG13 used one of the four alternatives of RS (Reed-Solomon) codes suggested in a CMTT/3 Liaison. The selected alternative is given in the attached description. It is based on a 16-cell matrix, chosen to minimize processing delay.

- The attached description conforms to one of the two alternatives (i.e., based on 47 or 48 - octets) of an interleaving process suggested by SG15 (ATM Video Group). The method described uses a 47-octet instead of 48-octet based matrix. Hence the method avoids unnecessary and complicated processing between SAR and CS operations.

Regarding RS code, SG 13 recognizes that the binary primitive polynomial suggested by SG 15 (ATM Video Group) is different from that suggested by CMTT/3 as summarized below:

- From SG15 : $g(x)=x^8+x^4+x^3+x^2+1$. (Included in Liaison from SG15)
- From CMTT/3 : $g(x)=x^8+x^7+x^2+x+1$. (This is for a long interleaving method, i.e., error correction method for loss sensitive signal transport. See Report of CCITT SG XVIII Jan. meeting.

SG13 wishes to have a common and unique binary primitive polynomial for error correction methods of both loss and delay sensitive signal transport. Note that in an AAL, support of an erasure mode is mandatory.

SG13 would appreciate a careful review of the topics covered in this Liaison.

ATTACHMENT

ANNEX 7 of the ~~Q.6/(AAL1/3)/SG 13~~ WP2 meeting report.

ATTACHMENT

(Tokyo report of WP 13/21)

Annex 2

Cell loss correction method for delay sensitive services

A method is proposed in the AAL 1 for counteraction of network impairments such as cell loss and/or errored bits. This method is particularly adapted to those services sensitive to delay, e.g. low bit rates services like conversational audiovisual services or High Quality audio. The method relies on a combination of FEC using Reed-Solomon codes and octet interleaving of data.
In order to meet short delay requirements, the method is based on a 16 cell interleaver, with an improved interleaving mechanism which keeps all correction capabilities of the classical one in relation to both cell.loss and errored bits.

Characteristics of the short interleaver method

The method is based on Reed-Solomon (94,88) codes which have been suggested in the Liaison Statement from the CMTT/3. The erasure mode is used for the correction of dummy octets corresponding to cell losses. The same polynomial as that of the long interleaver may be desirable as far as applicable.
The size of the interleaver is 16 cells, the matrix has 8 rows and 94 columns.
Correction capabilities are :
- one cell loss in the group of 16 cells
- 3 octets in a row of 94 octets.

The overhead of the method is 6.38 %.

Diagonal interleaving mechanism

A diagonal interleaving mechanism is used to improve the processing delay of the method. In the interleaver, the writing mode and the reading mode are alternate. The process in the interleaver is continuous, i.e. only one interleaving memory is necessary at each end.

Operation in the transmitting end:

The writing order in the interleaver is horizontal.
The reading order is diagonal.
Let a (i,j) be a coefficient (i.e. an octet) in the matrix, where i is the row number and j the column number. Then the sequence of coefficients to be read out of the matrix diagonally is as follows :

... , a (i+1,j-1) , a (i,j) , a (i-1,j+1) , ...

The organisation of the interleaver is given in fig.1.

writing order ⟶

A1	A2	A3	...	A93	A94	*A95*
B1	B2	B3	...	B93	B94	*B95*
C1	C2	C3	...	C93	C94	*C95*
D1	D2	D3	...			
E1	E2	E3	...			
F1	F2	F3	...			
G1	G2	G3	...	G93	G94	*G95*
H1	H2	H3	...	H93	H94	*H95*

Fig.1. Interleaver structure

For a correct reading order of the diagonal mechanism, a dummy column is added. It is used only for counting, it does not contain any information and it is not transmitted. It is mentioned in italics in the following sequences only to permit a good understanding of the method.
Examples of 47 octets sequences that are read out are given hereafter :

...
seq. k : *(B95)*, A1,H2,G3, ... , A9, ... , A17, ... , A25, ... , A33, ... , A41, ... , C47.
seq. k+1 : B48, A49, H50, ... , B56, ... , B64, ... , B72, ... , B80, ... , B88, ... , D94.
seq. k+2 : *(C95)*, B1, A2, H3, G4, ... , B9, ... , B17, ... , B25, ... , B33, ... , B41, ... , D47.
seq. k+3 : C48, B49, A50, ... , C56, ... , C64, ... , C72, ... , C80, ... , C88, ... , E94.
seq. k+4 : *(D95)*, C1, B2, ... , C9, ... , C17, ... , C25, ... , C33, ... , C41, ... , E47.
...

Operation at the beginning of the communication :

At the beginning of the call, the reading of the interleaver begins before it is completely filled up. In practice, the reading process begins as soon as the first row has been written in the interleaver. As a result, in the first SAR-PDUs of the communication, only some octets carry valid information. Other octets are filled with dummy information as they correspond to positions in the interleaver which are not yet filled.
The communication begins as follows (X : dummy octets) :

1st SAR-PDU : A1, X ... X, A9, X ... X, A17, X ... X, A25, X ... X, A33, X ... X, A41, X ... X.
2nd SAR-PDU : B48, A49, X ... X, B56, A57, X ... X, B64, A65, X ... X, B72, A73, X ... X, B80, A 81, X ... X, B88, A89, X ... X.

The first SAR-PDU to be completed is number 16.

Operation at the end of the communication :

At the end of the communication, the transmitting interleaver is read out until it gets completely empty. Some data in the first rows of the transmitting interleaver will be transmitted twice, which has no action in the receiving interleaver where they will be stored a second time in the corresponding first rows after they have already been read out.

Operation in the receiving end

The mechanism in the receiving interleaver is inverse of that of the transmitting interleaver, i.e. the writing order is diagonal and the reading order is horizontal. When a row has been completed in the interleaver, it is immediately read out for FEC processing.

Processing delay

The following calculation of the processing delay takes into account both the transmitting and the receiving ends. Let D be the processing delay corresponding to an interleaver.
Due to the diagonal mechanism, for a given row of the interleaver, the distribution of the delay is following :
- for the first octets of the row to be transmitted the delay is null in the transmitter and D in the receiver
- for the last octets of the row to be transmitted the delay is D in the transmitter and null in the receiver.

As a result, for a given row the total delay is D instead of 2D with a classical interleaver.
Examples of values are given for the total processing delay. Processing delays are: 14.7 ms for 384 kbit/s, 3.67 ms for 1536 kbit/s, 2.93 ms for 1920 kbit/s.

Delineation of the interleaver

For the delineation of the 16 cell interleaver, the CSI bit is used.

ANNEX 18

(Emergent-SC13)

ITU - Telecommunication Standardization Sector — Temporary Document 28(13/2)

STUDY GROUP 13

Geneva, 5-16 july 1993

Question: 28/13

Liaison Statement to SG I, SG 9, SG 11 OF SG 15, MPEG

SOURCE: SG 13 (Geneva MEETING 5-16 JULY 1993) RS 10

Subjectr: IVS BASELINE DOCUMENT

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In accordance with Question 28/13 Study Group 13 will continue its Integrated Video coordination activities across Study Groups. The IVS Base Document, which serves as a mechanism to achieve this coordination, has been updated and is attached. The updates include material from Liaison Statements received from ISO/IEC JTC1/SC29/WG11 MPEG, Task Group CMTT/3 and the SG 13 meeting.

Please review the document and send any additional material or modifications.

IVS Document will be reproduced as a contribution for SG13.