Telecommunication Standardization Sector
Study Group 15
Experts Group for ATM Video Coding
(Rapporteur's Group on Part of Q.2/15)

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Title: **Harmonising/combining low complexity, error resilience, scalability, image quality and compatibility**

Source: **PTT Research (NL)**

Purpose: **Discussion**

Introduction

In the current stage of the MPEG/Experts group work the focus goes out to the main profile and it's main level. The main profile is required to have error resilience, but scalability and compatibility are considered to fall in other profiles.

During the course of MPEG many proposals have been made which combine some of the **features of: low complexity, error resilience, image quality, scalability and compatibility.** Till so far no effort has been made to combine all proposals into one concise generic solution.

In this contribution a proposal will be made which combines most of the ideas, which were on the table at some time, into one concise generic solution. **With this solution all features can be combined for the main profile.**

Examples of the proposals currently on the table

The first example would be the most 'simple' decoder system currently proposed by Sarnoff and Thomson, which will provide error resilience. Data partitioning is used to achieve error resilience and high frequency coefficients (along the zigzag scan path) are merged with low frequency coefficients. In principle this merge can be seen as a addition, this is depicted in figure 1.

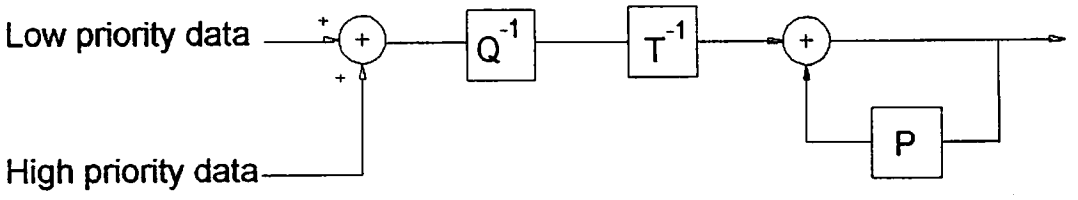

Figure 1: Functional equivalent of the data partitioning decoder block diagram

A second scheme is using a sort of data partitioning, always taking the 4x4 low frequency components for a high priority channel to provide error resilience and scalability. The low frequency coefficients may be recoded again in the second layer. This is the scheme being proposed by the Australian consortium and is shown in figure 2.

The third scheme, using SNR scalability to achieve error resilience, has been proposed by Philips LEP and CCETT, and is also depicted in figure 2.

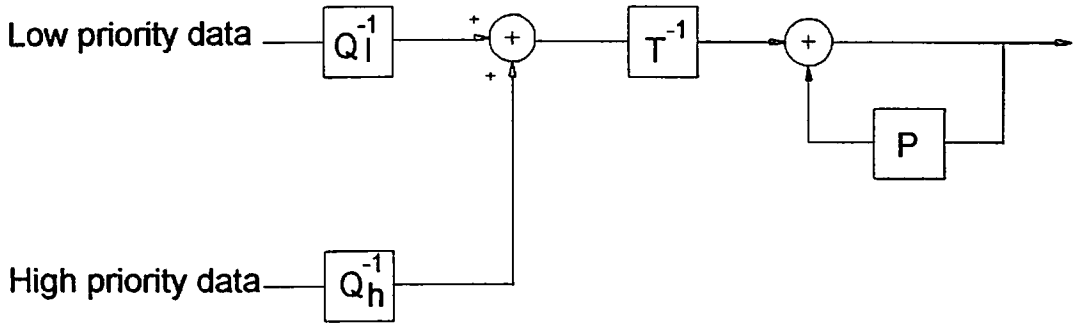

Figure 2: Functional equivalent of the SNR scalable and frequency scalable decoder block diagram

It should be noted that figure 1 and figure 2 are identical, when one defines the Ql and Qh in figure 2 to be the same.

The concise generic decoder solution

It is even possible to shift the addition to after the inverse DCT and one could come to a figure depicted in figure 3, which is still equivalent to figure 1 and figure 2 and has all functionality's as comes the functionality for the schemes from figure 1 and figure 2.

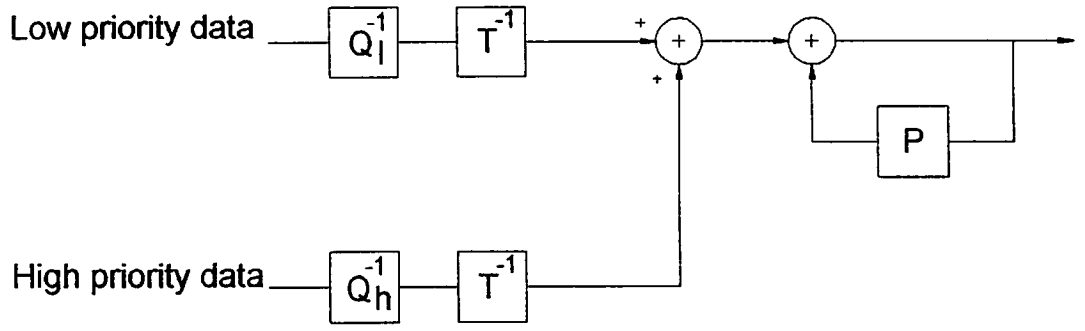

Figure 3: Functional equivalent of figure 1 and figure 2

It should be noted that in Figures 1,2 and 3, the inverse transforms in both data streams have to operate at the same pixel rate. It also should also be noted that it is not possible to support an optimally down-converted image with these systems and therefore does not have compatibility and inter working with smaller coded images e.g. MPEG1, H.261 or even MPEG2.

What one can do to solve this problem is to generalise the model of Figure 3 and allow the possibility of an up conversion in the system as shown in Figure 4. The system one then would get is only slightly more complex then the system depicted in figure 1 and 2, but will offer much more functionality then those systems. It will support all functionality of the data-partitioning system (error resilience), the SNR scalable system (watchable high priority data images) and the frequency scalable system ('simple' 'software' decoding of the high priority data images). **But more is offered,** this scheme does also provide in addition to all these features the possibility of being compatible (see figure 4).

One form of decoder diagram for a main profile, main level system is depicted in figure 4.

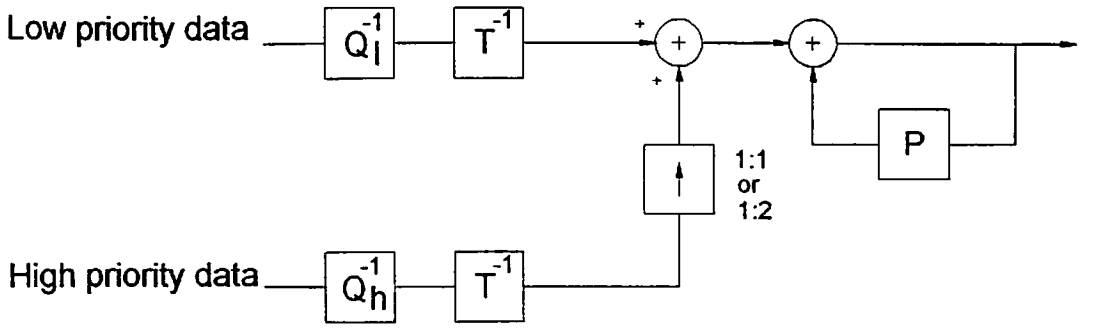

Figure 4: Suggested main profile decoder structure

Note: the up converter supports 1:1 (no up conversion) as wells as 1:2 up conversion.

The above proposal can be combined with the current TM spatial scalable solution in one block diagram showing the two options. This is shown in Figure 5.

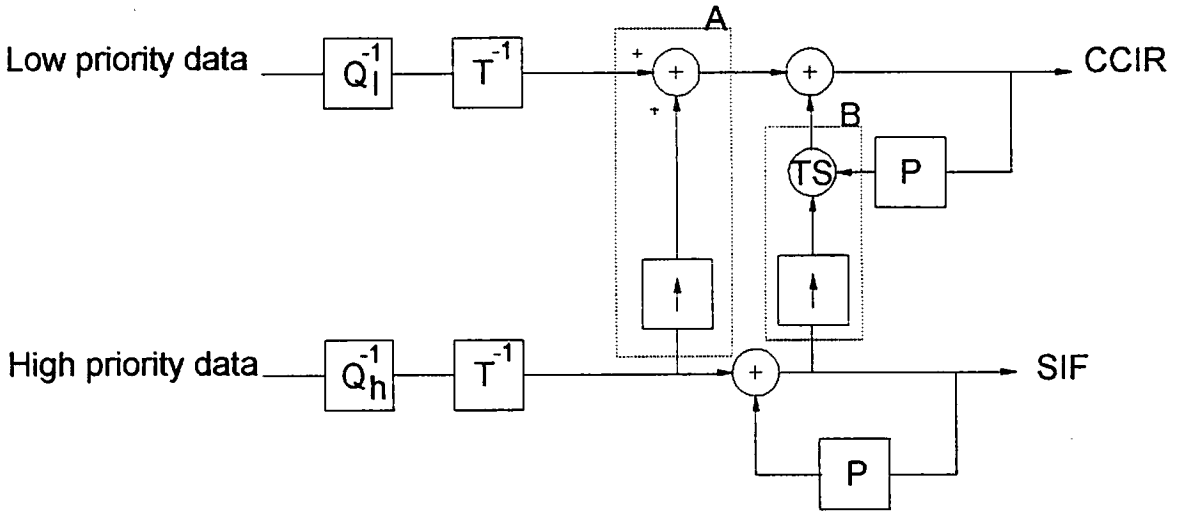

Figure 5: Full scalable/compatible core level decoder structure (possibly an extension of the MAIN)

TS - Temporal-Spatial weighting switch

Data paths A and B are not used concurrently. **It is proposed to signal in the sequence header which data path is used.** Data path A is selected for low complexity, error resilient decoders, data path B is selected for full scalable, compatible, higher image quality decoders.

NOTE: The up converters can be switched off (1:1 up conversion). Data path A's up converter for a 1:2 up conversion is a simple linear (1 2 1) filter inside a block for progressive to interlace (the temporal miss aligned field should not be predicted). Data path B's up converter for a 1:2 up conversion is a simple 1 2 1 filter inside a block for progressive to interlace.

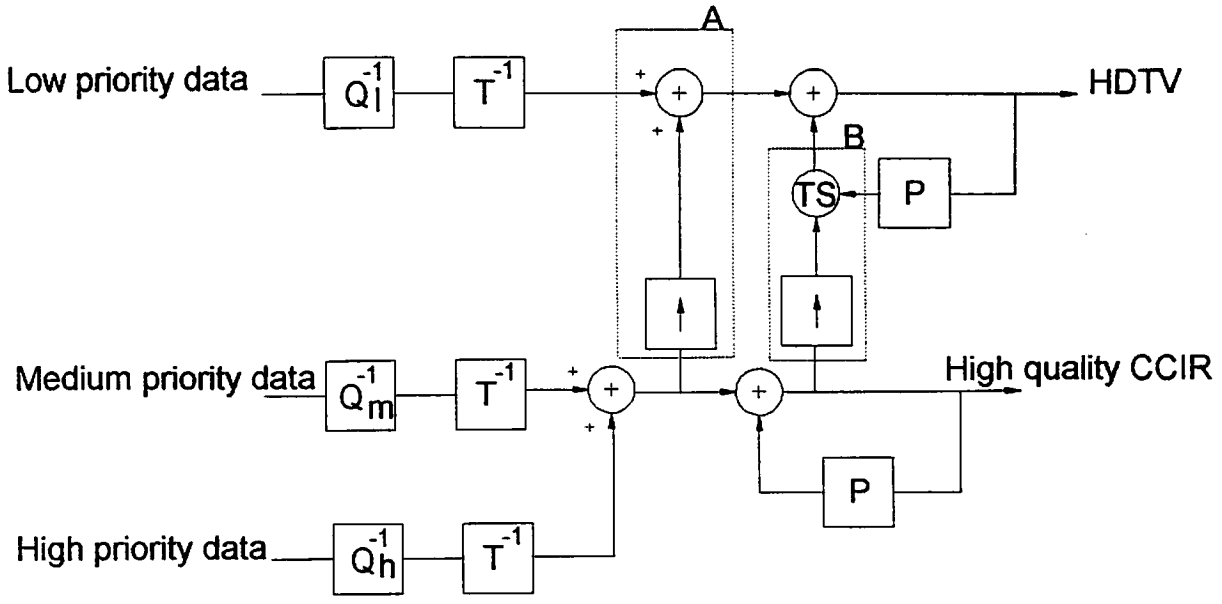

Figure 6: Full three level HDTV decoder structure

TS - Temporal-Spatial weighting switch

Data paths A and B are not used concurrently. **It is proposed to signal in the sequence header which data path is used.** Data path A is selected for low complexity, error resilient decoders, data path B is selected for full scalable, compatible, higher image quality decoders.

Decoder conclusion

The proposed structure has merged the Thomson-Sarnoff error resilient system, the Philips/CCETT error resilient/SNR scalable system, the Australian low complexity/error resilient system, the BT/AT&T compatible system and the PTT low complexity/compatible system. No changes to the syntax on the macroblock layer have to made. Signalling of the exact configuration of the encoder for will happen at the sequence layer.

It has been suggested that the above approach should be included in the Main Profile.

The encoder

The main profile, main level encoder could be configured in many different ways, partly depending on the implementation of the targeted (subset of) main profile, main level decoder. A possible implementation of the MAIN encoder is depicted in figure 6.

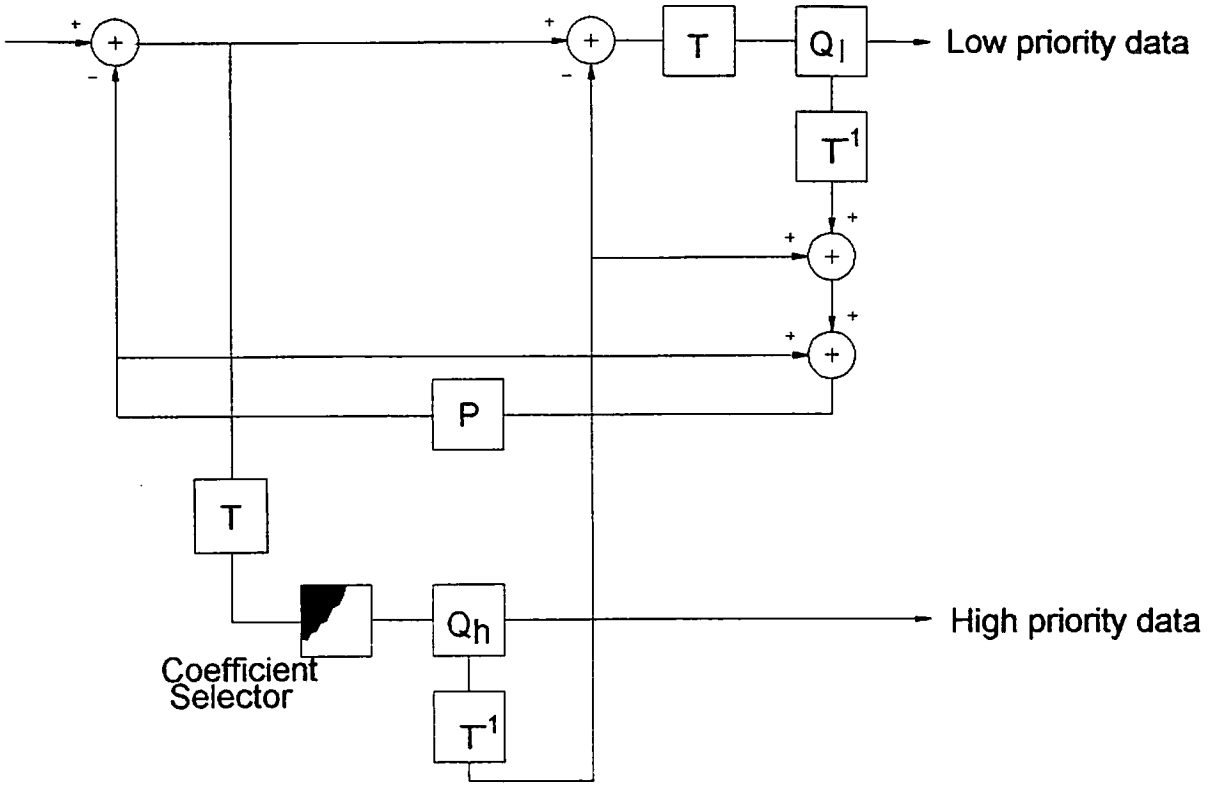

Figure 7: Possible logic block diagram of MAIN encoder encapsulating 3 coding schemes

Figure 6 encapsulates 3 coding schemes currently on the table:

1. Sarnoff-Thomson's error resilient scheme, Incas Qh and Ql are identical; coefficient coded in the high priority data stream will generate zero's coefficients in the low priority data stream.
2. Philips' error resilient/SNR scalable scheme, In case the coefficient selector selects all coefficients, a course quantisation is performed by Qh and a finer re-quantisation is performed by Ql.
3. Australian scalable/error resilient scheme, In case the coefficient selector always selects the 4x4 low frequency coefficients, and Qh and Ql could be identical; coefficient coded in the high priority data stream will generate zero's coefficients in the low priority data stream. If Ql performs a courser quantisation then Qh, the 4x4 low frequency coefficients are refined.

Using the proposed MAIN decoder, the selection of one of the three schemes will be an encoder option. The current macroblock layer syntax for spatial scalability will support all three options.

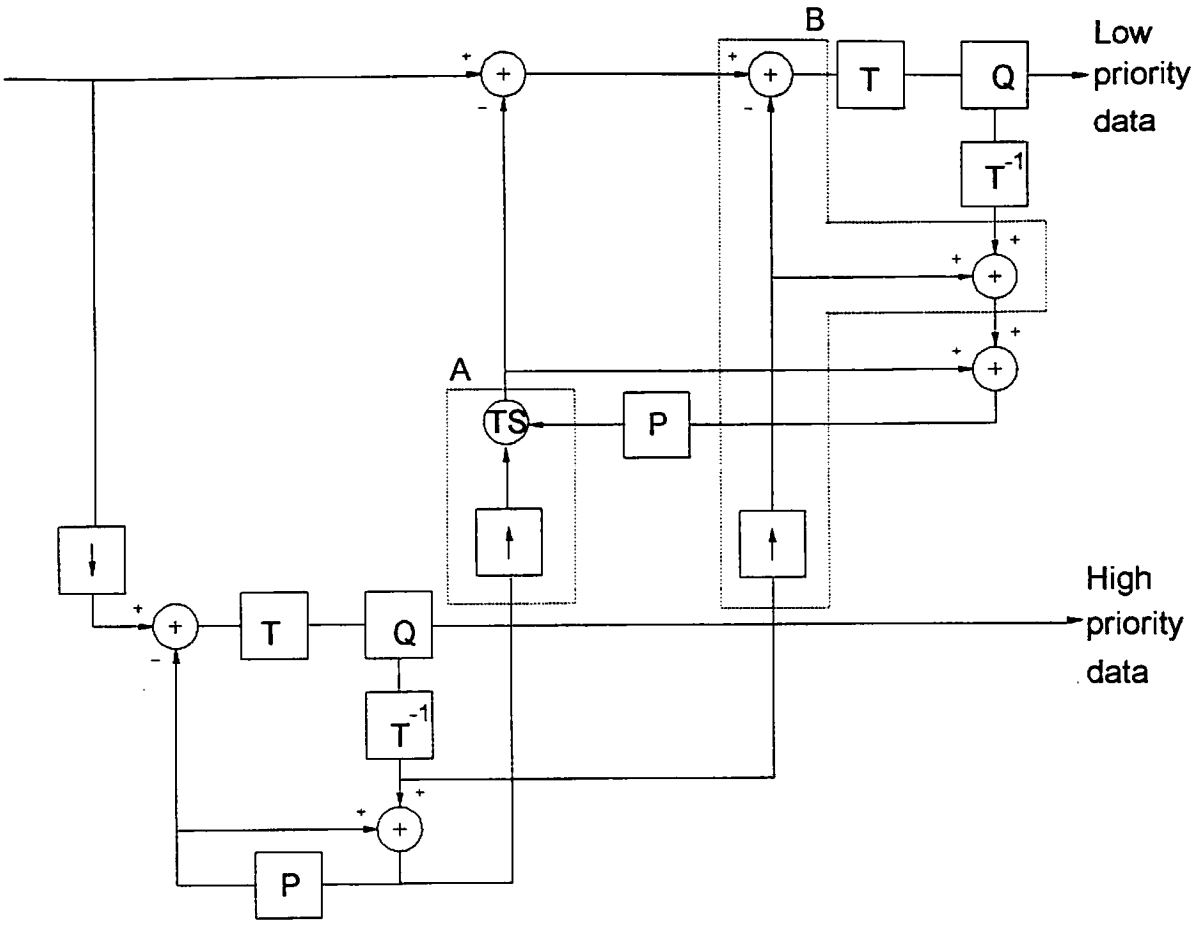

Figure 8: Possible implementation of a full scalable/compatible core level encoder, able to generate an MPEG1/H.261 high priority data stream, for the proposed MAIN decoder (figure 4), as well as an possible extension of the MAIN (figure \5).

Data paths A and B are not used concurrently. **It is proposed to signal in the sequence header with data path is used.** Data path A is selected for the proposed MAIN decoder (figure 1), data path B is selected for full scalable, compatible, higher image quality decoders.

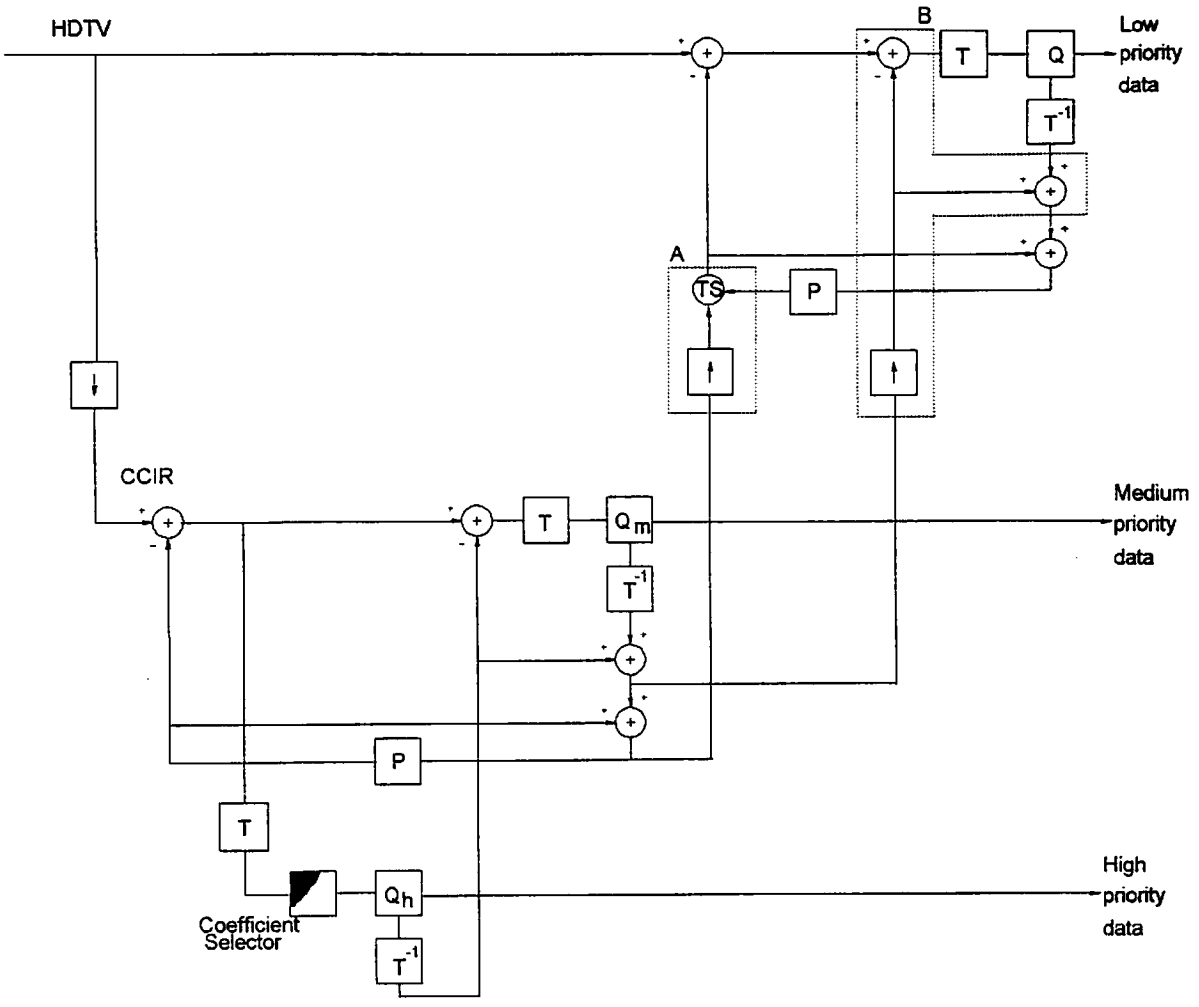

Figure 9: Possible functional block diagram of 3 level HDTV encoder

Encoder conclusion

The proposed structure has merged the Thomson-Sarnoff error resilient system, the Philips error resilient/SNR scalable system, the Australian low complexity/error resilient system, the BT/AT&T compatible system and the PTT compatible system. No changes to the syntax on the macroblock layer have to made. Signalling of the exact configuration of the encoder for will happen at the sequence layer.

Conclusion

Within the current macroblock syntax a harmonisation of most error resilient/low complexity/scalable/compatible schemes has been demonstrated. The proposed structure allows all above mentioned features for the main profile, main level decoder, which will allow future inter working for a wide range of applications.