

INTERNATIONAL STANDARDIZATION ORGANISATION
ISO/IEC JTC1/SC2/WG11
CODING OF MOVING PICTURES AND ASSOCIATED AUDIO

MPEG 91/210

Proposal 12

**16 CHANNEL SUBBAND BASED TV CODEC
FOR BIT-RATES UP TO 10 MBIT/S**

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European VADIS/COST collaboration**

PREFACE

This document describes the HHI proposal for MPEG II which is based on an image subband decomposition. The document is structured into four main parts: First, the features of the algorithm are listed (see summary of the proposal), second, the algorithm is described in some detail (see proposal document). Third, the hardware evaluation follows (updated version of distributed hardware evaluation paper) and, at last, tables of codes and statistics conclude the document.

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1. Introduction

This document describes the HHI proposal for MPEG II which is based on an image subband decomposition. The proposal is mainly intended to be used for bit-rates between 1 and 10 MBit/s, however, due to block-free signal processing different picture formats e.g. TV, EDTV, HDTV are supported. The core of the system works on progressive pictures. Only predictive coding is implemented up to now, however, an interpolative mode can be used. A progressively scanned picture source can feed the system core without any constraints. Figure 1 represents the block diagram of the proposed coder and the decoder.

2. General outline

The main features of the HHI subband proposal are (see also Annex 1)

- * full CCIR 601 format
- * hybrid subband coding
- * frame based coding
- * every 10th frame is coded INTRA
- * predictive coding
- * no interpolative coding mode
- * frame based calculation of motion vectors
- * full search block matching
- * block-size 8 x 8
- * 1/2 pel vector accuracy
- * motion vector range +-12 pixels, +-12 lines
- * subband based intra-inter decision
- * no macro-block concept
- * local and global bit-rate control
- * adaptive quantizing
- * different VLCs for coefficient coding

3. Picture format

Full CCIR 601 4:2:2 is supported i.e. 720 pels, 576 lines and 25 frames. All other picture formats i.e. EDTV and HDTV and progressive picture sources are possible.

4. De-/re-interlacing

After de-interlacing, the higher vertical correlation can be exploited in frame-based than in field-based systems. This holds only for non-moving picture areas. In moving areas additional high vertical frequencies can appear after field merging. A conversion between the initial interlaced CCIR 601 signal and the progressive input of the system core is needed. Simple field merging is used in the proposal, although more sophisticated motion compensated techniques will result in better deinterlaced pictures. After decoding the frame, two fields are generated out of one frame in the receiver.

16 channel subband based TV codec for bit-rates up to 10 MBit/s

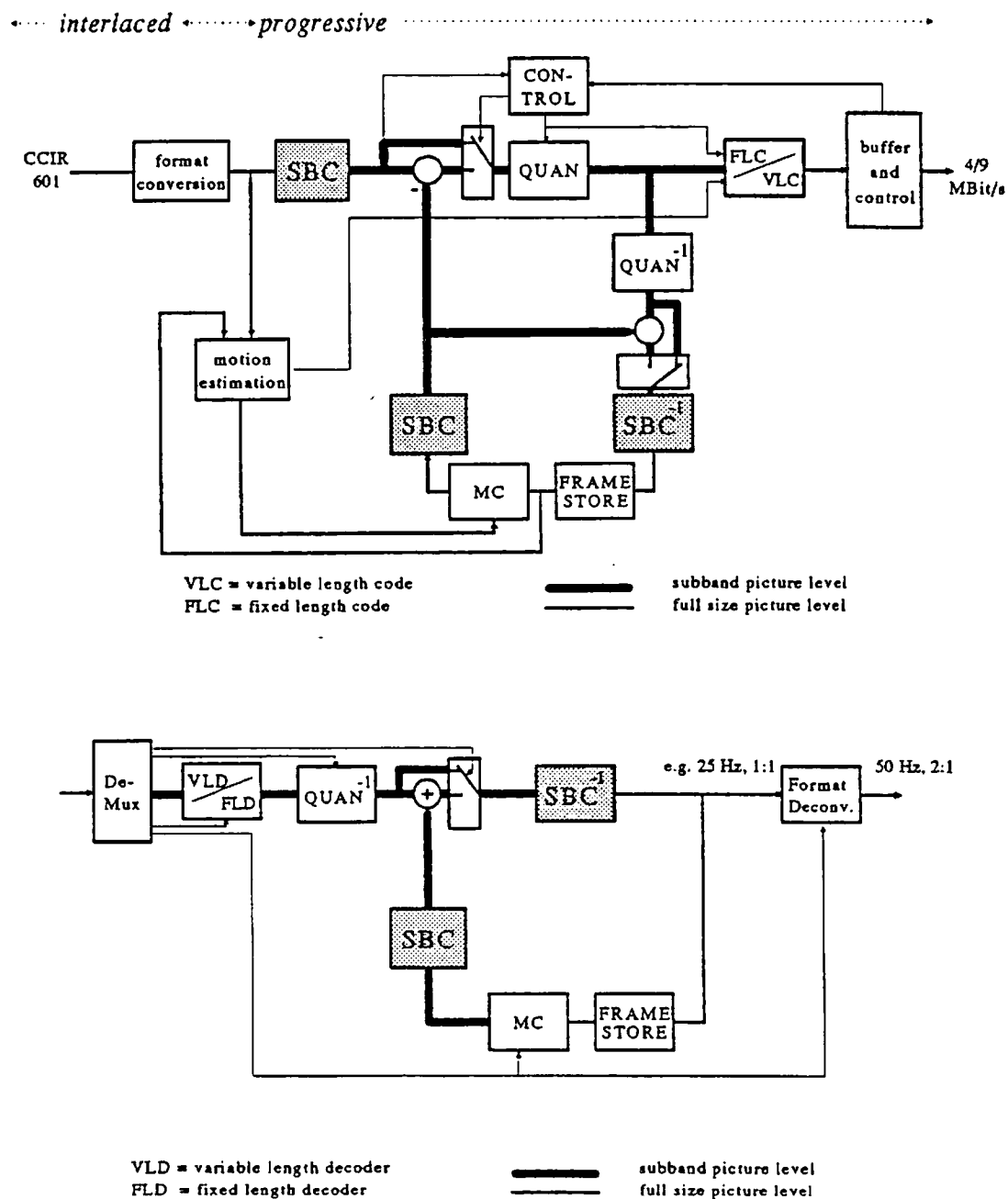


Figure 1: Block diagram of coder and decoder

5. Subband splitting

The core of the system is a regular tree structured subband decomposition into 16 layers or channels. Traditional quadrature-mirror-filters are used for filtering and interpolation. The number of taps used was very short (< 10) because no real advantage could be noticed by using higher order filters. For some reasons the number of 16 subbands may be sufficient. The correlation of the input image has been strongly reduced and further splitting of the higher subbands would only produce quantization errors. Different resolutions and window sizes are supported e.g. CIF, TV, HDTV. The subband clock frequency is small enough ($1/16 \times 13.5$ MHz) to use standard technology in the subband coding part or even programmable solutions. All subbands can be processed with the same clock frequency.

The fundamental idea of subband splitting and coding is to perform some decorrelation of the signal and to apply different quantizers adapted to the statistics of the subband signals and the sensitivity of the human visual system. In the proposal a hierarchical structure with horizontal splitting at the beginning followed by vertical splitting marks the inner core of the system. Each of these channels is split again into four channels by repeating the first step of processing on the smaller sized subband pictures. Figure 2 shows the block-diagram of the core subband splitting with four subbands and the full 16 channel splitting. The inverse splitting is performed in the same way. Polyphase realizations and the symmetry of the quadrature-mirror-filters are exploited to reduce mainly the number of multiplications. Luminance and chrominance are processed with the same filters.

Annex 2 shows the filter coefficients and the frequency responses for the filters in use.

6. Subband prediction

The temporal correlation is reduced by motion compensated coding of all subbands. After subband quantization the full input frame format is reconstructed in the encoder. This signal is used for motion compensation. The motion vectors that point from the input image to the last decoded reconstructed image (which has been stored in the frame memory) are calculated. Then, the prediction image is decomposed into 16 subbands. The subsequent intra/inter switching is very flexible and could be adapted to each subband. With that, high frequent moving artifacts can be avoided. A trade-off between resolution and quantization errors is inherent in the system.

7. Motion estimation

Motion vectors are calculated on blocks of 8×8 pixels within a frame. First, the search is done on integer pel accuracy using the absolute difference value between two blocks for optimization. Then, a half pel accuracy vector is calculated from the neighbourhood. The maximum search range is ± 12.5 pixels and ± 12.5 lines. There are no subband specific techniques used for motion estimation. However, the block nature of motion estimation does not fit well the block-overlapping subband filtering of the predicted image. There are some techniques under discussion to avoid block structures in the predicted image. They have not been implemented for the Kurihama tests.

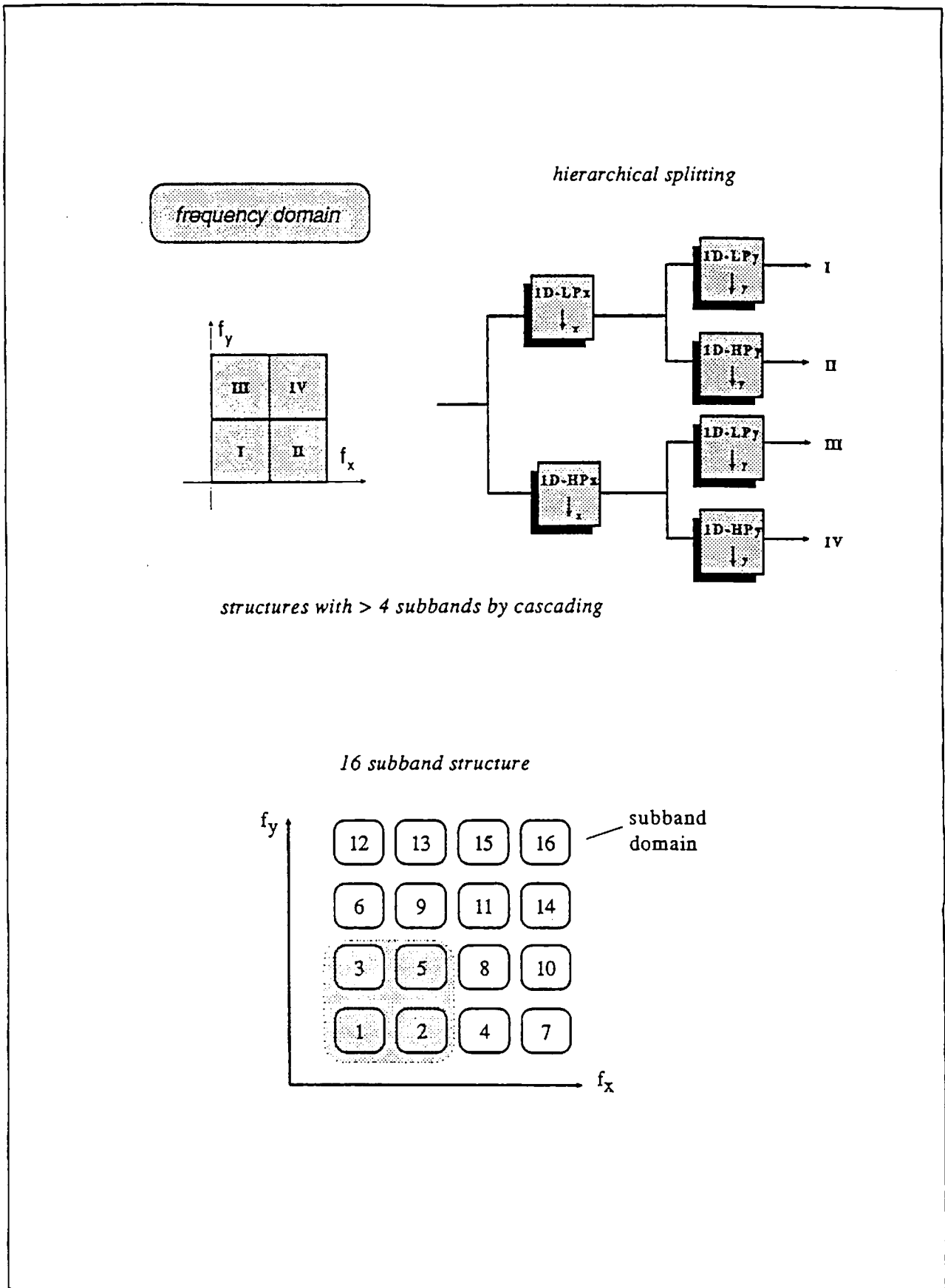


Figure 2: Core of subband splitting and full 16 channel splitting

8. Group of pictures (GOP)

A GOP consists of 10 pictures. A picture consists of one luminance and one chrominance field for each colour component, respectively. All even chrominance fields are skipped and not used for coding. The first picture is entirely INTRA coded. The remaining 9 inter pictures are both intra and inter coded.

9. Subband coding

Subbands are coded nearly individually. First, 4 x 4 pels within each subband are processed in the same way. These pels are quantized using a linear quantizer from a set of 32 available quantizers. There are different parameters which control the quantizer selection:

- * picture mode (e.g. intra, inter, luminance, chrominance)
- * frequency weighting
- * global buffer control
- * local buffer control
- * pre-analysis of the input subbands

Usually, the finest quantizer is selected at the beginning of a 4 x 4 pel area in the subband. If the bit account increases more than a given threshold, coarser quantizers are taken. Threshold values of 5% (4 MBit/s) and 10% (9 MBit/s) have been implemented. All 16 subbands are processed in the same way. Then, a sequence of 256 pels (4 x 4 pels in 16 subbands) is scanned and entropy coded. The available quantizers cover the whole range of necessary step-sizes.

10. Scanning

Scanning is used to generate a so called string of 256 pels:

- * pel domain scanning
- * subband domain scanning

The scanning path for pel domain scanning depends on the spatial frequencies of the subbands. Actually, diagonal, horizontal and vertical scanning of 4 x 4 pels are used (see figure 3). Diagonal scanning is used for the lowest and highest subbands. Horizontal and vertical scanning is used for subbands with vertical and horizontal frequencies, respectively.

Subband domain scanning is performed with a zig-zag like scanning pattern adapted to a 4 x 4 array of 16 subbands. However, due to the field merged frame to be processed, some modifications have been included. High vertical frequencies have higher energy concentration in moving areas because of vertical aliasing. Therefore, the priority of these subbands related to scanning is increased. This procedure holds only for the luminance signal. Both chrominance signals have not been field merged and the unmodified zig-zag pattern can be used. If 4:2:2 processing is needed, luminance and chrominance become similar.

The scanning paths are given in figure 3 and figure 4.

11. Entropy coding

In a high-frequency subband, one can easily recognize two kinds of regions:

- * regions with zeros --> low activity
- * regions with non-zero values --> high activity

These two kinds of regions have their proper signal statistics, and therefore, the bit rate in each region is compressed with an appropriate code. Therefore, a two-state coding algorithm is proposed, with states that reflect the two kinds of regions:

- * zero-state for coding regions with zeros
- * non-zero state for regions with non-zero amplitudes

The possible messages that have to be coded in each region of the states are:

- * in the non-zero-state:
pel amplitude = 0, +1, -1, +2, -2, ..., +255, -255
- * in the zero-state:
EOB (end of block), zero run length = 0, 1, 2, ..., 255

The state transitions of the entropy coding system take place under the following conditions:

- * from zero-state to non-zero-state:
after the transmission of a zero run length
(i.e. a non-zero value ends a zero run)
- * from non-zero-state to zero-state:
after the transmission of a zero amplitude

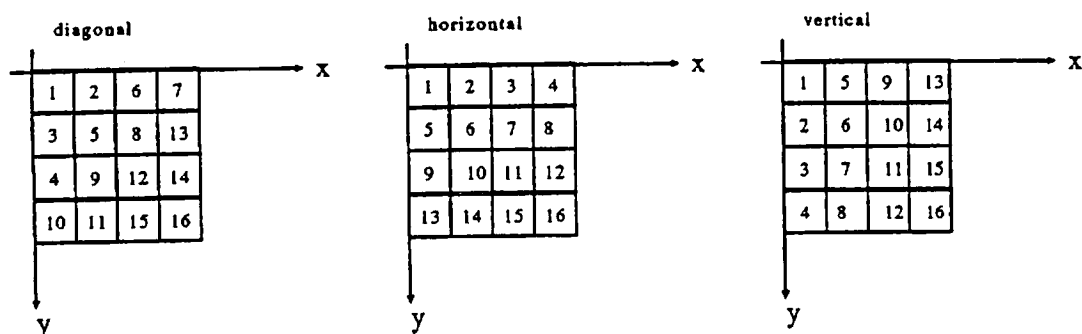
These transitions do not require the transmission of any overhead information. This entropy coding algorithm requires two VLC codebooks:

- * one for amplitudes in the non-zero-state
- * one for zero run length and EOB in the zero-state

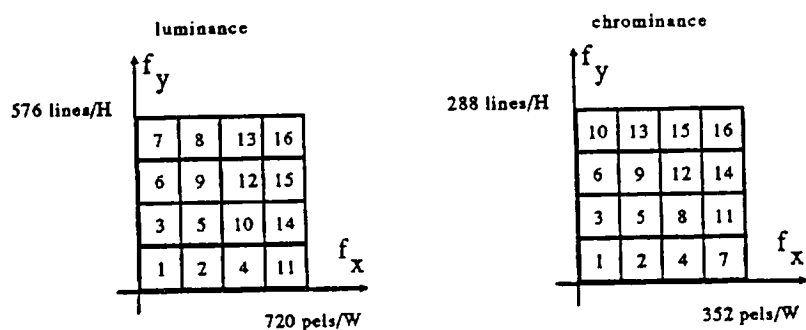
For an improved performance, both VLC-codebooks should be optimized for each subband. In the case of 16-band subband coding, a lot of subbands have similar signal statistics, so that not 2*16 VLC-codebooks have to be optimized. Eight sets of VLC-codebooks are proposed (one "set" is an amplitude codebook and a run-length codebook). As the signal statistics also depends on inter-/intra- frame coding, four sets are available for intra-coding and four for inter-coding.

The subband pels are coded in strings of 256 values, composed by 16 values of each subband as follows (see figure 5). Zero runs can start among the values of one subband, and continue in the next subband of the above string. If different codebooks are foreseen for these subbands, the code word for this run length is taken from the codebook for the subband where the zero run starts. The VLC-codebooks are optimized for Laplacian (non-zero-state) and Poisson (zero-state) probability distributions, with variances measured in a training session. The VLCs have been optimized taken into account a maximum code word length.

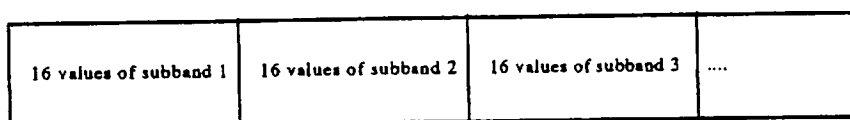
Pel domain scanning modes



Subband domain scanning modes



Entropy coding of strings of 256 amplitudes



Initial bit allocation for all modes

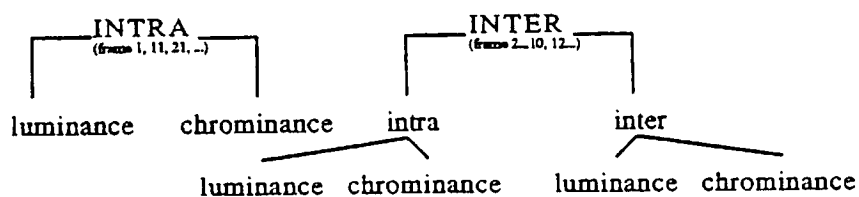


Figure 3: Pel domain scanning
Figure 5: Entropy coding

Figure 4: Subband domain scanning
Figure 6: Initial bit-allocation

The main advantages of this entropy coding are:

- * easy implementation
- * easy interpretation of its parameters
- * adaptable to the statistics of the layers of a coding hierarchy
- * bit rate approximates the signal entropy

Annex 3 shows the VLC tables in use. The same tables have been used for 4 and 9 MBit/s.

12. Local and global bit-rate control

Bit per frame control, global and local bit-rate control have been implemented. The distribution of the priorities between the three different control systems is given below:

- | | | | |
|---|---------------------|----|------------------|
| * | global control | => | highest priority |
| * | bit / frame control | => | mean priority |
| * | local control | => | lowest priority |

In the following, the notation "local" means 4 x 4 pixels of 16 subbands. Because of the GOP of 10 frames (1 intra and 9 inter images), there are different bit-rates to be processed. The main task of the buffer is to smooth these different rates. The **global bit-rate control** depends on the buffer status. For most of the time (buffer status between 10 and 90 %), the global bit-rate control does not change any coding parameters. To avoid buffer overflow, coarser quantizers are selected in the "emergency case" than they would normally be by the local bit-rate control. However, the emergency case is mostly avoided due the local control, i.e. global control is only used if all pixels exceed a given number of bits.

The number of bits allocated to one frame and subsequent to one string of 256 amplitudes is initially calculated and recalculated from frame to frame: Gain in intra-images is given to the last three luminance images of a GOP. Gains in chrominance pictures are given to the subsequent luminance inter-pictures. Gain in inter luminance is given to the subsequent inter luminance pictures.

The **local bit-rate control** allocates bits to strings of 256 amplitudes. At the beginning, initial values of bits are calculated for the different picture modes as proposed in figure 6. These values are always recalculated after finishing the coding of the last 256 amplitudes. Gain or loss in bit-rate is spread over the neighbouring future strings of 256 amplitudes. However, loss due to too many used bits can only appear in regions where all available quantizers would not decrease the bit account and with that, of course, the quality.

13. Low frequency subband processing

Due to some remaining correlation in the low frequency subband, further signal processing can achieve higher compression. Both, predictive or transform algorithms can be used. However, additional quantization noise should be avoided because of the noise spreading feature of the subband reconstruction. Therefore, reversible or nearly reversible coding of the low frequency subband must be realized. In the proposal a DPCM like procedure is implemented which works in two dimensions on a 4×4 block of pels.

14. Intra-inter decision

Generally, all 16 subbands are individually motion compensated, however, the prediction is done on the full size image. In all inter pictures of a GOP, there are some areas which should be coded in an intra mode. There are at least two reasons for that:

- * due to object movements i.e. in areas where motion estimation fails and results in a bad prediction image or background of a moving object that could not be predicted
- * motion vectors calculated on the full size image produce worse prediction of high-frequency subbands

In summary, it must be locally checked whether intra or inter gives the best coding results. The sum of all 4×4 absolute pixel values is taken in each subband and compared to the corresponding sum of the subband prediction error. This calculation is performed 16 times starting from the highest subband and ending at the lowest subband after using a special scanning path. For the first time, the inter mode is decided for a subband, all subsequent lower frequency subbands are decided to be inter. With that, there is only one switch from inter to intra in a picture subband area of 4×4 . One 4 bit address has to be transmitted to the decoder in fixed bit length format. Statistical evaluation of the inter-intra switching showed that most changes from intra to inter occur in the four highest subbands. In about 50% of the picture areas there is no change i.e. all subbands are processed in the inter mode. Of course, this strongly depends on the signal statistics.

15. Buffer sizes

Buffer sizes of 800000 bits and 1600000 bits for 4 and 9 MBit/s have been used, respectively. An initial buffer value of 25 % has been implemented.

16. Motion vector coding

There are 90×72 motion vectors to be transmitted for each frame consisting of luminance and chrominance. Each vector is horizontally predicted using its preceding value. This calculation is performed for each vector component. Variable length coding of difference vectors is done.

The same VLC-code is used for all sequences and bit-rates to be considered for the Kurihama tests.

Annex 5 shows the VLC table in use.

17. Overhead information

Beside all synchronization bits which have not been considered so far, there is some necessary overhead to be transmitted regularly. For 256 pixels which are always taken together, 4 vectors have to be transmitted. Then, a 5 bit address is needed for the quantizer selection in the decoder. Furthermore, a 4 bit address is used to give the decoder the switching address for the inter-intra decision.

18. Post-processing

First, de-interlacing of the luminance frames is performed by reading two fields out of a frame memory. Second, chrominance fields have to be inserted. Simple field repetition is performed so far.

19. Compatibility feature

Compatibility to MPEG I was not sought for. However, as mentioned in the PPD, there are several possible implementation methods for these compatibilities.

- * simulcast and switchable schemes are possible

The codec is mainly intended to be used for TV and higher quality transmission (EDTV, HDTV). For these applications upward and downward compatibility with different resolutions and window sizes is possible.

20. Random access feature

Random access is guaranteed by using the group of picture concept. One out of 10 frames (720 x 576) is entirely coded in INTRA mode. The maximum access time can be approximated as follows by taking the worst case i.e.

- * 9 frames plus the delay of the decoder

assuming synchronization of the decoder at the beginning of the first inter-frame within a group of frames. The delay of the decoder can be calculated by summarizing all delays mentioned in the implementation study document. In our proposal a small decoder delay results because no interpolative decoding mode is used. The whole delay for random access is nearly 380 msec.

21. Coding/decoding delay

The coding/decoding delay is mainly determined by the buffer-size. For the 9 MBit/s coding scheme the buffer-size was 1600000 bit, thus a maximum delay of 178 msec results. Again, the whole delay can be calculated by summarizing all delays of the coder and decoder mentioned in the implementation study document. In our proposal a decoder delay of about 30 msec results. Thus, the total delay is

- * 208 msec for 9 MBit/s
- * 230 msec for 4 MBit/s

Low coding delay mode implies well-balanced control of the system, hopefully not by using the buffer status as criterion rather than analysing the input image. Subband based coding schemes mostly perform a spectral decomposition of the input image and are well suited to include a signal-adaptive control in order to decrease the buffer size and with that the coding/decoding delay.

22. Statistics

A number of different statistic values have been measured. They are listed in Annex 4. It should be mentioned that the **bits for coding the vectors are included in the bit per frame value of the luminance.**

23. Implementation of Subband Codec

This hardware evaluation document was written as a description of encoder and decoder hardware. The encoder is described in more detail. The decoder circuitry is basically the same. Only the parts that differ from the encoder are described more detailed.

Two aspects have been evaluated: Regarding the topics of the PPD the number of arithmetic operations, memory size, ... as a basis for an estimation of hardware effort was evaluated. Besides that, proposals for the hardware realization have been made and transistor counts as well as chip sizes are given. In most cases these estimates are based on chip realizations at HHI or from other companies and given as a support information. All chip size estimates are made for a 0.8 micron CMOS technology besides the motion compensating predictor (1.2 micron).

This evaluation was made with the goal of a hardware with medium flexibility and high integration scale. Nevertheless the proposal allows the realization of flexible coding systems due to the 16 subband processing scheme. The low data rates in each subband allow parallel sprocessing with more flexible processor architectures.

24. ENCODER

The block diagram of the encoder is shown in Figure 7. Thin lines are control signals, medium lines are pixel data and the thick black lines indicate the processing of the 16 subbands. The 16 channels are not processed with parallel hardware but in a pixelwise sequential manner like in DCT based schemes. Chrominance is processed in parallel with the luminance with the two components C1/C2 being pel-by-pel multiplexed. The processing rate of the chrominance is half the luminance clock rate according to the 4:2:0 scheme.

Each of the sixteen subband channels forms processing blocks of 4×4 pixels. For all sixteen channels the sequence of these blocks forms a so called STRING of 256 pixels.

The overall system delay can be evaluated by adding the single delays of the complete processing chain. It is found to be not critical which is mainly due to the fact that no interpolative coding is done.

Block1: Field Merging

Function: The two fields of the interlaced video input signal (CCIR 601, 4:2:2) are merged to a progressive frame (4:2:0). One chrominance field is skipped and the two chrominance components are merged by pel-by-pel multiplexing. No motion compensation is performed for field merging.

Input: 720*288*50 (luminance, 13.5 MS/s)

Output: 360*288*50 (chrominance, 13.5 MS/s for C1+C2)
720*576*25 (luminance, 13.5 MS/s)
720*288*25 (chrominance, C1+C2 pel-by-pel
multiplexed 6.75 MS/s)

Realization: Asynchronous field buffers with FIFO function and simultaneous Read/Write operations can be used (similar to mPD42270). No address arithmetic is needed only some control clocks for R/W operation. The control signal for this block are generated by the control block 3g as this unit keeps tracks of frames and lines.

Specifications:

Pixel rate (Lum) [MS/s]:	In 13.5; Out 13.5
Pixel rate (Chrom) [MS/s]:	In 13.5; Out 6.75
Word width [bit]:	8
Memory type:	Field buffer chip; FIFO function
" size:	3.33 Mbit for luminance and chrominance
" bandwidth:	324 MBit/s
Chip count:	2-4 memory chips. One 8bit multiplexer
DELAY:	207.936 cycles (about 20 ms)

Advantages: Low chip count, easy control.

Comment: No special features. Any other solution possible.

Block Diagram of Subband based Encoder

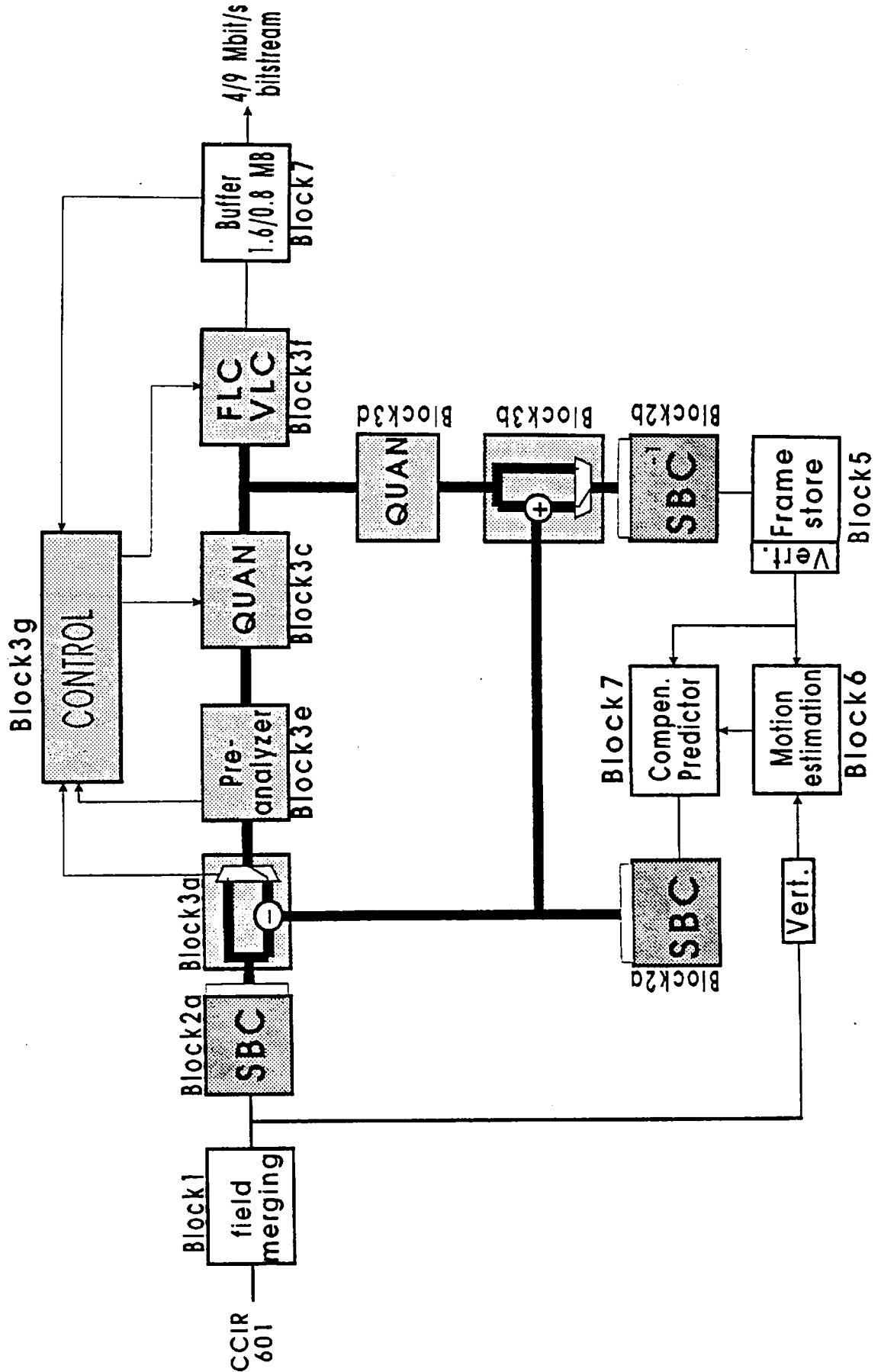


Figure 7: Block diagram of Subband Encoder

25. Subband Splitting Block Diagram (Fig. 8):

The functional block diagram shows the use of different filter hardware blocks in the subband splitting scheme. As the data rate in each section is different, various hardware structures are used to reduce the number of arithmetic operations (mainly multiplications) and to decrease the amount of line delays.

As the field sampling structure is 4:2:0, the chrominance filtering is processed at half of the luminance speed. C1 and C2 are multiplexed pel-by-pel so that for horizontal filtering switchable filters are used, whereas the vertical filter structures don't need to be modified compared to the luminance filter blocks. The chrominance components are processed with the same architecture. The filters for horizontal filtering are switchable for the processing of the two chrominance components.

In Section A and B of Fig. 8 filtering is done with parallel hardware. Low data rates in section C&D allow the use of sequentially operating MAC-structures for filtering.

Luminance filters (horizontal, vertical, analysis and synthesis) are 9 tap filters whereas chrominance needs only 5 tap filters normally. For the sake of regularity in chip design it is useful to process the chrominance signal with the same 9 tap filter type. With the proposed filter moduls, the number of multiplications is reduced by a factor of 4 for horizontal low and high pass filters. For vertical filtering a reduction factor of two is achieved. The coefficient word length is 14 bit (including sign). The data width is reduced to 12 bit at the output of each filter stage but the internal accuracy of the filters is high enough (12*14 multiplication and 20 bit accumulation).

Line delays are shared in the vertical low and high pass filters. As the direct form of the FIR filter is used for vertical filtering the word width for the line delays is reduced to the input data width (12 bit).

Multiplier layout is optimized according to the fact that the coefficients are fixed.

A parallel to serial data formatter and a control block is included at the output of the chip although not drawn in the diagram. This block is extremely important to build 4*4 blocks in each channel and to perform different scanning modes for the latter processing. (4*4 blocks are scanned horizontally, vertically or diagonally. Line delays, multiplexers and a small register set is necessary for this data sorting process.

Two different chip designs for SBC and SBC⁻¹ are necessary.

A second proposal using polyphase filters is shown in the lower half of Fig. 8. The main advantages of the polyphase approach are the reduction of processing speed because the subsampling is done before the filtering. The symmetrical splitting of the HHI proposal allows direct 4band splitting. Row/Column conversion is only needed once and saves memory.

Hardware Block Diagram for 2D symmetrical 16 Band Splitting

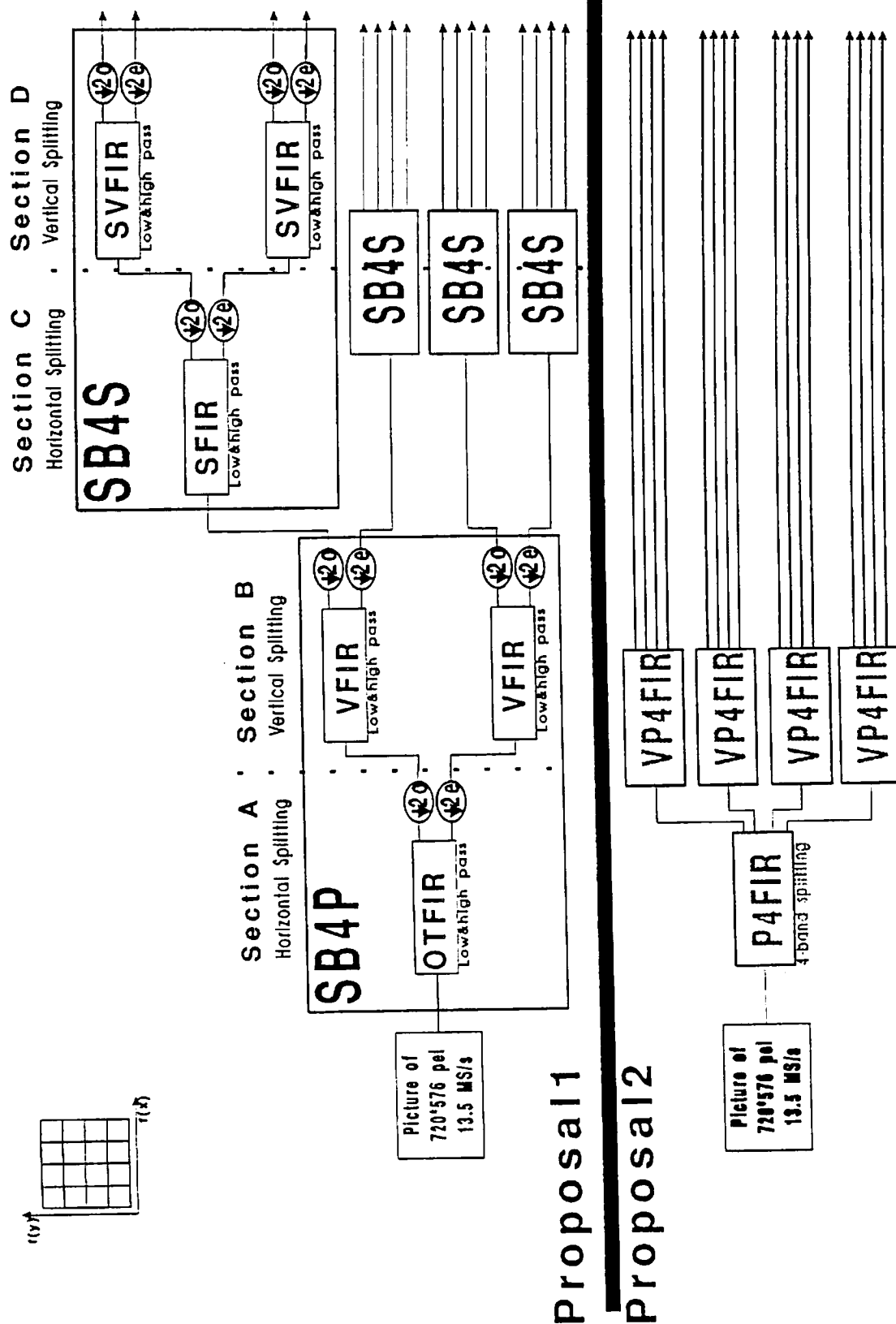


Fig.8: Block diagrams of two alternative subband splitting realizations

Block 2a: Subband Splitting (proposal 1 of Fig. 8)

Function: The input signal is split into sixteen subbands (channels) by FIR filtering (see Fig.2).

Input: 8 bit luminance, 13.5 MS/s

8 bit chrominance, 6.75 MS/s C1/C2.

Clock, Sync, ...

Output: 10 bit luminance, $16 * 0.845$ MHz, blocks of 4*4 pixel

10 bit chrominance, $16 * 0.422$ MHz, blocks of 4*4 pixel

Realization: Full-custom-design VLSI IC. Optimized structures for FIR-filtering are implemented on the chip. Optimized FIR filter structures for each step of the subband decomposition process minimizing delays, number of multiplications or processing speed are used.

In each of the 16 output channels pixels are sorted to form blocks of 4*4 pixel (relating to 16*16 block in the original frame).

The vertical, horizontal or diagonal scanning of the blocks and subbands is done by the output data formatter. 100 kbits of memory and control functions are needed for this process. All 16 subbands are output sequentially to save pins.

Specifications:

Pixel rate (LUM) [MS/s]:	In 13.5 down to 0.42
Pixel rate (Chrom) [MS/s]:	In 6.75 down to 0.21
Word width [bit]:	In 8, 12 bit after each filter bank
Multipl./second; width [bit]:	463 M/s (many fixed multipliers)
Additions/second; width [bit]:	1450 M/s
Memory type:	line delays and FIFOs on chip
" size:	340.000 bit
Transistors:	1.285.000
Chip area:	121 mm ²
Package:	64 pins PLCC
Inputs:	8 bit data, clock, sync
Outputs:	10 bit data, sync
Delay:	5778 cycles (13.5 MHz)

Comment: 80% of chip size is memory size. For the use of tricks see the remarks on key symbols on next page.

Advantages: Regular splitting structure leads to only one fixed data rate for all subbands.

Comments: Polyphase realization of proposal two will reduce chips size due to the saving of memory but was not implemented up to now.

Block2b: Subband synthesis

Inverse process of block 2a with similar complexity but different design.

Comments on the key symbols for subband diagram (Fig. 9):

Sample picture: Serves to clarify data sequences. 'A0,A1,A2' indicate horizontal scanning whereas 'A0,B0,C0, A1,B1,C1 ...' is a typical sequence at the input of a vertical filter.

Subsampling: The downward arrow stands for subsampling, an upward arrow for upsampling. The figure behind denotes the factor for up/down sampling. A letter 'e' or 'o' is given to specify the phase of subsampling if necessary. Vertical subsampling makes use of FIFOs that are included in the calculations but not drawn in the block diagram.

FIFO: First In First Out, used for delays with asynchronous read/write operations (as necessary with vertical polyphase filters).

DELAY: Synchronous FIFO mostly used for line delay.

DFIR: Direct form FIR filter.

TFIR: Transposed FIR filter structure. Advantageous for longer filters because the $N-1$ additions are pipelined and so the additions no longer form a timing critical data path.

OTFIR: Optimized Transposed FIR filter structure. The symmetries of the filter coefficients halve the number of multiplications. As the high pass coefficients differ only in sign, no multiplications are needed for the high pass filter what again halves the number of multiplications. As the coefficients are fixed, the design of the multipliers can be very space efficient (half size or smaller depending on coefficient).

SFIR: Sequential FIR filter structure. Low data rates in the latter stages of subband splitting allow the sequential processing of the filter arithmetic. This reduces the number of hardware multipliers to one per filter. Low and high pass coefficient symmetries can be utilized (see above).

PFIR: Polyphase realization of FIR filter. This structure is advantageous if the input data rate is too high, as the subsampling is done before the filtering. This reduces processing speed requirements by a factor of two. The standard FIR filter is broken into two parts of half complexity plus one adder and subtractor to achieve the low and high pass results.

VFIR: Vertical FIR filter structure. The direct form structure is proposed for vertical filtering as the cost expensive line delays can be shared between the low pass and high pass. No additional multipliers are necessary for the high pass filter due to coefficient symmetries.

SVFIR: Sequential Vertical FIR filter structure. When data rates are low, the vertical filter can be implemented using a sequential MAC structure. Only one multiplier and two accumulators are needed for efficient implementation of the low and high pass. The outputs of the line delays for vertical filtering are multiplexed at the input of the multiplier. The pel-by-pel multiplexing of the two chrominance components allows the use of exactly the same structure without any additional switchings in the filter for the processing of the two chrominance components as in vertical filtering: pixel A0,B0,C0, ... belong to chrominance component C1 and pixel A1,B1,C1, ... belong to chrominance component C2.

P4FIR, VP4FIR: Fourband DCT-based polyphase realization of FIR filters. This structure allows further reduction of speed and memory effort but has not been implemented yet.

Key to the Symbols of the Block Diagrams

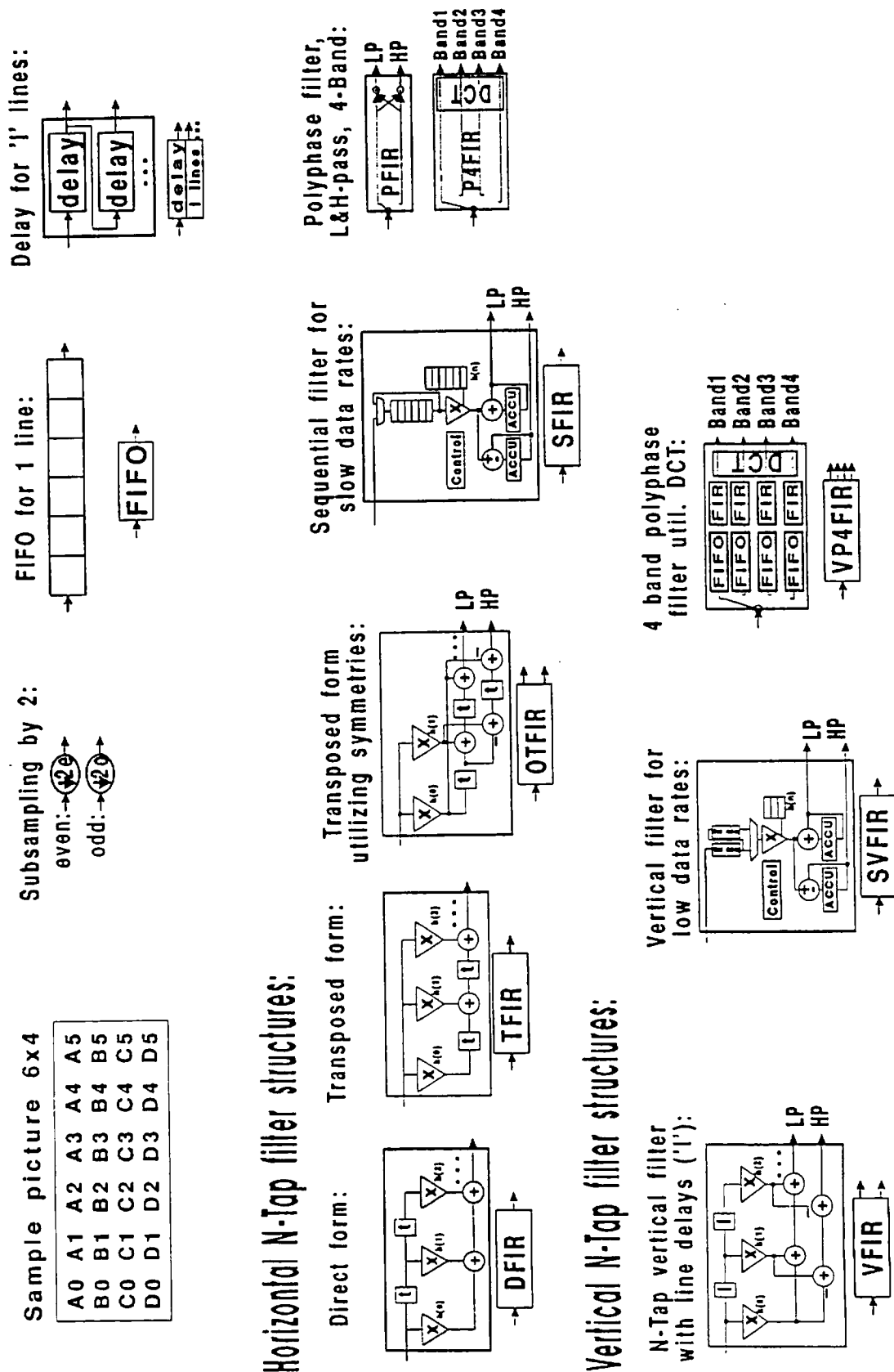


Fig.9: Key symbol table for subband block diagram

Block 3a: Intra/inter decision and multiplexing

Function: Depending whether the sum of absolute values in a 4*4 block of the original input is greater than the sum of absolute values of the pixelwise difference of original input and predicted input the inter mode or the intra mode is chosen.

Sixteen 4*4 blocks form a so called STRING of 256 pixel in which the intra/inter switching is performed only once. Only one four bit code per string must be generated as overhead information.

The 4-Mbit mode uses weighting of the high frequency subbands. Weighting can be added at this block using a multiplier with a register set for weighting factor. Cost is about 0.6 mm²

Input: 10 bit luminance, 13.5 MS/s
10 bit chrominance, 6.75 MS/s

Output: 11 bit luminance,
11 bit chrominance,

Realization: Part of the BLOCK3 full-custom-design chip. Two adders, a comparator, a multiplexer and short FIFOs are needed.

Specifications:

Pixel rate (LUM) [MS/s]:	In 13.5
Pixel rate (Chrom) [MS/s]:	In 6.75
Word width [bit]:	In 10, Out 11
Additions/second; width [bit]:	40.5 M/s; 10 bit
Transistors:	2500
Chip area:	0.45 mm ²
Delay:	17 cycles (13.5 MHz)

Block 3b: Intra/Inter mode multiplexing

Function: This multiplexer is controlled by the block 3a intra/inter decision (via CONTROL) with the appropriate delay (related to the data). Predicted frame pixels are added in inter mode. Realization is close to block 3a and the but with half complexity.

Input: 11 bit luminance, 13.5 MS/s
11 bit chrominance, 6.75 MS/s

Output: 12 bit luminance,
12 bit chrominance,

Realization: Part of the BLOCK3 full custom design chip.

Specifications:

Additions/second; width [bit]:	20.25 M/s; 11 bit
Transistors:	400
Chip area:	0.1 mm ²
Delay:	1 cycle (13.5 MHz)

Block 3c: Quantization

Function: Adaptive linear quantization in all channels. For inter/intra coding and luminance/chrominance 96 fixed coefficient sets (each set containing 1 coefficient for each subband) are used. Easy selection of different quantization factors by inter/intra decision and buffer control. Quantization factor sets may change only for complete 4*4 blocks within a 256 pixel string. Quantizer control is done depending on preanalyzer output and buffer level (see block Preanalyzer). Quantization factors are in the range of 1 to 1/127

Input: 11 bit luminance, 13.5 MS/s; 11 bit chrominance, 6.75 MS/s
Output: 8 bit luminance; 8 bit chrominance,
Realization: Part of the BLOCK3 full custom design chip. Linear quantization can easily be performed by two multipliers (lum/chrom).

Specifications:

Pixel rate (LUM) [MS/s]:	In 13.5
Pixel rate (Chrom) [MS/s]:	In 6.75
Word width [bit]:	In 11, Out 8
Multipl./second; width [bit]:	20.25 M/s ; 11*7
Table sizes:	$3*32*16*7 = 10.752$ bit coefficients
Table lookups:	0.1 M/s
Transistors:	70.000
Chip area:	6 mm^2
Delay:	2 cycles (13.5 MHz)

Advantages: Linear Quantization reduces table sizes, as only some multiplication factors need to be stored.

Block 3d: Quantization⁻¹

Function: Inverse process to block 3c.

Input: 11 bit luminance, 13.5 MS/s; 11 bit chrominance, 6.75 MS/s

Output: 8 bit luminance; 8 bit chrominance,

Realization: All parameters similar to Quantizer.

Block 3e: Preanalyzer

Function: Blocks of 4*4 pels are analyzed to find an appropriate quantizer. Preanalysis counts the number of values above and below a threshold as an estimate of VLC and RLC output. The comparison with 32 threshold values is done in parallel. The result of this analysis together with the buffer level information determines the quantizer set used. A five bit overhead information is generated for a string of 256 bits.

Input: 11 bit luminance, 13.5 MS/s; 11 bit chrominance, 6.75 MS/s

Output: 8 bit luminance; 8 bit chrominance,

Realization: Part of the BLOCK3 full custom design chip. 64 parallel counters and adders are used

Specifications:

Pixel rate (LUM) [MS/s]:	In 13.5
Pixel rate (Chrom) [MS/s]:	In 6.75
Word width [bit]:	11
Additions/second; width [bit]:	1200 M/s ; 10
Transistors:	25.000
Chip area:	3.5 mm^2
Delay:	20 cycles (13.5 MHz)

Advantages: This block is only used in encoder.

Block 3f: Coder (FLC, VLC, RLC)

Function: Entropie coding is done with an 1-dimensional Huffman code with a maximum code length of 16 bit. Entropie coding is applied to pixel data and motion vectors. The coding is done across a string (256 pixel) starting with the lowest subband. The function of FLC, VLC and RLC are quite well known and not further described. Basically 8 different "tables" (inter/intra * 4 frequency zones) are used.

Input: 8 bit luminance, 13.5 MS/s; 8 bit chrominance, 6.75 MS/s C1/C2

Output: bitstream

Realization: Part of the BLOCK3 full custom design chip. Table sizes are drastically reduced using a special structure for the Huffman code (sorted). The complexity values given below are based on the VLC/RLC codec currently under design at HHI. As this chip is a Gate-Array design, transistor complexity is based on a gate equivalent of 4. Optimization can be done with full-custom. The decoder is much less complex!

Specifications:

Pixel rate (LUM) [MS/s]:	In 13.5 down to 0.42
Pixel rate (Chrom) [MS/s]:	In 6.75 down to 0.21
Logic gates:	9000 gates
Table memory type:	18.592 gates registers
Table sizes:	$8 \times 300 + 8 \times 32 = 2656$ bits
Transistors:	110.000 (gate equivalent = 4)
Chip area:	10 mm^2
Delay:	4 cycles (13.5 MHz)

Advantages: Simple decoder.

Block 3g: Control

Function: CONTROL is needed for managing the overhead information (4bit subband address of intra/inter switching, 5bit address for quantizer, motion vectors ...). Overhead information is inserted to the data stream in the FLC/VLC block.

CONTROL sums the number of bits generated by the VLC per string and updates the thresholds for quantization. Gain or loss is propagated and shared for the next 16 strings and from predicted frame to predicted frame as well as from inter frame to next inter frame.

CONTROL counts frames and lines and thereby generates some sync signals (for field merging and SBC too)

Control keeps track of delays inherent to some processing units and propagates control information adequately.

Control contains FIFOs to resort the top-down string (high pass to low pass) of 256 pixels to a bottom-up string (low pass to high pass) before coding.

Input: several values and control signals, microprocessor interface

Output: control signals mainly plus some data

Realization: Part of the BLOCK3 full custom design chip. CONTROL was not evaluated in detail but it is arithmetically uncritical. A hard wired control hardware could be designed or a processor could be used for control operations. The microprocessor solution would lead to a more flexible implementation that could also provide downloading of quantization coefficients and VLC codes.

Specifications:

Transistors:	100.000
Chip area:	$6\text{-}7 \text{ mm}^2$
Delay:	---

Block 4: Coded data buffer

Function: Well known.

Input: packed bit stream

Output: constant data rate 4/9Mbit/s

Realization: Available FIFO chips.

Specifications:

buffer size:

1.6 Mbit (9Mbit/s); 0.8 Mbit (4Mbit/s)

Delay:

140 ms (encoder+decoder buffer)

Blocks 5-7: Motion estimation/compensation

Function: Motion estimation and motion compensated prediction. There parameters for motion estimation in our scheme are quite typical and hardware effort is not evaluated to detailed:

Motion estimation is performed between original and decoded frame. Reference block size is 8*8, search area size is 24*24. Full search block matching is performed to find a motion vector. A half pel accurate vector is calculated in the direct neighbourhood of pel vector.

Realization: The hardware effort estimated for block 6 is based on Thomson's STI3220 which can be modified for subpel calculation. Motion compensation (block 7) is based on another Thomson developement which was presented on the "Fourth International Workshop of HDTV and beyond" in Torino (Italy) in september of this year. The parameters of these chips are given on the next pages.

Block 5: Frame store and vertical scanning block

Function: Delay of one frame minus the delay that occurred in the processing chain. The same memories as for the field merging can be used. At the output of the the frame store (component `Vert` in Fig. 7) 3 blocks with a delay of 8 lines are added. The first block converts from horizontal to vertical scanning and the other two blocks with 8 line delays are necessary to feed the motion compensating predictor with the search area pixel. The search area memory on that chip is thereby continuously updated

Input: 8 bit luminance, 13.5 MS/s

8 bit chrominance, 6.75 MS/s C1/C2

Output: 3*8 bit luminance, 8 vertically scanned pixels

3*8 bit chrominance, 8 vertically scanned pixels

Realization: Asynchronous field buffers (see block 1, field merging). One row column conversion module plus 2 delays for 8 lines each. This module can be build with line delays.

Specifications:

Pixel rate (LUM) [MS/s]:	In 13.5
Pixel rate (Chrom) [MS/s]:	In 6.75
Word width [bit]:	8
Memory type:	Field buffer chip; FIFO function
" size:	3.33 Mbit for luminance&chrominance
" bandwidth:	324 MBit/s
Chip count:	2-4 memory chips.
DELAY:	40ms minus delay of processing chain
Memory type:	Three * 8 line delay.
" size:	276.480 bit
" bandwidth:	324 MBit/s
Chip area:	55 mm ² .

Advantages: The vertically scanned lines suite to both, the motion estimation chip and the motion compensating predictor.

Comments: Evaluation was based on Thomson chips. Other chips may require a different memory configuration.

Block 6: Motion estimation

Function: See above description of blocks 5-7.

Input: 8 bit luminance, 13.5 MS/s

Output: subpel motion vector, block energy, vector distortions

Realization: 0.8 microns, 3 metal layer CMOS. Full-custom-design for the integer pixel unit; Standard cells, compiled datapaths and RAMs for the controller and the half pixel unit.

Specifications:

Pixel rate (LUM) [MS/s]:	In 13.5
Inputs:	1 for ref. block, 4 for search area scanning column by column
Internal frequency:	27 MHz
Delay:	64 cycles from the last pixel of reference block and the output referring to 13.5 MHz pixel rate.
Transistors:	776.000
Chip area:	125 mm ²
Power dissipation:	3 Watts
Package:	80 pins ceramic

Fig. 10: Diagram of motion estimation chip

Block7: Motion compensation

Function: See above description of blocks 5-7.

Input: 8 bit luminance, 13.5 MS/s

8 bit chrominance, 6.75 MS/s C1/C2 pel-by-pel

Output: Predicted block

Realization: Full-custom-design (1.2 microns, Thomson HCMOS3)

Specifications:

Pixel rate (LUM) [MS/s]:	In 13.5
Inputs:	1 for ref. block, 4 for search area scanning column by column
Outputs:	Predicted data block horizontally scanned
Internal frequency:	27 MHz
Delay:	64 cycles from the last pixel of reference block and the output referring to 13.5 MHz pixel rate.
Transistors:	120.000
Chip area:	49 mm ² (1.2 micron!)
Package:	68 PLCC

26. Decoder

The decoder contains mostly blocks that are known from the encoder. Only differences are pointed out in the subsequent text.

In the decoder the following blocks could be integrated on one chip: Blocks 2a, 2b, 2c, 3b, 6 and the the line memories of the block called 'VERT'. SBC and the inverse process is estimated to need 2-4 chips. Frame store, coded data buffer and the re-interlacing module will be based on available memory chips.

Block1: Buffer Inverse and similar to encoder

Block2a: FLD/VLD

Function: Variable length and fixed length decoding.

Input: bitstream

Output: 8 bit luminance, 13.5 MS/s; 8 bit chrominance, 6.75 MS/s C1/C2 and additional information for control.

Realization: Part of the BLOCK2 chip of decoder. Table sizes are again drastically reduced compared to encoder. The complexity values given below are based on the VLC/RLC codec currently under design at HHI.

Specifications:

Logic gates:	6000 gates
Table memory type:	registers
Table sizes:	120*8 = 960 bits (registers)
Transistors:	40.000 (gate equivalent = 4)
Chip area:	5 mm ²
Delay:	9 cycles (13.5 MHz)

Block 2b: Control. Similar to encoder but less complex

Block 2c: Inverse quantization. Similar to encoder same complexity

Block 2d: Inter/intra switch. Similar to encoder same complexity

Block 3a/b: Subband analysis and synthesis. Similar to encoder same complexity.

Block4: Re-interlacing

Function: The reinterlacing and chrominance demultiplexing can be performed with field buffers like they were used for field merging. 4:2:0 to 4:2:2 is done by field repetition.

Block 5: Frame store and vertical scanning module; Identical with encoder.

Block 6: Motion compensation. The chip used for motion compensated prediction in the encoder can be used here too.

Block Diagram of 16 Band Subband Decoder

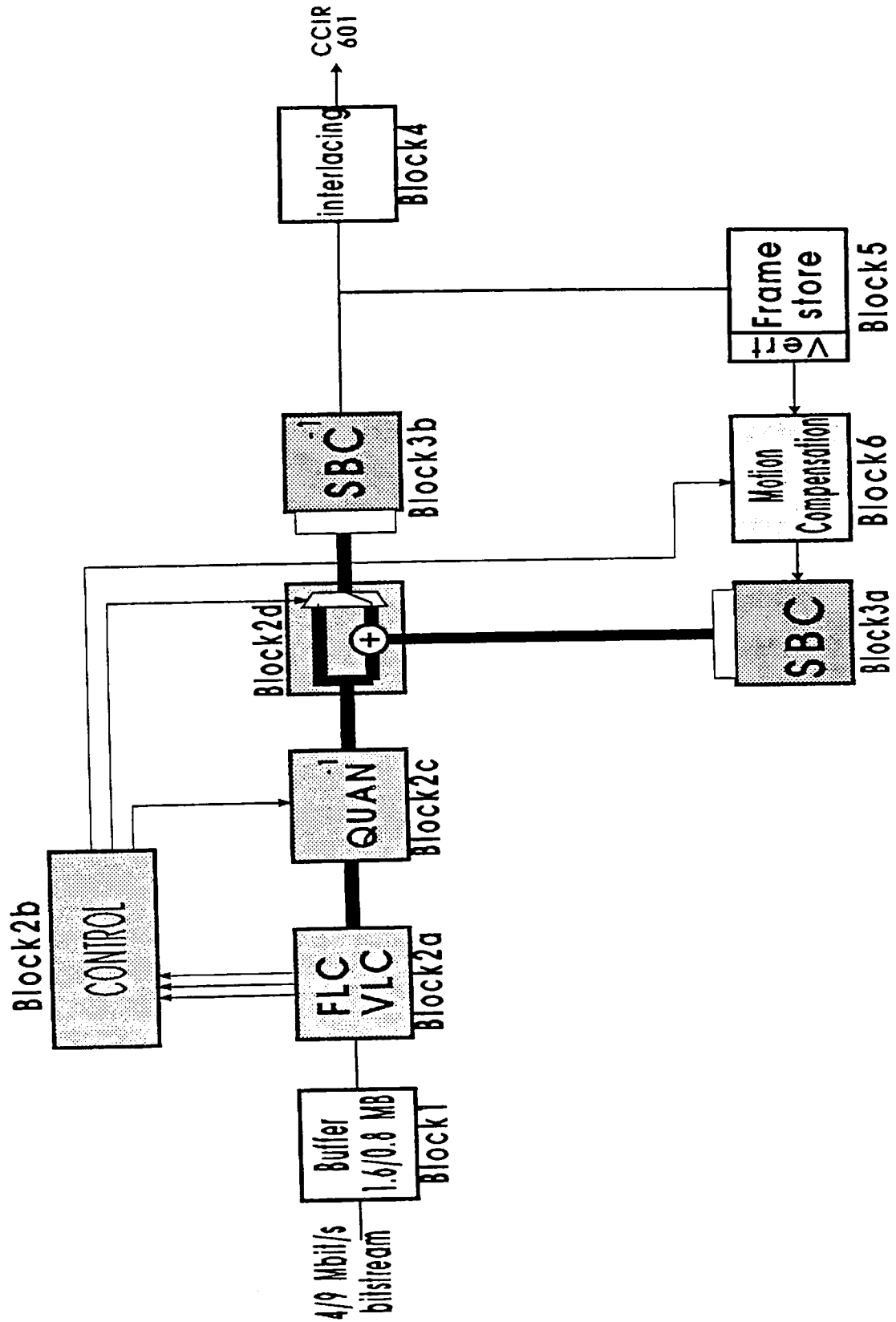


Figure 11: Decoder block diagram

ANNEX 1

Summary specification of 16 channel subband based TV codec for bit-rates up to 10 MBit/s

This proposal is submitted by G. Schamel, Heinrich-Hertz-Institut für Nachrichtentechnik Berlin GmbH and has been developed in the framework of the European VADIS/COST collaboration.

Video input/output:

4:2:2 level of CCIR Recommendation 601, 8 bit resolution

Picture format:

720 x 288 x 50
352 x 288 x 50

Signal preprocessing:

deinterlacing by field merging
4:2:2 to 4:2:0 using field skipping

Coding: General features:

flexibility to adapt to other standards
graceful degradation possible, not implemented
scalable bitstream possible, not implemented
supports different picture sizes and spatial resolutions
high flexibility in bit rates

Modes:

no interpolative coding
only predictive coding
frame based coding
nearly independant coding of luminance and chrominance
10 frames refresh cycle, i.e. intraframe coding in frame 1,
11, 21, 31, ...
mixed intra/inter-frame coding in all non-intra frames

Subband processing:

regular 16 channel splitting
separable filtering and subsampling
short (< 10 taps) tap filters for luminance and chrominance

filtering realized in polyphase structure to minimize
memory and arithmetics
realization of subband splitting with DCT chip is feasible

Lowpass processing:

redundancy reduction in the lowpass signal by processing a
4x4 pixel domain

Subband weighting:

due to out-of-loop subband splitting, weighting of subband
signals is realized in 4 MBit/s version

Pixel scanning:

blocks of 4x4 pixels are scanned
diagonal pixel scanning in the lowpass
vertical pixel scanning of horizontal frequencies
horizontal pixel scanning of vertical frequencies
diagonal scanning of remaining frequencies

Subband scanning:

zig-zag like subband scanning
vertical motion aliasing due to field merging is considered

Prediction and motion compensation:

predictive coding similar to hybrid DCT
subband reconstruction in the loop
subband splitting in the loop
prediction on full picture size
blocks of 8x8 pixels according to interframe mode are
processed, a reference block is taken from the position of
the current block by application of a displacement vector

Motion estimation:

motion vector calculation between original and decoded
image
motion vector calculation within two field merged frames
block size is 8x8
search area is -12 ... +12 in both directions
full search block matching
half-pel vectors are calculated from the initial pel vector
median filter postprocessing of vectors

Intra/inter decision:

one decision for 16x16 pixels of the full picture

one decision for all 16 subbands, i.e. one address has to be transmitted (4 bit fixed word length)
 sum of 4x4 absolute pixel values is calculated within each (!) subband and compared to the corresponding value of the prediction
 decision process starts at highest subband

Quantization:

linear quantizers
 all subband pixels are quantized with a step size of the quantizer depending both globally on the spatial frequencies and locally on the buffer status
 32 different quantizers to be selected for intra/inter/luminance/chrominance

Variable length coding:

VLCs and RLCs to encode both quantized subband pixel values and motion vectors
 different code tables for intra-inter
 different code tables for luminance and chrominance
 4 code tables for 16 subbands
 run lengths of zero amplitudes across subbands

Buffer memory capacity:

1600000 bits (9MBit/s)
 800000 bits (4 MBit/s)

Buffer control:

buffer is mainly for smoothing intraframe bits
 buffer overflow is avoided by multiplying step-size of quantizers with integer value
 buffer underflow is avoided by selecting finer quantizers (out of the available set)

Local bit rate control:

local bit rate can change within given limits (5%-10%)
 local gain in bit rate is spread over the future image area within an image
 global gain (at end of an image) is given to next image
 chrominance gain is given to next luminance image
 global gain in intra mode is spread over last three inter-lum-images of group of frames

Motion vector processing:

horizontal prediction of each vector component and VLC coding of each component
 subpel vectors are processed in the same way

Overhead information:

4 motion vectors (VLC) for 16x16 pixels within the picture
1 x 5 bit FLC address of selected quantizer
1 x 4 bit FLC address of subband for intra-inter switching

Signal postprocessing:

reinterlacing by subsequent displaying two fields from the
frame store
4:2:0 to 4:2:2 using field repetition

Some additional features

4:2:2 is possible
50 Hz progressive mode is possible
improved de- and re-interlace techniques will improve
performance of coding
different picture sizes and resolutions are easy to be
implemented
scene adaptive coding is possible
separate predictive subband coding is possible and saves
hardware

ANNEX 2

Coefficients of QMF lowpass

.01995
-.04271
-.05224
.29271
.56458
.29271
-.05224
-.04271
.01995

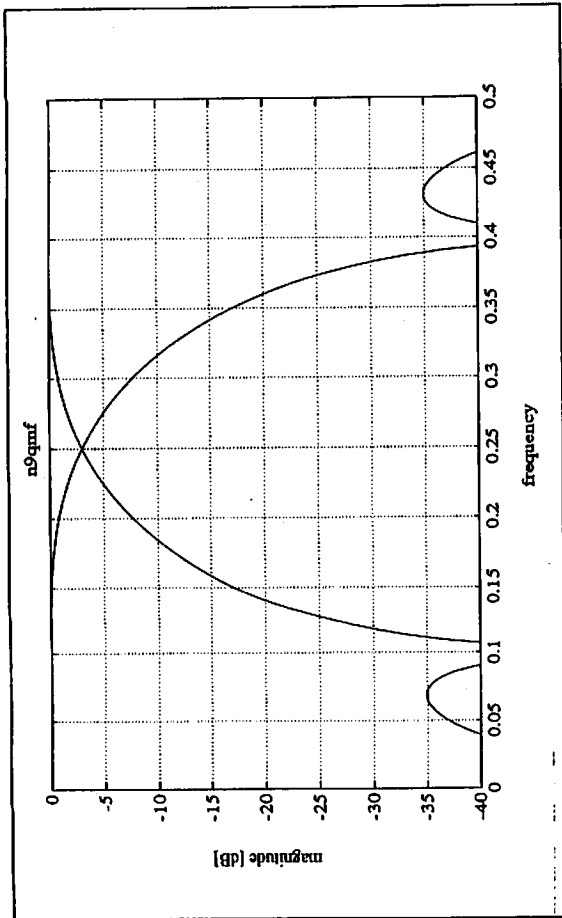


Figure 7: Frequency response of 9 tap quadrature-mirror low- and highpass filter

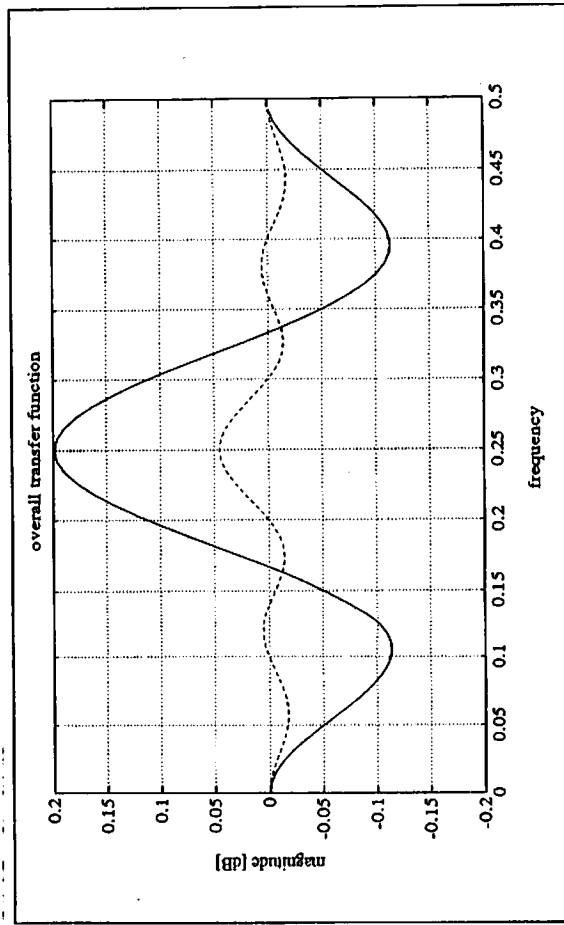


Figure 8: Overall transfer function

ANNEX 3 VLC for motion vectors

no.	probability	word	length	event	code
1	0.000000	0	1	0	000000000
2	0.000000	1	1	1	000000001
3	0.000000	2	1	2	000000010
4	0.000000	3	1	3	000000011
5	0.000000	4	1	4	000000100
6	0.000000	5	1	5	000000101
7	0.000000	6	1	6	000000110
8	0.000000	7	1	7	000000111
9	0.000000	8	1	8	000001000
10	0.000000	9	1	9	000001001
11	0.000000	10	1	10	000001010
12	0.000000	11	1	11	000001011
13	0.000000	12	1	12	000001100
14	0.000000	13	1	13	000001101
15	0.000000	14	1	14	000001110
16	0.000000	15	1	15	000001111
17	0.000000	16	1	16	000010000
18	0.000000	17	1	17	000010001
19	0.000000	18	1	18	000010010
20	0.000000	19	1	19	000010011
21	0.000000	20	1	20	000010100
22	0.000000	21	1	21	000010101
23	0.000000	22	1	22	000010110
24	0.000000	23	1	23	000010111
25	0.000000	24	1	24	000011000
26	0.000000	25	1	25	000011001
27	0.000000	26	1	26	000011010
28	0.000000	27	1	27	000011011
29	0.000000	28	1	28	000011100
30	0.000000	29	1	29	000011101
31	0.000000	30	1	30	000011110
32	0.000000	31	1	31	000011111
33	0.000000	32	1	32	000012000
34	0.000000	33	1	33	000012001
35	0.000000	34	1	34	000012010
36	0.000000	35	1	35	000012011
37	0.000000	36	1	36	000012100
38	0.000000	37	1	37	000012101
39	0.000000	38	1	38	000012110
40	0.000000	39	1	39	000012111
41	0.000000	40	1	40	000013000
42	0.000000	41	1	41	000013001
43	0.000000	42	1	42	000013010
44	0.000000	43	1	43	000013011
45	0.000000	44	1	44	000013100
46	0.000000	45	1	45	000013101
47	0.000000	46	1	46	000013110
48	0.000000	47	1	47	000013111
49	0.000000	48	1	48	000014000
50	0.000000	49	1	49	000014001
51	0.000000	50	1	50	000014010
52	0.000000	51	1	51	000014011
53	0.000000	52	1	52	000014100
54	0.000000	53	1	53	000014101
55	0.000000	54	1	54	000014110
56	0.000000	55	1	55	000014111
57	0.000000	56	1	56	000015000
58	0.000000	57	1	57	000015001
59	0.000000	58	1	58	000015010
60	0.000000	59	1	59	000015011
61	0.000000	60	1	60	000015100
62	0.000000	61	1	61	000015101
63	0.000000	62	1	62	000015110
64	0.000000	63	1	63	000015111
65	0.000000	64	1	64	000016000
66	0.000000	65	1	65	000016001
67	0.000000	66	1	66	000016010
68	0.000000	67	1	67	000016011
69	0.000000	68	1	68	000016100
70	0.000000	69	1	69	000016101
71	0.000000	70	1	70	000016110
72	0.000000	71	1	71	000016111
73	0.000000	72	1	72	000017000
74	0.000000	73	1	73	000017001
75	0.000000	74	1	74	000017010
76	0.000000	75	1	75	000017011
77	0.000000	76	1	76	000017100
78	0.000000	77	1	77	000017101
79	0.000000	78	1	78	000017110
80	0.000000	79	1	79	000017111
81	0.000000	80	1	80	000018000
82	0.000000	81	1	81	000018001
83	0.000000	82	1	82	000018010
84	0.000000	83	1	83	000018011
85	0.000000	84	1	84	000018100
86	0.000000	85	1	85	000018101
87	0.000000	86	1	86	000018110
88	0.000000	87	1	87	000018111
89	0.000000	88	1	88	000019000
90	0.000000	89	1	89	000019001
91	0.000000	90	1	90	000019010
92	0.000000	91	1	91	000019011
93	0.000000	92	1	92	000019100
94	0.000000	93	1	93	000019101
95	0.000000	94	1	94	000019110
96	0.000000	95	1	95	000019111
97	0.000000	96	1	96	000020000
98	0.000000	97	1	97	000020001
99	0.000000	98	1	98	000020010
100	0.000000	99	1	99	000020011
101	0.000000	100	1	100	000020100
102	0.000000	101	1	101	000020101
103	0.000000	102	1	102	000020110
104	0.000000	103	1	103	000020111
105	0.000000	104	1	104	000021000
106	0.000000	105	1	105	000021001
107	0.000000	106	1	106	000021010
108	0.000000	107	1	107	000021011
109	0.000000	108	1	108	000021100
110	0.000000	109	1	109	000021101
111	0.000000	110	1	110	000021110
112	0.000000	111	1	111	000021111
113	0.000000	112	1	112	000022000
114	0.000000	113	1	113	000022001
115	0.000000	114	1	114	000022010
116	0.000000	115	1	115	000022011
117	0.000000	116	1	116	000022100
118	0.000000	117	1	117	000022101
119	0.000000	118	1	118	000022110
120	0.000000	119	1	119	000022111
121	0.000000	120	1	120	000023000
122	0.000000	121	1	121	000023001
123	0.000000	122	1	122	000023010
124	0.000000	123	1	123	000023011
125	0.000000	124	1	124	000023100
126	0.000000	125	1	125	000023101
127	0.000000	126	1	126	000023110
128	0.000000	127	1	127	000023111
129	0.000000	128	1	128	000024000
130	0.000000	129	1	129	000024001
131	0.000000	130	1	130	000024010
132	0.000000	131	1	131	000024011
133	0.000000	132	1	132	000024100
134	0.000000	133	1	133	000024101
135	0.000000	134	1	134	000024110
136	0.000000	135	1	135	000024111
137	0.000000	136	1	136	000025000
138	0.000000	137	1	137	000025001
139	0.000000	138	1	138	000025010
140	0.000000	139	1	139	000025011
141	0.000000	140	1	140	000025100
142	0.000000	141	1	141	000025101
143	0.000000	142	1	142	000025110
144	0.000000	143	1	143	000025111
145	0.000000	144	1	144	000026000
146	0.000000	145	1	145	000026001
147	0.000000	146	1	146	000026010
148	0.000000	147	1	147	000026011
149	0.000000	148	1	148	000026100
150	0.000000	149	1	149	000026101
151	0.000000	150	1	150	000026110
152	0.000000	151	1	151	000026111
153	0.000000	152	1	152	000027000
154	0.000000	153	1	153	000027001
155	0.000000	154	1	154	000027010
156	0.000000	155	1	155	000027011
157	0.000000	156	1	156	000027100
158	0.000000	157	1	157	000027101
159	0.000000	158	1	158	000027110
160	0.000000	159	1	159	000027111
161	0.000000	160	1	160	000028000
162	0.000000	161	1	161	000028001
163	0.000000	162	1	162	000028010
164	0.000000	163	1	163	000028011
165	0.000000	164	1	164	000028100
166	0.000000	165	1	165	000028101
167	0.000000	166	1	166	000028110
168	0.000000	167	1	167	000028111
169	0.000000	168	1	168	000029000
170	0.000000	169	1	169	000029001
171	0.000000	170	1	170	000029010
172	0.000000	171	1	171	000029011
173	0.000000	172	1	172	000029100
174	0.000000	173	1	173	000029101
175	0.000000	174	1	174	000029110
176	0.000000	175	1	175	000029111
177	0.000000	176	1	176	000030000
178	0.000000	177	1	177	000030001
179	0.000000	178	1	178	000030010
180	0.000000	179	1	179	000030011
181	0.000000	180	1	180	000030100
182	0.000000	181	1	181	000030101
183	0.000000	182	1	182	000030110
184	0.000000	183	1	183	000030111
185	0.000000	184	1	184	000031000
186	0.000000	185	1	185	000031001
187	0.000000	186	1	186	000031010
188	0.000000	187	1	187	000031011
189	0.000000	188	1	188	000031100
190	0.000000	189	1	189	000031101
191	0.000000	190	1	190	000031110
192	0.000000	191	1	191	000031111
193	0.000000	192	1	192	000032000
194	0.000000	193	1	193	000032001
195	0.000000	194	1	194	000032010
196	0.000000	195	1	195	000032011
197	0.000000	196	1	196	000032100
198	0.000000	197	1	197	000032101
199	0.000000	198	1	198	000032110
200	0.000000	199	1	199	000032111

no.	probability	word	length	event	code
1	0.000000	0	1	0	000000000
2	0.00				

MOBILE & CALENDAR 9Mbit/s

[illegible]

FLOWER GARDEN 4 Mbit/s

frame 1	0 bits for coding vectors	frame 63	29533 bits for coding vectors
frame 2	37634 bits for coding vectors	frame 64	30607 bits for coding vectors
frame 3	39258 bits for coding vectors	frame 65	32381 bits for coding vectors
frame 4	38513 bits for coding vectors	frame 66	32383 bits for coding vectors
frame 5	39876 bits for coding vectors	frame 67	29982 bits for coding vectors
frame 6	38581 bits for coding vectors	frame 68	29649 bits for coding vectors
frame 7	37129 bits for coding vectors	frame 69	31973 bits for coding vectors
frame 8	36578 bits for coding vectors	frame 70	31844 bits for coding vectors
frame 9	34427 bits for coding vectors	frame 71	0 bits for coding vectors
frame 10	33010 bits for coding vectors	frame 72	32196 bits for coding vectors
frame 11	0 bits for coding vectors	frame 73	31009 bits for coding vectors
frame 12	32785 bits for coding vectors	frame 74	31287 bits for coding vectors
frame 13	32584 bits for coding vectors	frame 75	32418 bits for coding vectors
frame 14	32138 bits for coding vectors	frame 76	32011 bits for coding vectors
frame 15	31919 bits for coding vectors	frame 77	32126 bits for coding vectors
frame 16	30560 bits for coding vectors	frame 78	31220 bits for coding vectors
frame 17	30764 bits for coding vectors	frame 79	32538 bits for coding vectors
frame 18	30226 bits for coding vectors	frame 80	32593 bits for coding vectors
frame 19	30977 bits for coding vectors	frame 81	0 bits for coding vectors
frame 20	30615 bits for coding vectors	frame 82	30730 bits for coding vectors
frame 21	0 bits for coding vectors	frame 83	34649 bits for coding vectors
frame 22	31480 bits for coding vectors	frame 84	34888 bits for coding vectors
frame 23	30968 bits for coding vectors	frame 85	34647 bits for coding vectors
frame 24	31450 bits for coding vectors	frame 86	32337 bits for coding vectors
frame 25	30411 bits for coding vectors	frame 87	30933 bits for coding vectors
frame 26	31810 bits for coding vectors	frame 88	32325 bits for coding vectors
frame 27	31674 bits for coding vectors	frame 89	33902 bits for coding vectors
frame 28	32823 bits for coding vectors	frame 90	33907 bits for coding vectors
frame 29	31163 bits for coding vectors	frame 91	0 bits for coding vectors
frame 30	32029 bits for coding vectors	frame 92	34882 bits for coding vectors
frame 31	0 bits for coding vectors	frame 93	34886 bits for coding vectors
frame 32	33337 bits for coding vectors	frame 94	34640 bits for coding vectors
frame 33	32873 bits for coding vectors	frame 95	34640 bits for coding vectors
frame 34	31352 bits for coding vectors	frame 96	33937 bits for coding vectors
frame 35	32372 bits for coding vectors	frame 97	32082 bits for coding vectors
frame 36	29972 bits for coding vectors	frame 98	34659 bits for coding vectors
frame 37	30191 bits for coding vectors	frame 99	34068 bits for coding vectors
frame 38	32239 bits for coding vectors	frame 100	31113 bits for coding vectors
frame 39	28991 bits for coding vectors	frame 101	0 bits for coding vectors
frame 40	31989 bits for coding vectors	frame 102	34778 bits for coding vectors
frame 41	0 bits for coding vectors	frame 103	34769 bits for coding vectors
frame 42	33963 bits for coding vectors	frame 104	35152 bits for coding vectors
frame 43	34711 bits for coding vectors	frame 105	34820 bits for coding vectors
frame 44	34100 bits for coding vectors	frame 106	37894 bits for coding vectors
frame 45	35014 bits for coding vectors	frame 107	43829 bits for coding vectors
frame 46	32183 bits for coding vectors	frame 108	44618 bits for coding vectors
frame 47	41124 bits for coding vectors	frame 109	40289 bits for coding vectors
frame 48	34679 bits for coding vectors	frame 110	37999 bits for coding vectors
frame 49	32095 bits for coding vectors	frame 111	0 bits for coding vectors
frame 50	31490 bits for coding vectors	frame 112	33907 bits for coding vectors
frame 51	0 bits for coding vectors	frame 113	31614 bits for coding vectors
frame 52	33214 bits for coding vectors	frame 114	31239 bits for coding vectors
frame 53	34860 bits for coding vectors	frame 115	31154 bits for coding vectors
frame 54	31040 bits for coding vectors	frame 116	30774 bits for coding vectors
frame 55	32416 bits for coding vectors	frame 117	31603 bits for coding vectors
frame 56	34090 bits for coding vectors	frame 118	32540 bits for coding vectors
frame 57	32017 bits for coding vectors	frame 119	30491 bits for coding vectors
frame 58	34480 bits for coding vectors	frame 120	29460 bits for coding vectors
frame 59	32010 bits for coding vectors	frame 121	0 bits for coding vectors
frame 60	31114 bits for coding vectors	frame 122	32999 bits for coding vectors
frame 61	0 bits for coding vectors	frame 123	30910 bits for coding vectors
frame 62	29300 bits for coding vectors	frame 124	32148 bits for coding vectors

FLOWER GARDEN 4 Mbit/s

TABLE TENNIS 9 Mbit/s

frame 1	33.40 db for L	frame 56	34.20 db for L	frame 111	34.84 db for CI	frame 166	34.84 db for CI
frame 2	28.83 db for L	frame 57	34.92 db for L	frame 112	37.87 db for CI	frame 167	35.34 db for CI
frame 3	29.37 db for L	frame 58	35.27 db for L	frame 113	38.01 db for CI	frame 168	36.04 db for CI
frame 4	30.94 db for L	frame 59	35.43 db for L	frame 114	38.12 db for CI	frame 169	36.46 db for CI
frame 5	31.32 db for L	frame 60	35.93 db for L	frame 115	38.43 db for CI	frame 170	36.70 db for CI
frame 6	32.38 db for L	frame 61	36.47 db for L	frame 116	39.11 db for CI	frame 171	36.34 db for CI
frame 7	30.80 db for L	frame 62	38.36 db for L	frame 117	39.39 db for CI	frame 172	36.44 db for CI
frame 8	32.40 db for L	frame 63	37.20 db for L	frame 118	39.77 db for CI	frame 173	37.07 db for CI
frame 9	28.98 db for L	frame 64	37.79 db for L	frame 119	40.02 db for CI	frame 174	37.43 db for CI
frame 10	29.34 db for L	frame 65	37.36 db for L	frame 120	40.28 db for CI	frame 175	37.73 db for CI
frame 11	30.95 db for L	frame 66	37.02 db for L	frame 121	40.38 db for CI	frame 176	38.02 db for CI
frame 12	31.71 db for L	frame 67	36.94 db for L	frame 122	40.38 db for CI	frame 177	38.11 db for CI
frame 13	29.74 db for L	frame 68	37.00 db for L	frame 123	40.41 db for CI	frame 178	38.17 db for CI
frame 14	31.42 db for L	frame 69	36.93 db for L	frame 124	40.40 db for CI	frame 179	38.28 db for CI
frame 15	31.14 db for L	frame 70	36.84 db for L	frame 125	40.44 db for CI	frame 180	38.35 db for CI
frame 16	29.47 db for L	frame 71	36.37 db for L	frame 126	38.94 db for CI	frame 181	36.16 db for CI
frame 17	29.34 db for L	frame 72	35.80 db for L	frame 127	39.50 db for CI	frame 182	36.95 db for CI
frame 18	31.71 db for L	frame 73	37.83 db for L	frame 128	39.71 db for CI	frame 183	37.42 db for CI
frame 19	34.38 db for L	frame 74	37.70 db for L	frame 129	39.88 db for CI	frame 184	37.68 db for CI
frame 20	34.31 db for L	frame 75	37.82 db for L	frame 130	39.79 db for CI	frame 185	37.89 db for CI
frame 21	30.33 db for L	frame 76	37.87 db for L	frame 131	40.09 db for CI	frame 186	38.08 db for CI
frame 22	31.93 db for L	frame 77	37.80 db for L	frame 132	40.30 db for CI	frame 187	38.20 db for CI
frame 23	34.60 db for L	frame 78	37.70 db for L	frame 133	40.09 db for CI	frame 188	38.20 db for CI
frame 24	35.41 db for L	frame 79	37.43 db for L	frame 134	40.48 db for CI	frame 189	38.34 db for CI
frame 25	29.53 db for L	frame 80	37.42 db for L	frame 135	40.42 db for CI	frame 190	38.38 db for CI
frame 26	32.49 db for L	frame 81	36.42 db for L	frame 136	40.15 db for CI	frame 191	38.04 db for CI
frame 27	29.98 db for L	frame 82	36.87 db for L	frame 137	40.24 db for CI	frame 192	37.93 db for CI
frame 28	29.97 db for L	frame 83	38.39 db for L	frame 138	35.57 db for CI	frame 193	32.43 db for CI
frame 29	29.44 db for L	frame 84	31.33 db for L	frame 139	36.49 db for CI	frame 194	34.21 db for CI
frame 30	29.45 db for L	frame 85	33.17 db for L	frame 140	37.61 db for CI	frame 195	34.95 db for CI
frame 31	40.32 db for L	frame 86	34.03 db for L	frame 141	38.24 db for CI	frame 196	35.66 db for CI
frame 32	34.99 db for L	frame 87	34.99 db for L	frame 142	38.41 db for CI	frame 197	36.19 db for CI
frame 33	32.97 db for L	frame 88	35.85 db for L	frame 143	38.97 db for CI	frame 198	36.44 db for CI
frame 34	32.04 db for L	frame 89	36.47 db for L	frame 144	39.20 db for CI	frame 199	36.87 db for CI
frame 35	33.71 db for L	frame 90	36.80 db for L	frame 145	39.31 db for CI	frame 200	36.91 db for CI
frame 36	34.13 db for L	frame 91	35.13 db for L	frame 146	40.43 db for CI	frame 201	36.41 db for CI
frame 37	28.23 db for L	frame 92	35.93 db for L	frame 147	40.98 db for CI	frame 202	37.04 db for CI
frame 38	27.95 db for L	frame 93	36.92 db for L	frame 148	41.22 db for CI	frame 203	37.27 db for CI
frame 39	29.11 db for L	frame 94	36.99 db for L	frame 149	41.28 db for CI	frame 204	37.49 db for CI
frame 40	28.01 db for L	frame 95	36.88 db for L	frame 150	41.35 db for CI	frame 205	37.60 db for CI
frame 41	38.56 db for L	frame 96	36.71 db for L	frame 151	41.39 db for CI	frame 206	37.73 db for CI
frame 42	34.43 db for L	frame 97	37.09 db for L	frame 152	41.39 db for CI	frame 207	37.83 db for CI
frame 43	35.70 db for L	frame 98	38.08 db for L	frame 153	41.21 db for CI	frame 208	37.72 db for CI
frame 44	33.90 db for L	frame 99	34.04 db for L	frame 154	40.93 db for CI	frame 209	37.57 db for CI
frame 45	33.18 db for L	frame 100	32.91 db for L	frame 155	40.66 db for CI	frame 210	37.50 db for CI
frame 46	29.00 db for L	frame 101	35.43 db for L	frame 156	42.21 db for CI	frame 211	37.35 db for CI
frame 47	29.83 db for L	frame 102	34.95 db for L	frame 157	41.39 db for CI	frame 212	37.61 db for CI
frame 48	29.49 db for L	frame 103	34.35 db for L	frame 158	40.92 db for CI	frame 213	37.49 db for CI
frame 49	31.68 db for L	frame 104	32.12 db for L	frame 159	40.69 db for CI	frame 214	37.44 db for CI
frame 50	32.01 db for L	frame 105	31.92 db for L	frame 160	40.82 db for CI	frame 215	37.92 db for CI
frame 51	31.90 db for L	frame 106	31.21 db for L	frame 161	40.30 db for CI	frame 216	36.74 db for CI
frame 52	34.17 db for L	frame 107	30.87 db for L	frame 162	40.37 db for CI	frame 217	36.48 db for CI
frame 53	35.13 db for L	frame 108	30.70 db for L	frame 163	40.23 db for CI	frame 218	36.39 db for CI
frame 54	29.37 db for L	frame 109	30.68 db for L	frame 164	40.40 db for CI	frame 219	36.16 db for CI
frame 55	31.40 db for L	frame 110	31.75 db for L	frame 165	40.38 db for CI	frame 220	36.88 db for CI

TABLE TENNIS 9 Mbit/s

Motion vector coding

frame 1: 0 bits for coding vectors
frame 2: 31684 bits for coding vectors
frame 3: 32938 bits for coding vectors
frame 4: 34813 bits for coding vectors
frame 5: 36874 bits for coding vectors
frame 6: 39281 bits for coding vectors
frame 7: 42128 bits for coding vectors
frame 8: 45428 bits for coding vectors
frame 9: 49184 bits for coding vectors
frame 10: 53400 bits for coding vectors
frame 11: 0 bits for coding vectors
frame 12: 32785 bits for coding vectors
frame 13: 32284 bits for coding vectors
frame 14: 32138 bits for coding vectors
frame 15: 31979 bits for coding vectors
frame 16: 30360 bits for coding vectors
frame 17: 30704 bits for coding vectors
frame 18: 30224 bits for coding vectors
frame 19: 30097 bits for coding vectors
frame 20: 30614 bits for coding vectors
frame 21: 0 bits for coding vectors
frame 22: 31480 bits for coding vectors
frame 23: 30948 bits for coding vectors
frame 24: 31440 bits for coding vectors
frame 25: 30611 bits for coding vectors
frame 26: 31615 bits for coding vectors
frame 27: 32674 bits for coding vectors
frame 28: 32833 bits for coding vectors
frame 29: 31463 bits for coding vectors
frame 30: 32039 bits for coding vectors
frame 31: 0 bits for coding vectors
frame 32: 32537 bits for coding vectors
frame 33: 32675 bits for coding vectors
frame 34: 32152 bits for coding vectors
frame 35: 32372 bits for coding vectors
frame 36: 32972 bits for coding vectors
frame 37: 30191 bits for coding vectors
frame 38: 32239 bits for coding vectors
frame 39: 32851 bits for coding vectors
frame 40: 31969 bits for coding vectors
frame 41: 0 bits for coding vectors
frame 42: 32965 bits for coding vectors
frame 43: 32731 bits for coding vectors
frame 44: 32160 bits for coding vectors
frame 45: 32614 bits for coding vectors
frame 46: 32183 bits for coding vectors
frame 47: 32124 bits for coding vectors
frame 48: 32478 bits for coding vectors
frame 49: 32095 bits for coding vectors
frame 50: 32100 bits for coding vectors
frame 51: 0 bits for coding vectors
frame 52: 32124 bits for coding vectors
frame 53: 32460 bits for coding vectors
frame 54: 32140 bits for coding vectors
frame 55: 32116 bits for coding vectors
frame 56: 32400 bits for coding vectors
frame 57: 32027 bits for coding vectors
frame 58: 32440 bits for coding vectors
frame 59: 32080 bits for coding vectors
frame 60: 32114 bits for coding vectors
frame 61: 0 bits for coding vectors
frame 62: 32300 bits for coding vectors

frame 63: 29333 bits for coding vectors
frame 64: 30607 bits for coding vectors
frame 65: 32161 bits for coding vectors
frame 66: 32383 bits for coding vectors
frame 67: 32982 bits for coding vectors
frame 68: 32649 bits for coding vectors
frame 69: 31975 bits for coding vectors
frame 70: 31664 bits for coding vectors
frame 71: 0 bits for coding vectors
frame 72: 32156 bits for coding vectors
frame 73: 31009 bits for coding vectors
frame 74: 31547 bits for coding vectors
frame 75: 32118 bits for coding vectors
frame 76: 32011 bits for coding vectors
frame 77: 31216 bits for coding vectors
frame 78: 31120 bits for coding vectors
frame 79: 32258 bits for coding vectors
frame 80: 32383 bits for coding vectors
frame 81: 0 bits for coding vectors
frame 82: 30730 bits for coding vectors
frame 83: 31649 bits for coding vectors
frame 84: 30886 bits for coding vectors
frame 85: 31337 bits for coding vectors
frame 86: 31337 bits for coding vectors
frame 87: 30333 bits for coding vectors
frame 88: 31235 bits for coding vectors
frame 89: 32405 bits for coding vectors
frame 90: 32607 bits for coding vectors
frame 91: 0 bits for coding vectors
frame 92: 32725 bits for coding vectors
frame 93: 32882 bits for coding vectors
frame 94: 32668 bits for coding vectors
frame 95: 32460 bits for coding vectors
frame 96: 32377 bits for coding vectors
frame 97: 32082 bits for coding vectors
frame 98: 32469 bits for coding vectors
frame 99: 32665 bits for coding vectors
frame 100: 32113 bits for coding vectors
frame 101: 0 bits for coding vectors
frame 102: 32478 bits for coding vectors
frame 103: 32169 bits for coding vectors
frame 104: 32152 bits for coding vectors
frame 105: 32620 bits for coding vectors
frame 106: 32894 bits for coding vectors
frame 107: 32821 bits for coding vectors
frame 108: 32619 bits for coding vectors
frame 109: 32408 bits for coding vectors
frame 110: 32799 bits for coding vectors
frame 111: 0 bits for coding vectors
frame 112: 32807 bits for coding vectors
frame 113: 32614 bits for coding vectors
frame 114: 32137 bits for coding vectors
frame 115: 32134 bits for coding vectors
frame 116: 32724 bits for coding vectors
frame 117: 31405 bits for coding vectors
frame 118: 32340 bits for coding vectors
frame 119: 32492 bits for coding vectors
frame 120: 32480 bits for coding vectors
frame 121: 0 bits for coding vectors
frame 122: 32999 bits for coding vectors
frame 123: 32910 bits for coding vectors
frame 124: 32168 bits for coding vectors

POPPLE 9 MBit/s

frame 1: 34.76 db for L 42.01 db for C1 38.83 db for C2
frame 2: 31.35 db for L 36.84 db for C1 35.13 db for C2
frame 3: 32.23 db for L 36.61 db for C1 35.30 db for C2
frame 4: 31.06 db for L 36.05 db for C1 34.80 db for C2
frame 5: 32.96 db for L 36.21 db for C1 35.02 db for C2
frame 6: 31.96 db for L 35.79 db for C1 34.48 db for C2
frame 7: 32.74 db for L 35.83 db for C1 34.34 db for C2
frame 8: 32.79 db for L 35.74 db for C1 34.13 db for C2
frame 9: 32.79 db for L 35.64 db for C1 34.17 db for C2
frame 10: 32.79 db for L 35.58 db for C1 34.17 db for C2
frame 11: 34.65 db for L 42.31 db for C1 38.88 db for C2
frame 12: 32.63 db for L 36.88 db for C1 35.13 db for C2
frame 13: 32.21 db for L 36.40 db for C1 35.16 db for C2
frame 14: 32.02 db for L 36.11 db for C1 34.40 db for C2
frame 15: 32.05 db for L 36.04 db for C1 34.43 db for C2
frame 16: 32.02 db for L 36.04 db for C1 34.37 db for C2
frame 17: 32.02 db for L 36.17 db for C1 34.50 db for C2
frame 18: 32.08 db for L 36.04 db for C1 34.34 db for C2
frame 19: 32.09 db for L 35.75 db for C1 34.24 db for C2
frame 20: 32.37 db for L 42.18 db for C1 38.70 db for C2
frame 21: 32.37 db for L 36.23 db for C1 34.96 db for C2
frame 22: 32.36 db for L 36.26 db for C1 35.00 db for C2
frame 23: 32.36 db for L 36.82 db for C1 34.31 db for C2
frame 24: 32.38 db for L 36.70 db for C1 34.31 db for C2
frame 25: 32.79 db for L 35.44 db for C1 34.24 db for C2
frame 26: 32.82 db for L 35.93 db for C1 34.27 db for C2
frame 27: 32.86 db for L 35.93 db for C1 34.11 db for C2
frame 28: 32.87 db for L 35.86 db for C1 34.33 db for C2
frame 29: 32.77 db for L 35.98 db for C1 34.19 db for C2
frame 30: 32.77 db for L 42.45 db for C1 35.25 db for C2
frame 31: 34.59 db for L 36.43 db for C1 35.25 db for C2
frame 32: 33.48 db for L 35.86 db for C1 34.74 db for C2
frame 33: 33.10 db for L 35.83 db for C1 34.54 db for C2
frame 34: 32.77 db for L 35.44 db for C1 34.13 db for C2
frame 35: 32.54 db for L 35.58 db for C1 34.17 db for C2
frame 36: 32.59 db for L 35.58 db for C1 34.03 db for C2
frame 37: 32.48 db for L 35.70 db for C1 34.23 db for C2
frame 38: 32.32 db for L 35.70 db for C1 34.23 db for C2

frame 39: 32.43 db for L 35.61 db for C1 34.06 db for C2
frame 40: 32.44 db for L 35.73 db for C1 34.24 db for C2
frame 41: 34.77 db for L 42.42 db for C1 35.10 db for C2
frame 42: 33.37 db for L 36.66 db for C1 35.18 db for C2
frame 43: 32.94 db for L 36.49 db for C1 34.89 db for C2
frame 44: 31.94 db for L 36.10 db for C1 34.95 db for C2
frame 45: 31.90 db for L 36.04 db for C1 34.49 db for C2
frame 46: 31.33 db for L 35.73 db for C1 34.14 db for C2
frame 47: 31.27 db for L 35.94 db for C1 34.31 db for C2
frame 48: 31.33 db for L 35.62 db for C1 34.23 db for C2
frame 49: 30.00 db for L 35.72 db for C1 34.00 db for C2
frame 50: 29.86 db for L 35.75 db for C1 33.92 db for C2
frame 51: 34.35 db for L 42.32 db for C1 38.64 db for C2
frame 52: 31.41 db for L 36.67 db for C1 34.63 db for C2
frame 53: 31.01 db for L 36.02 db for C1 34.34 db for C2
frame 54: 31.01 db for L 35.88 db for C1 34.18 db for C2
frame 55: 30.64 db for L 35.50 db for C1 34.11 db for C2
frame 56: 30.07 db for L 35.77 db for C1 34.29 db for C2
frame 57: 30.37 db for L 35.31 db for C1 34.13 db for C2
frame 58: 30.13 db for L 35.33 db for C1 34.32 db for C2
frame 59: 30.39 db for L 35.20 db for C1 34.04 db for C2
frame 60: 30.39 db for L 35.14 db for C1 34.24 db for C2
frame 61: 34.19 db for L 43.29 db for C1 41.17 db for C2
frame 62: 32.83 db for L 35.95 db for C1 35.26 db for C2
frame 63: 32.32 db for L 35.25 db for C1 34.56 db for C2
frame 64: 32.39 db for L 35.25 db for C1 34.30 db for C2
frame 65: 32.10 db for L 35.25 db for C1 34.43 db for C2
frame 66: 32.38 db for L 35.03 db for C1 33.86 db for C2
frame 67: 32.16 db for L 34.81 db for C1 33.82 db for C2
frame 68: 32.01 db for L 34.69 db for C1 33.98 db for C2
frame 69: 32.33 db for L 34.53 db for C1 33.90 db for C2
frame 70: 32.33 db for L 34.81 db for C1 33.94 db for C2
frame 71: 34.32 db for L 43.40 db for C1 41.39 db for C2
frame 72: 34.37 db for L 35.16 db for C1 34.56 db for C2
frame 73: 33.74 db for L 34.50 db for C1 33.97 db for C2
frame 74: 32.21 db for L 34.31 db for C1 34.09 db for C2

frame100: 1436633 bits 81409 bits 429615 bits 244390 bits 1600977 bits
 frame110: 1501739 bits 88993 bits 507433 bits 307433 bits 1761791 bits
 frame120: 1710084 bits 961937 bits 582079 bits 316079 bits 1921100 bits

CUMULATIVE BIT COUNT (CBC) AFTER 10 FRAMES OF MOB 9 Kbit/s

frame 10: 324242 bits 140175 bits 132747 bits 2588707 bits
 frame 20: 458049 bits 201847 bits 167934 bits 7174746 bits
 frame 30: 597923 bits 423094 bits 400732 bits 10757646 bits
 frame 40: 731945 bits 593104 bits 520484 bits 14759746 bits
 frame 50: 864151 bits 698024 bits 618764 bits 17848237 bits
 frame 60: 973699 bits 787669 bits 726474 bits 21477907 bits
 frame 70: 1078522 bits 871390 bits 800870 bits 25463374 bits
 frame 80: 1178522 bits 9450017 bits 871390 bits 30000000 bits
 frame 90: 1278522 bits 10200000 bits 9450017 bits 34650000 bits
 frame100: 1378522 bits 10950000 bits 10200000 bits 39300000 bits
 frame110: 1478522 bits 11700000 bits 10950000 bits 43950000 bits
 frame120: 1578522 bits 12450000 bits 11700000 bits 48600000 bits

CUMULATIVE BIT COUNT (CBC) AFTER 10 FRAMES OF MOB 4 Kbit/s

frame 10: 1451239 bits 76412 bits 80597 bits 137477 bits 1610455 bits
 frame 20: 2901487 bits 157336 bits 162842 bits 267716 bits 3211487 bits
 frame 30: 4351649 bits 237318 bits 243834 bits 400732 bits 4837885 bits
 frame 40: 5801811 bits 316371 bits 325516 bits 530464 bits 6447931 bits
 frame 50: 7251973 bits 395418 bits 401107 bits 618764 bits 7564094 bits
 frame 60: 8698950 bits 473337 bits 488893 bits 726474 bits 8779428 bits
 frame 70: 10141108 bits 561342 bits 571304 bits 803870 bits 9789907 bits
 frame 80: 11590258 bits 645991 bits 654533 bits 864875 bits 10649077 bits
 frame 90: 13040318 bits 731400 bits 736485 bits 950478 bits 12004203 bits
 frame100: 14489900 bits 810246 bits 818233 bits 103594 bits 14111459 bits
 frame110: 15977487 bits 892863 bits 901804 bits 1168740 bits 15772114 bits
 frame120: 17461187 bits 971479 bits 984556 bits 1298550 bits 17921122 bits

ANNEX 5 Code Tables for VLC

Table 1

-128	11111110101010
-127	11111110101001
-126	11111110101000
-125	11111110101011
-124	11111110101010
-123	11111110101011
-122	11111110101000
-121	11111110101001
-120	11111110101011
-119	11111110101000
-118	11111110101001
-117	11111110101011
-116	11111110101000
-115	11111110101001
-114	11111110101011
-113	11111110101000
-112	11111110101001
-111	11111110101011
-110	11111110101000
-109	11111110101001
-108	11111110101011
-107	11111110101000
-106	11111110101001
-105	11111110101011
-104	11111110101000
-103	11111110101001
-102	11111110101011
-101	11111110101000
-100	11111110101001
-99	11111110101011
-98	11111110101000
-97	11111110101001
-96	11111110101011
-95	11111110101000
-94	11111110101001
-93	11111110101011
-92	11111110101000
-91	11111110101001
-90	11111110101011
-89	11111110101000
-88	11111110101001
-87	11111110101011
-86	11111110101000
-85	11111110101001
-84	11111110101011
-83	11111110101000
-82	11111110101001
-81	11111110101011
-80	11111110101000
-79	11111110101001
-78	11111110101011
-77	11111110101000
-76	11111110101001
-75	11111110101011
-74	11111110101000
-73	11111110101001
-72	11111110101011
-71	11111110101000
-70	11111110101001
-69	11111110101011
-68	11111110101000
-67	11111110101001
-66	11111110101011
-65	11111110101000
-64	11111110101001
-63	11111110101011
-62	11111110101000
-61	11111110101001
-60	11111110101011
-59	11111110101000
-58	11111110101001

101	11111110110000
102	11111110110001
103	11111110110010
104	11111110110011
105	11111110110100
106	11111110110101
107	11111110110110
108	11111110110111
109	11111110110000
110	11111110110001
111	11111110110010
112	11111110110011
113	11111110110100
114	11111110110101
115	11111110110110
116	11111110110111
117	11111110110000
118	11111110110001
119	11111110110010
120	11111110110011
121	11111110110100
122	11111110110101
123	11111110110110
124	11111110110111
125	11111110110000
126	11111110110001
127	11111110110010

Table 1

0	010
1	011
2	000
3	001
4	100
5	101
6	1000
7	1001
8	11010
9	11011
10	11000
11	11001
12	111010
13	111011
14	111000
15	111001
16	111010
17	111011
18	111000
19	111001
20	1111010
21	1111011
22	1111000
23	1111001
24	11111010
25	11111011
26	11111000
27	11111001
28	111111010
29	111111011
30	111111000
31	111111001
32	1111111000
33	1111111001
34	111111101000
35	111111101001
36	1111111011010
37	1111111011011
38	1111111011000
39	1111111011001
40	1111111011010
41	1111111011011
42	1111111011000
43	1111111011001
44	1111111011010
45	1111111011011
46	1111111011000
47	1111111011001
48	1111111011010

[illegible]

Code Tables for VLC

91	38	1111111100010010	117	1111111111000011
92	39	1111111100010011	118	1111111111000010
93	40	1111111100010011	119	1111111111000111
94	41	1111111100010011	120	1111111111000110
95	42	1111111100010011	121	1111111111000111
96	43	1111111100010010	122	1111111111000110
97	44	1111111100010000	123	1111111111000111
98	45	1111111100010001	124	1111111111000110
99	46	1111111100010010	125	1111111111000000
100	47	1111111100010010	126	1111111111000001
101	48	1111111100010011	127	1111111111000111
102	49	1111111100010011	128	1111111111000110
103	50	1111111100010011	129	1111111111000011
104	51	1111111100010011	130	1111111111000111
105	52	1111111100010011	131	1111111111000110
106	53	1111111100010011	132	1111111111000100
107	54	1111111100000001	133	1111111100010010
108	55	1111111100010010	134	1111111100010000
109	56	1111111100010011	135	1111111100010000
110	57	1111111100010011	136	1111111100010011
111	58	1111111100010011	137	1111111100010011
112	59	1111111100000011	138	1111111100010010
113	60	1111111100000010	139	1111111100010011
114	61	1111111100010010	140	1111111100010011
115	62	1111111100010000	141	1111111100010011
116	63	1111111100010001	142	1111111100010010
117	64	1111111100010010	143	1111111100010000
118	65	1111111100010011	144	1111111100010010
119	66	1111111100010011	145	1111111100010010
120	67	1111111100010011	146	1111111100010010
121	68	1111111100010011	147	1111111100010011
122	69	1111111100010011	148	1111111100010010
123	70	1111111100000010	149	1111111100010011
124	71	1111111100010001	150	1111111100010010
125	72	1111111100010011	151	1111111100010011
126	73	1111111100010010	152	1111111100010000
127	74	1111111100010010	153	1111111100010011
Table 3				
0	0	001	154	1111111100010001
1	1	000	155	1111111100010001
2	2	1001	156	1111111100010010
3	3	1010	157	1111111100010010
4	4	1000	158	1111111100010000
5	5	0110	159	1111111100010001
6	6	0111	160	1111111100010010
7	7	11001	161	1111111100010010
8	8	11010	162	1111111100010010
9	9	11000	163	1111111100010011
10	10	10110	164	1111111100010011
11	11	10111	165	1111111100010011
12	12	110001	166	1111111100000000
13	13	111010	167	1111111100000001
14	14	111000	168	1111111100010010
15	15	110110	169	1111111100010011
16	16	110111	170	1111111100010010
17	17	1111001	171	1111111100010011
18	18	1111010	172	1111111100000010
19	19	1111010	173	1111111100000011
20	20	111010	174	1111111100000000
21	21	111011	175	1111111100000001
22	22	11111001	176	1111111100000011
23	23	11111010	177	1111111100000011
24	24	11111010	178	1111111100000010
25	25	1111010	179	1111111100000010
26	26	1111001	180	1111111100000011
27	27	1111001	181	1111111100000011
28	28	11111010	182	1111111100000000
29	29	11111010	183	1111111100010010
30	30	11111000	184	1111111100010010
31	31	1111010	185	1111111100010011
32	32	11110111	186	1111111100010011
33	33	1111100000	187	1111111100010011
34	34	111110110	188	1111111100010011
35	35	111110100	189	1111111100010000
36	36	111110101	190	1111111100010010
37	37	111110010	191	1111111100010011
			192	1111111100010010
			193	1111111100010010
			194	1111111100010010
			195	1111111111000011

Table 3

0	001	78	11111111010001	157	11111111001110
1	000	79	11111111010001	158	11111111000000
2	1001	80	11111111010101	159	11111111010001
3	1010	81	11111111010100	160	11111111010110
4	1000	82	11111111010000	161	11111111010111
5	0111	83	11111111010110	162	11111111010010
6	0110	84	11111111010111	163	11111111010011
7	11001	85	11111111010100	164	11111111010010
8	11010	86	11111111010101	165	11111111010111
9	11000	87	11111111010100	166	11111111000000
10	10110	88	11111111010111	167	11111111010110
11	10101	89	11111111010110	168	11111111010111
12	110001	90	11111111010101	169	11111111010110
13	110101	91	11111111010100	170	11111111010110
14	110100	92	11111111010100	171	11111111010110
15	110110	93	11111111010101	172	1111111100000010
16	110111	94	11111111010100	173	1111111100000011
17	1111001	95	11111111010100	174	1111111100000100
18	1111000	96	11111111010101	175	1111111100000101
19	11110010	97	11111111010100	176	1111111100000110
20	11101011	98	11111111010101	177	1111111100000111
21	1110111	99	11111111010101	178	1111111100000100
22	11111001	100	11111111010100	179	1111111100000101
23	11111010	101	11111111010111	180	1111111101010010
24	11110000	102	11111111000010	181	1111111101010001
25	11110010	103	11111111000011	182	1111111101000000
26	11110011	104	11111111000000	183	11111111010111
27	11111001	105	11111111000001	184	11111111010100
28	11111010	106	11111111010101	185	11111111010101
29	11111000	107	11111111010100	186	11111111010101
30	11110110	108	11111111010110	187	11111111010110
31	11110111	109	11111111010111	188	11111111010100
32	11111011	110	11111111010110	189	11111111010100
33	11111000	111	11111111010111	190	11111111010101
34	11111010	112	11111111010110	191	11111111010111
35	11111000	113	11111111010111	192	11111111010100
36	11111001	114	11111111010110	193	11111111010101
37	11111010	115	11111111010111	194	11111111010110
38	11111011	116	11111111000000	195	11111111010111

Table 4

-128 : 1111111010011110
 -127 : 1111111010011011
 -126 : 1111111010010000
 -125 : 1111111010010000
 -124 : 1111111010010111
 -123 : 1111111010010111
 -122 : 1111111010010111
 -121 : 1111111010010100
 -120 : 1111111010010100
 -119 : 1111111010010100
 -118 : 1111111010010101
 -117 : 1111111010010101
 -116 : 1111111010010101
 -115 : 1111111010010100
 -114 : 1111111010010100
 -113 : 1111111010010100
 -112 : 1111111010010100
 -111 : 1111111010010100
 -110 : 1111111010010100
 -109 : 1111111010010101
 -108 : 1111111010010110
 -107 : 1111111010010101
 -106 : 1111111010010101
 -105 : 1111111010010111
 -104 : 1111111010010101
 -103 : 1111111010010101
 -102 : 1111111010010111
 -101 : 1111111010010101
 -100 : 1111111010010101
 -99 : 1111111010010111
 -98 : 1111111010010111

-57	111111110001	61	111111110010	9	11000	86	111111110000	157	111111101111	-127	111111101100	-48	111111101011
-56	111111110001	62	111111110011	10	11001	87	111111110001	158	111111100000	-126	111111100111	-47	111111100011
-55	111111110001	63	111111110010	11	11010	88	111111110000	159	111111100011	-125	111111100110	-46	111111100011
-54	111111110001	64	111111110011	12	11011	89	111111110001	160	111111100010	-124	111111100110	-45	111111100011
-53	111111110001	65	111111110000	13	11000	90	111111110000	161	111111100011	-123	111111100110	-44	111111100011
-52	111111110001	66	111111110001	14	11001	91	111111110001	162	111111100010	-122	111111100111	-43	111111100011
-51	111111110001	67	111111110000	15	11010	92	111111110000	163	111111100011	-121	111111100110	-42	111111100011
-50	111111110001	68	111111110001	16	11011	93	111111110001	164	111111100010	-120	111111100111	-41	111111100011
-49	111111110001	69	111111110000	17	11000	94	111111110000	165	111111100011	-119	111111100110	-40	111111100011
-48	111111110001	70	111111110001	18	11001	95	111111110001	166	111111100010	-118	111111100111	-39	111111100011
-47	111111110001	71	111111110000	19	11010	96	111111110000	167	111111100011	-117	111111100110	-38	111111100011
-46	111111110001	72	111111110001	20	11011	97	111111110001	168	111111100010	-116	111111100111	-37	111111100011
-45	111111110001	73	111111110000	21	11000	98	111111110000	169	111111100011	-115	111111100110	-36	111111100011
-44	111111110001	74	111111110001	22	11001	99	111111110001	170	111111100010	-114	111111100111	-35	111111100011
-43	111111110001	75	111111110000	23	11010	100	111111110000	171	111111100011	-113	111111100110	-34	111111100011
-42	111111110001	76	111111110001	24	11011	101	111111110001	172	111111100010	-112	111111100111	-33	111111100011
-41	111111110001	77	111111110000	25	11000	102	111111110000	173	111111100011	-111	111111100110	-32	111111100011
-40	111111110001	78	111111110001	26	11001	103	111111110001	174	111111100010	-110	111111100111	-31	111111100011
-39	111111110001	79	111111110000	27	11010	104	111111110000	175	111111100011	-109	111111100110	-30	111111100011
-38	111111110001	80	111111110001	28	11011	105	111111110001	176	111111100010	-108	111111100111	-29	111111100011
-37	111111110001	81	111111110000	29	11000	106	111111110000	177	111111100011	-107	111111100110	-28	111111100011
-36	111111110001	82	111111110001	30	11001	107	111111110001	178	111111100010	-106	111111100111	-27	111111100011
-35	111111110001	83	111111110000	31	11010	108	111111110000	179	111111100011	-105	111111100110	-26	111111100011
-34	111111110001	84	111111110001	32	11011	109	111111110001	180	111111100010	-104	111111100111	-25	111111100011
-33	111111110001	85	111111110000	33	11000	110	111111110000	181	111111100011	-103	111111100110	-24	111111100011
-32	111111110001	86	111111110001	34	11001	111	111111110001	182	111111100010	-102	111111100111	-23	111111100011
-31	111111110001	87	111111110000	35	11010	112	111111110000	183	111111100011	-101	111111100110	-22	111111100011
-30	111111110001	88	111111110001	36	11011	113	111111110001	184	111111100010	-100	111111100111	-21	111111100011
-29	111111110001	89	111111110000	37	11000	114	111111110000	185	111111100011	-99	111111100110	-20	111111100011
-28	111111110001	90	111111110001	38	11001	115	111111110001	186	111111100010	-98	111111100111	-19	111111100011
-27	111111110001	91	111111110000	39	11010	116	111111110000	187	111111100011	-97	111111100110	-18	111111100011
-26	111111110001	92	111111110001	40	11011	117	111111110001	188	111111100010	-96	111111100111	-17	111111100011
-25	111111110001	93	111111110000	41	11000	118	111111110000	189	111111100011	-95	111111100110	-16	111111100011
-24	111111110001	94	111111110001	42	11001	119	111111110001	190	111111100010	-94	111111100111	-15	111111100011
-23	111111110001	95	111111110000	43	11010	120	111111110000	191	111111100011	-93	111111100110	-14	111111100011
-22	111111110001	96	111111110001	44	11011	121	111111110001	192	111111100010	-92	111111100111	-13	111111100011
-21	111111110001	97	111111110000	45	11000	122	111111110000	193	111111100011	-91	111111100110	-12	111111100011
-20	111111110001	98	111111110001	46	11001	123	111111110001	194	111111100010	-90	111111100111	-11	111111100011
-19	111111110001	99	111111110000	47	11010	124	111111110000	195	111111100011	-89	111111100110	-10	111111100011
-18	111111110001	100	111111110001	48	11011	125	111111110001	196	111111100010	-88	111111100111	-9	111111100011
-17	111111110001	101	111111110000	49	11000	126	111111110000	197	111111100011	-87	111111100110	-8	111111100011
-16	111111110001	102	111111110001	50	11001	127	111111110001	198	111111100010	-86	111111100111	-7	111111100011
-15	111111110001	103	111111110000	51	11010	128	111111110000	199	111111100011	-85	111111100110	-6	111111100011
-14	111111110001	104	111111110001	52	11011	129	111111110001	200	111111100010	-84	111111100111	-5	111111100011
-13	111111110001	105	111111110000	53	11000	130	111111110000	201	111111100011	-83	111111100110	-4	111111100011
-12	111111110001	106	111111110001	54	11001	131	111111110001	202	111111100010	-82	111111100111	-3	111111100011
-11	111111110001	107	111111110000	55	11010	132	111111110000	203	111111100011	-81	111111100110	-2	111111100011
-10	111111110001	108	111111110001	56	11011	133	111111110001	204	111111100010	-80	111111100111	-1	111111100011
-9	111111110001	109	111111110000	57	11000	134	111111110000	205	111111100011	-79	111111100110	0	111111100011
-8	111111110001	110	111111110001	58	11001	135	111111110001	206	111111100010	-78	111111100111	1	111111100011
-7	111111110001	111	111111110000	59	11010	136	111111110000	207	111111100011	-77	111111100110	2	111111100011
-6	111111110001	112	111111110001	60	11011	137	111111110001	208	111111100010	-76	111111100111	3	111111100011
-5	111111110001	113	111111110000	61	11000	138	111111110000	209	111111100011	-75	111111100110	4	111111100011
-4	111111110001	114	111111110001	62	11001	139	111111110001	210	111111100010	-74	111111100111	5	111111100011
-3	111111110001	115	111111110000	63	11010	140	111111110000	211	111111100011	-73	111111100110	6	111111100011
-2	111111110001	116	111111110001	64	11011	141	111111110001	212	111111100010	-72	111111100111	7	111111100011
-1	111111110001	117	111111110000	65	11000	142	111111110000	213	111111100011	-71	111111100110	8	111111100011
0	111111110001	118	111111110001	66	11001	143	111111110001	214	111111100010	-70	111111100111	9	111111100011
1	111111110001	119	111111110000	67	11010	144	111111110000	215	111111100011	-69	111111100110	10	111111100011
2	111111110001	120	111111110001	68	11011	145	111111110001	216	111111100010	-68	111111100111	11	111111100011
3	111111110001	121	111111110000	69	11000	146	111111110000	217	111111100011	-67	111111100110	12	111111100011
4	111111110001	122	111111110001	70	11001	147	111111110001	218	111111100010	-66	111111100111	13	111111100011
5	111111110001	123	111111110000	71	11010	148	111111110000	219	111111100011	-65	111111100110	14	111111100011
6	111111110001	124	111111110001	72	11011	149	111111110001	220	111111100010	-64	111111100111	15	111111100011
7	111111110001	125	111111110000	73	11000	150	111111110000	221	111111100011	-63	111111100110	16	111111100011
8	111111110001	126	111111110001	74	11001	151	111111110001	222	111111100010	-62	111111100111	17	111111100011
9	111111110001	127	111111110000	75	11010	152	111111110000	223	111111100011	-61	111111100110	18	111111100011
10	111111110001	128	111111110001	76	11011	153	111111110001	224	111111100010	-60	111111100111	19	111111100011
11	111111110001	129	111111110000	77	11000	154	111111110000	225	111111100011	-59	111111100110	20	111111100011
12	111111110001	130	111111110001	78	11001	155	111111110001	226	111111100010	-58	111111100111	21	111111100011
13	111111110001	131	111111110000	79	11010	156	111111110000	227	111111100011	-57	111111100110	22	111111100011
14	111111110001	132	111111110001	80	11011	157	111111110001	228	111111100010	-56	111111100111	23	111111100011
15	111111110001	133	111111110000	81	11000	158	111111110000	229	111111100011	-55	111111100110	24	111111100011
16	1111111100												

94 : 1111111100001
95 : 1111111100001
96 : 1111111100001
97 : 1111111100001
98 : 1111111100001
99 : 1111111100001

Table 8

15 : 1111111100001
16 : 1111111100001
17 : 1111111100001
18 : 1111111100001
19 : 1111111100001
20 : 1111111100001
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89 : 1111111100001
90 : 1111111100001
91 : 1111111100001
92 : 1111111100001
93 : 1111111100001
94 : 1111111100001
95 : 1111111100001
96 : 1111111100001
97 : 1111111100001
98 : 1111111100001
99 : 1111111100001

0 : 1010

1 : 1011

2 : 1000

3 : 1001

4 : 11010

5 : 11011

6 : 11000

7 : 11001

8 : 11010

9 : 11011

10 : 11000

11 : 11001

12 : 111010

13 : 111011

14 : 111000

15 : 111001

16 : 1111010

17 : 1111011

18 : 1111000

19 : 1111001

20 : 11111010

21 : 11111011

22 : 11111000

23 : 11111001

24 : 111111010

25 : 111111011

26 : 111111000

27 : 111111001

28 : 1111111010

29 : 1111111011

30 : 1111111000

31 : 1111111001

32 : 11111111010

33 : 11111111011

34 : 11111111000

35 : 11111111001

36 : 111111111010

37 : 111111111011

38 : 111111111000

39 : 111111111001

40 : 111111111010

41 : 111111111011

42 : 111111111000

43 : 111111111001

44 : 1111111111010

45 : 1111111111011

46 : 1111111111000

47 : 1111111111001

48 : 11111111111010

49 : 11111111111011

50 : 11111111111000

51 : 11111111111001

52 : 111111111111010

53 : 111111111111011

54 : 111111111111000

55 : 111111111111001

56 : 1111111111111010

57 : 1111111111111011

58 : 1111111111111000

59 : 1111111111111001

60 : 11111111111111010

61 : 11111111111111011

62 : 11111111111111000

63 : 0

49 : 1111111100001
50 : 1111111100001
51 : 1111111100001
52 : 1111111100001
53 : 1111111100001
54 : 1111111100001
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66 : 1111111100001
67 : 1111111100001
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98 : 1111111100001
99 : 1111111100001

Table 7

171 : 1111111100001
172 : 1111111100001
173 : 1111111100001
174 : 1111111100001
175 : 010

-100 : 1111111100000

-99 : 1111111100001

-98 : 1111111100001

-97 : 1111111100001

-96 : 1111111100001

-95 : 1111111100001

-94 : 1111111100001

-93 : 1111111100001

-92 : 1111111100001

-91 : 1111111100001

-90 : 1111111100001

-89 : 1111111100001

-88 : 1111111100001

-87 : 1111111100001

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-36 : 1111111100001

-35 : 1111111100001

-34 : 1111111100001

-33 : 1111111100001

-32 : 1111111100001

-31 : 1111111100001

Table 7

0 : 1010
1 : 1011
2 : 1000
3 : 1001
4 : 11010
5 : 11011
6 : 11000
7 : 11001
8 : 11010
9 : 11011
10 : 11000
11 : 11001
12 : 111010
13 : 111011
14 : 111000
15 : 111001
16 : 111010
17 : 111011
18 : 111000
19 : 111001
20 : 1111010
21 : 1111011
22 : 1111000
23 : 1111001
24 : 11111010
25 : 11111011
26 : 11111000
27 : 11111001
28 : 111111010
29 : 111111011
30 : 111111000
31 : 111111001
32 : 1111111010
33 : 1111111011
34 : 1111111000
35 : 1111111001
36 : 11111111010
37 : 11111111011
38 : 11111111000
39 : 11111111001
40 : 111111111010
41 : 111111111011
42 : 111111111000
43 : 111111111001
44 : 1111111111010
45 : 1111111111011
46 : 1111111111000
47 : 1111111111001
48 : 11111111111010
49 : 11111111111011
50 : 11111111111000
51 : 11111111111001
52 : 111111111111010
53 : 111111111111011
54 : 111111111111000
55 : 111111111111001
56 : 1111111111111010
57 : 1111111111111011
58 : 1111111111111000
59 : 1111111111111001
60 : 11111111111111010
61 : 11111111111111011
62 : 11111111111111000
63 : 11111111111111001
64 : 111111111111111010
65 : 111111111111111011
66 : 111111111111111000
67 : 111111111111111001
68 : 1111111111111111010
69 : 1111111111111111011
70 : 1111111111111111000
71 : 1111111111111111001
72 : 11111111111111111010
73 : 11111111111111111011
74 : 11111111111111111000
75 : 11111111111111111001
76 : 111111111111111111010
77 : 111111111111111111011
78 : 111111111111111111000
79 : 111111111111111111001
80 : 1111111111111111111010
81 : 1111111111111111111011
82 : 1111111111111111111000
83 : 1111111111111111111001
84 : 11111111111111111111010
85 : 11111111111111111111011
86 : 11111111111111111111000
87 : 11111111111111111111001
88 : 111111111111111111111010
89 : 111111111111111111111011
90 : 111111111111111111111000
91 : 111111111111111111111001
92 : 1111111111111111111111010
93 : 1111111111111111111111011
94 : 1111111111111111111111000
95 : 1111111111111111111111001
96 : 11111111111111111111111010
97 : 11111111111111111111111011
98 : 11111111111111111111111000
99 : 11111111111111111111111001

Bitstream files

-rw----- 1 schamel 2487296 Oct 13 14:29 bitstream.flow_4mb
-rw----- 1 schamel 5611176 Oct 11 19:17 bitstream.flow_9mb
-rw----- 1 schamel 2481664 Oct 14 23:54 bitstream.mob_4mb
-rw----- 1 schamel 5608104 Oct 13 03:21 bitstream.mob_9mb
-rw----- 1 schamel 2499584 Oct 12 09:43 bitstream.ten_4mb
-rw----- 1 schamel 5610152 Oct 14 10:33 bitstream.ten_9mb
-rw----- 1 schamel 5601448 Oct 14 01:04 bitstream.pop_9mb