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TITLE: Buffering and Delays for a Sliding Window Channel Constraint
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Buffering and delays for a sliding window channel constraint

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1 Introduction

We present buffer and delay considerations for a video system when the transmitted bit-rate must satisfy a sliding window constraint as well as a peak rate constraint. The channel constraint (or UPC) is described both by a peak transmitted rate per frame period, R_{max} bits per frame period, and a sliding window. The sliding window constrains the total number of bits transmitted in a duration of S_{win} frames to be less than or equal to $\bar{R}S_{win}$.

Our objectives are two-fold:

- To give sizing of encoder and decoder buffers such that any encoded bit stream that conforms to the UPC can be transmitted without further buffer constraints.
- To demonstrate reduced cost over the solution proposed by AVC-90 [2].

The system we consider is as in AVC-56 [1], and shown in Figure 1. At the encoder and decoder, encoded bits are buffered. The number of encoded bits per frame is E_i, and the number of transmitted bits per frame period, which is selected by the rate control device, is R_i. The rate control device ensures that the coded bit-stream can be transmitted without violating the UPC. (Note that in general, R_i could be chosen to be less than the peak rate R_{max}, even if the encoder buffer is not empty.) The decoder contains one frame memory to store the frame currently being decoded, which is the next frame to be displayed.

2 Parameter selection

First, we select the delay and the encoder and decoder buffer sizes to ensure the decoder buffer will not impose additional rate constraints. We assume here, as in AVC-90, that bits are transmitted from the encoder buffer at the peak rate, provided the buffer is not empty.

As in AVC-90, we assume the peak number of encoded bits allowed in any one frame is determined by the channel constraints, $E_{max} = \bar{R}S_{win}$. Then, to allow both the encoder and decoder buffers to store E_{max}, we choose $B^e_{max} = \bar{R}S_{win}$ and $B^d_{max} = \bar{R}S_{win}$. The delay must be $L = E_{max}/R_{max}$ or $L = (\bar{R}/R_{max})S_{win}$, since we must be able to transmit E_{max} bits in L frame periods.

Using the buffer sizes and delay given above, the buffers will not impose further constraints on the maximum transmitted bit-rate. Each buffer is designed to contain all the bits in any period of length S_{win}, and hence can contain all the bits in any period of length L (since $L \leq S_{win}$ because $\bar{R} \leq R_{max}$). Only the channel constraints will constrain the maximum transmitted bit-rate; therefore, any bit-stream conforming to the channel constraints can be transmitted.

3 Comparison

Next, we compare the solution above and the solution proposed in AVC-90. The above encoder buffer size and delay are identical to those given in AVC-90. However, instead of requiring L frame memories at the decoder, we require only $\bar{R}S_{win}$ bits of buffer storage. This is a cheaper solution, since the maximum number of encoded bits per frame, $\bar{R}S_{win}$, cannot be larger than the number of un-encoded bits per frame that is necessary for one frame memory. Furthermore, this provides a solution for an H.261 decoder, which will be important for compatibility.

4 Conclusion

We have given the delay and the encoder and decoder buffer sizes that allow any encoded bit-stream conforming to a peak-plus-sliding window channel rate constraint (UPC) to be transmitted and decoded. This solution is less expensive to implement than the solution proposed by AVC-90.

Finally, we emphasize that the rate control device described in AVC-56 provides a solution for transmission within the rate constraints if the decoder buffer or the delay is not as large as that given here. This may be essential when a pre-existing decoder is used for VBR transmission, or if a delay shorter than $(\bar{R}/R_{max})S_{win}$ is desired.

References

[1] AVC-56, "Constraints on Variable Bit-Rate Video for ATM Networks", AT&T Bell Labs, Paris, 23–24 May 1991.

[2] AVC-90, "Considerations on delay with VBR coding", Japan, Santa Clara, 14–16 August 1991.

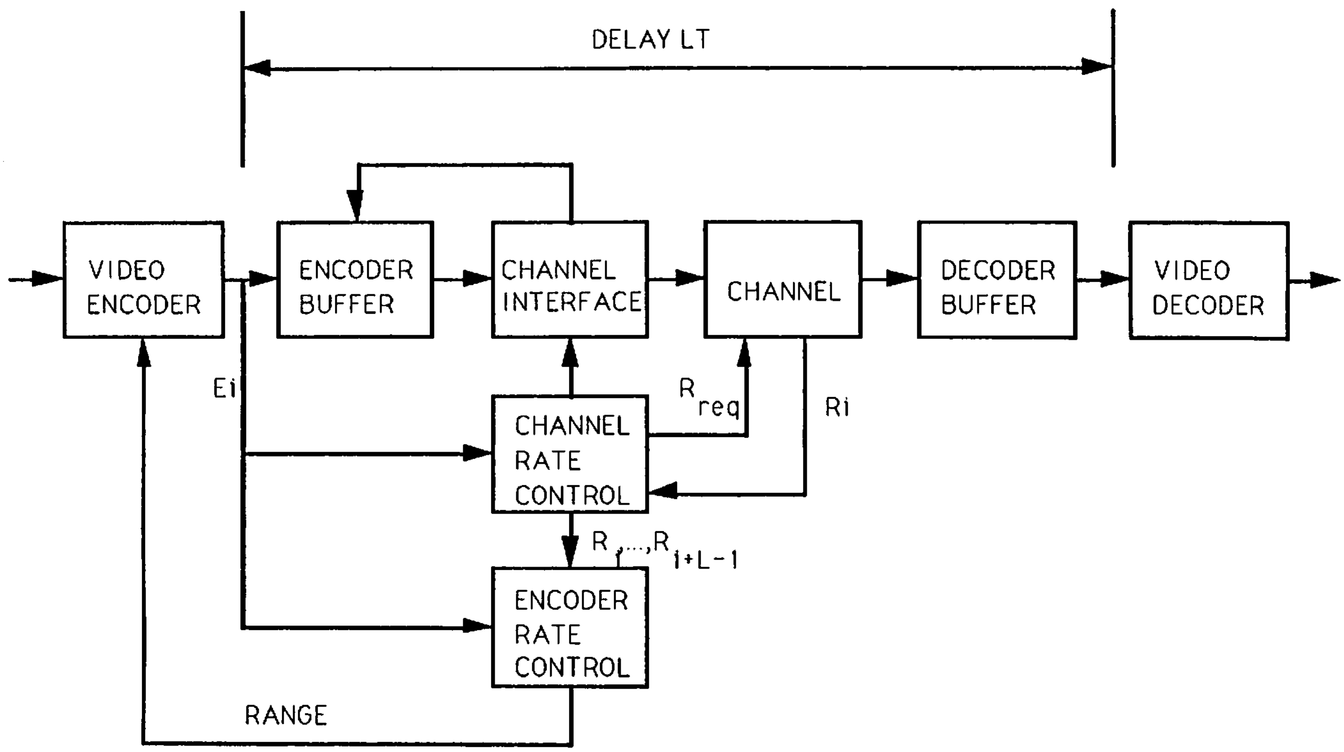

Figure 1: System