

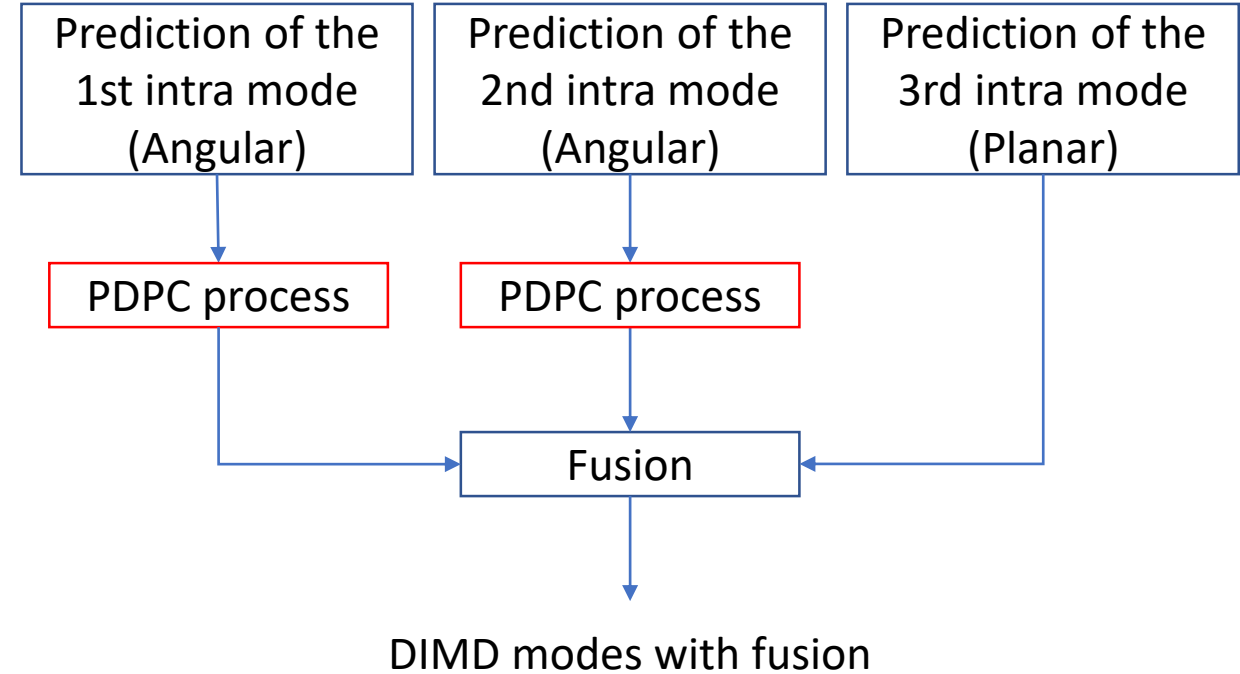
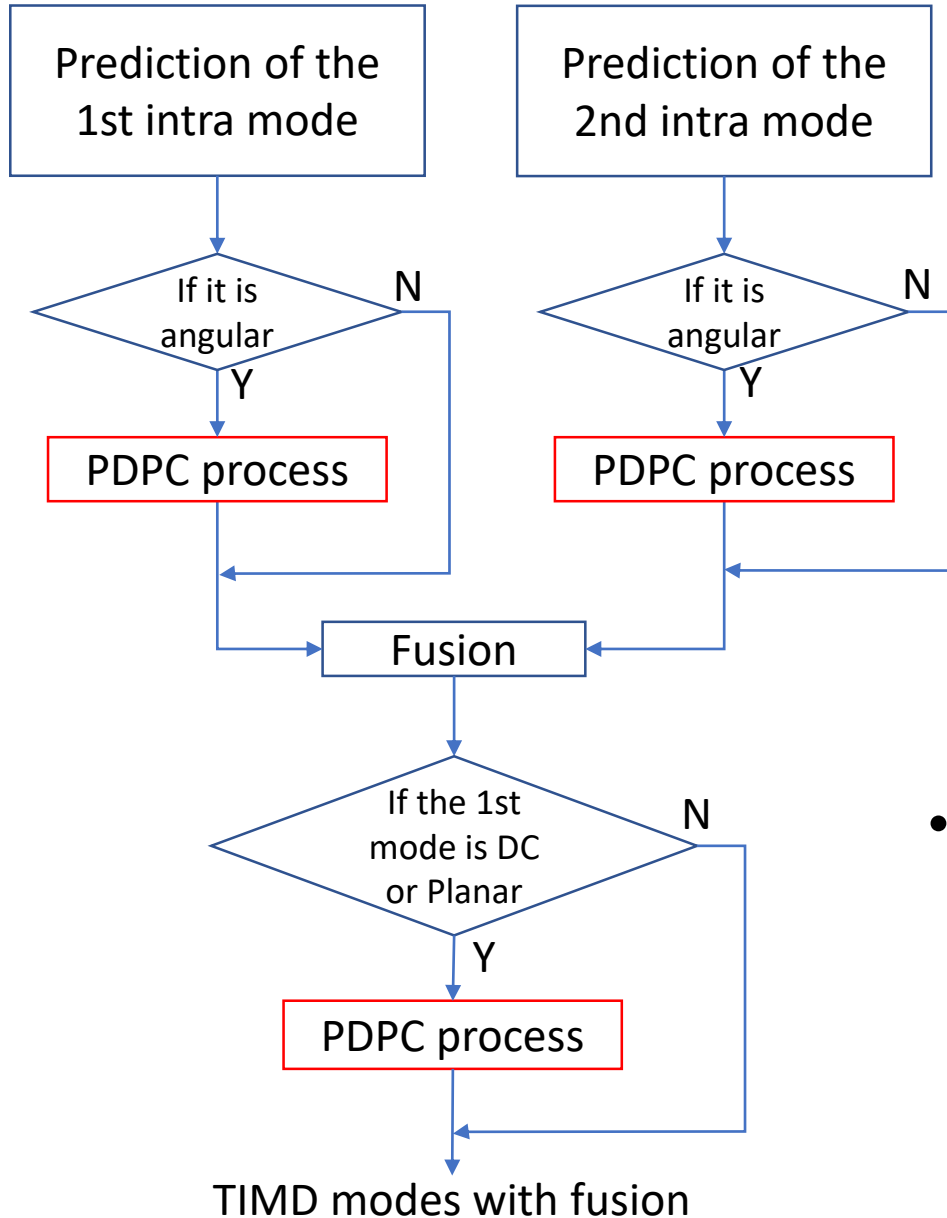
JVET-X0148

AHG12: On the PDPC handling in DIMD and TIMD

**Hong-Jheng Jhu, Xiaoyu Xiu, Yi-Wen Chen, Wei Chen, Che-Wei Kuo,
Ning Yan, Xianglin Wang**



PDPC for DIMD and TIMD in ECM-2.0



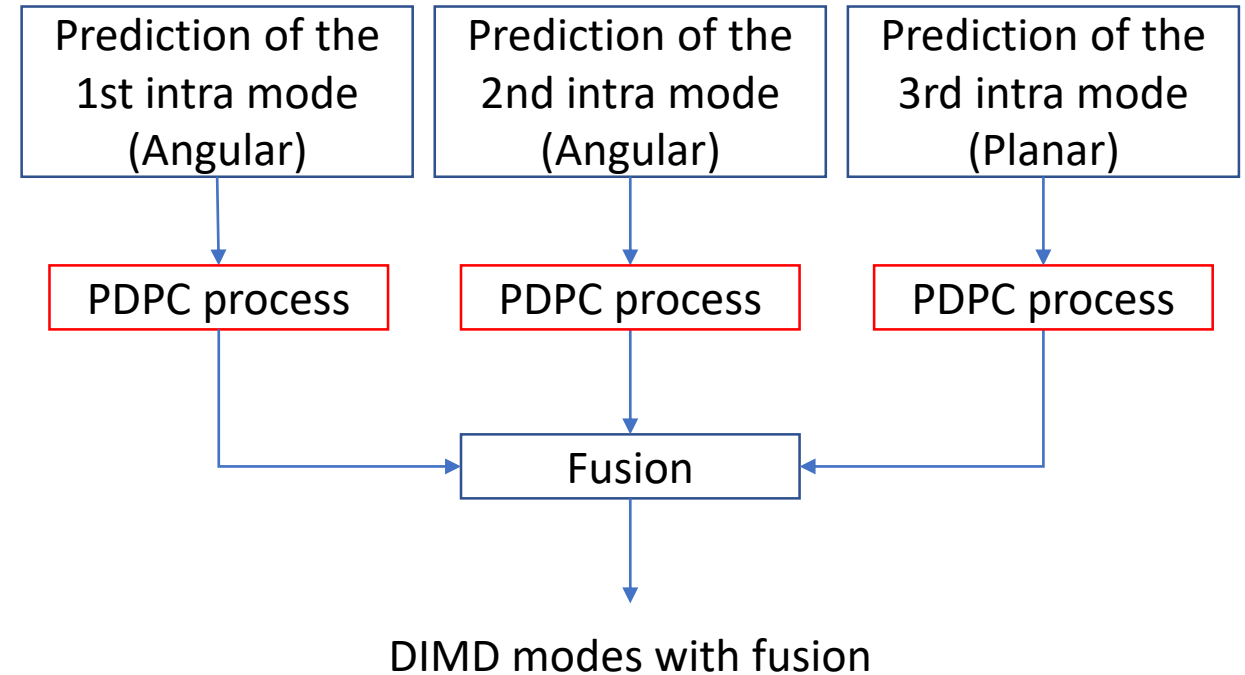
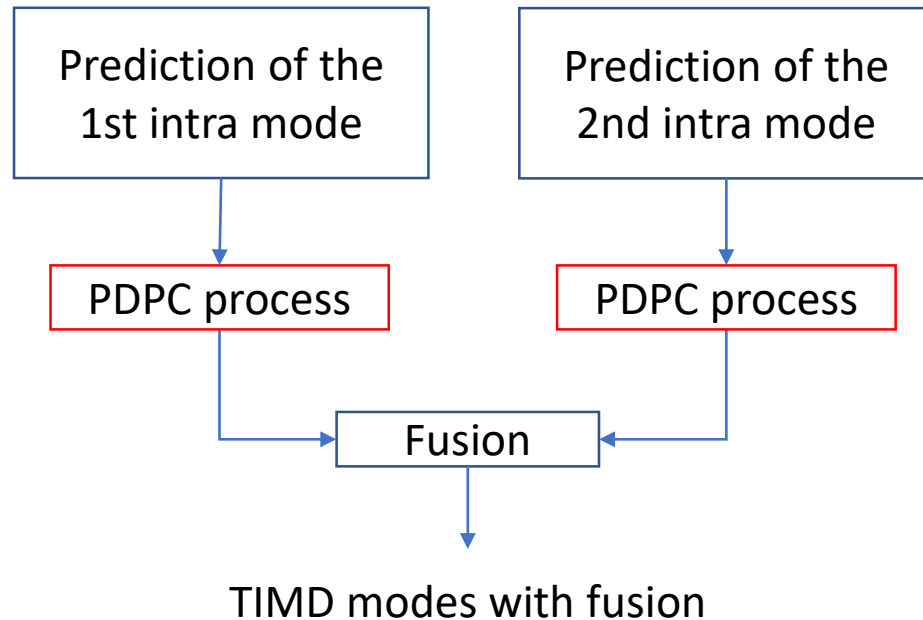
- Complexity issues

- Sequentially performing the PDPC on multiple locations within the TIMD could cause latency issue in the pipeline design
- Such non-unified design complicates software/hardware design logics



Proposed Modification

- Apply all PDPC processes before the fusion process of the DIMD and the TIMD



Simulation Results

- Anchor: ECM-2.0

	All Intra Main10				
	Over ECM-2.0				
	Y	U	V	EncT	DecT
Class A1	-0.02%	0.13%	-0.10%	100%	99%
Class A2	-0.03%	-0.10%	-0.04%	100%	99%
Class B	-0.02%	-0.02%	-0.12%	100%	100%
Class C	0.00%	0.05%	0.00%	100%	101%
Class E	-0.02%	-0.06%	0.09%	100%	100%
Overall	-0.02%	0.00%	-0.04%	100%	100%
Class D	0.01%	0.05%	-0.05%	101%	101%
Class F	-0.08%	-0.08%	-0.18%	101%	101%

	Random Access Main 10				
	Over ECM-2.0				
	Y	U	V	EncT	DecT
Class A1	0.00%	-0.01%	-0.09%	100%	101%
Class A2	0.01%	-0.11%	0.09%	100%	100%
Class B	-0.01%	0.01%	0.06%	101%	101%
Class C	-0.01%	-0.01%	-0.17%	101%	101%
Class E					
Overall	0.00%	-0.02%	-0.02%	101%	101%
Class D	0.00%	-0.42%	0.08%	101%	101%
Class F	0.01%	-0.11%	0.06%	101%	101%



Summary

- Recommend to adopt the proposed changes into ECM
- Thanks Qualcomm for cross-checking



Thank you

