

JVET-M0088

CE10-related: LIC restriction for pipeline structure

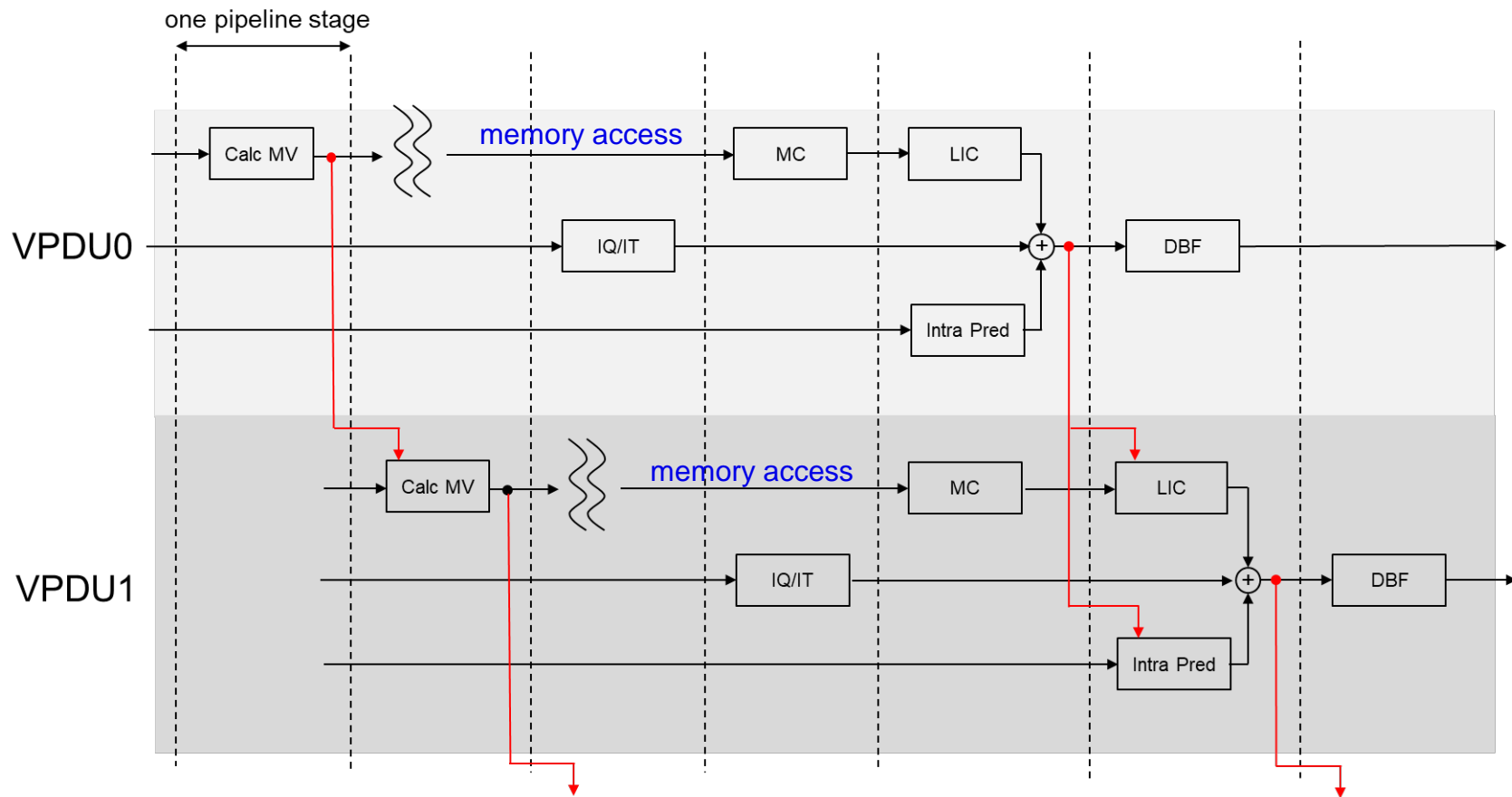
K. Abe, T. Toma

Panasonic Corporation

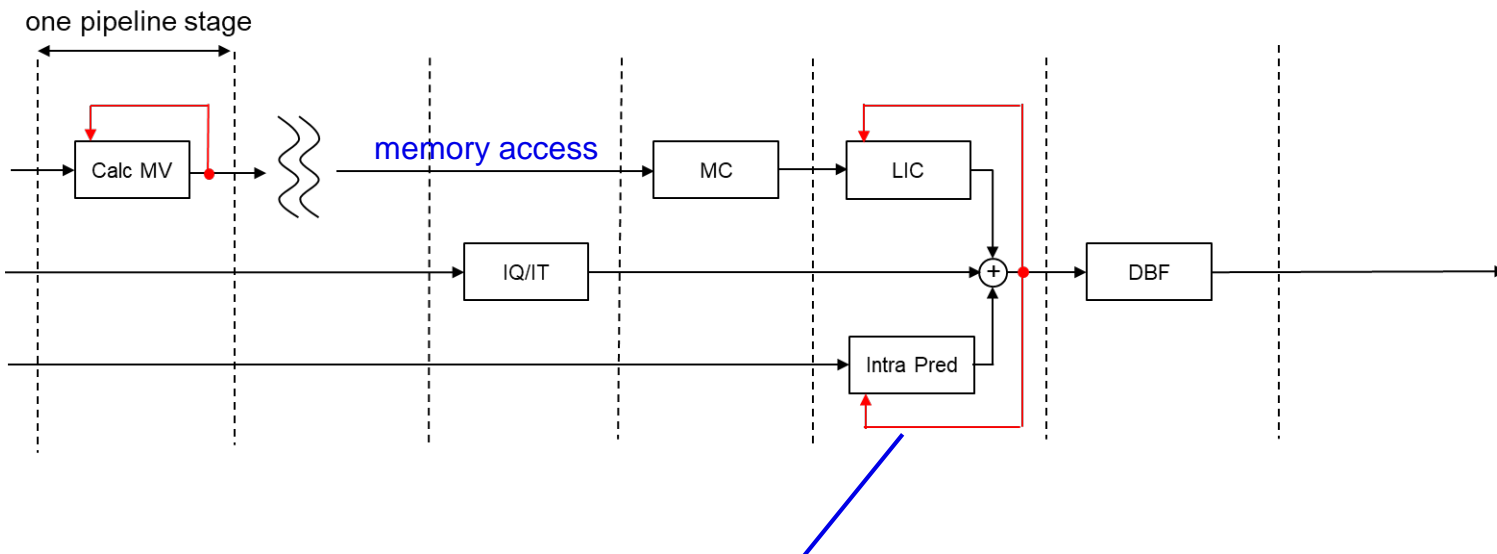
- CE10.5.2(JVET-M0087) proposes to introduce LIC, but it still has some pipeline issues in combination with following tools.
 - VPDU split process
 - ATMVP
 - MH-Intra

➡ We propose to introduce LIC restriction for these tools.

Introduction (Issue of feed-back loop)



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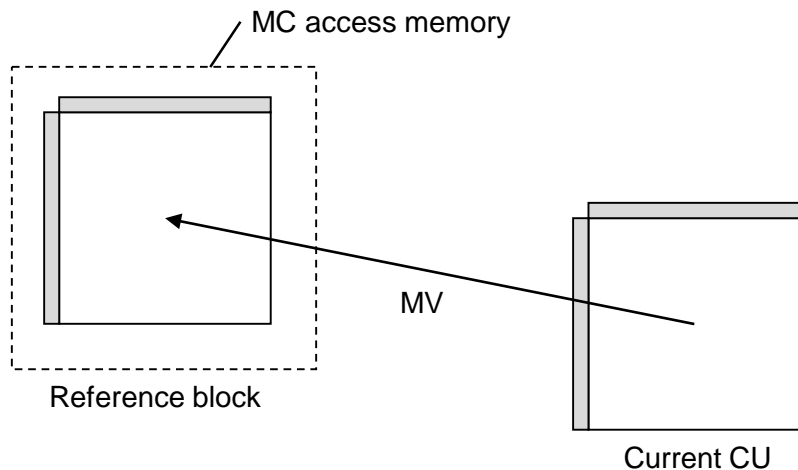


We call it “feed-back loop”.
All “feed-back loop” have to be closed in one stage

Proposed method (Item1 : VPDU restriction)

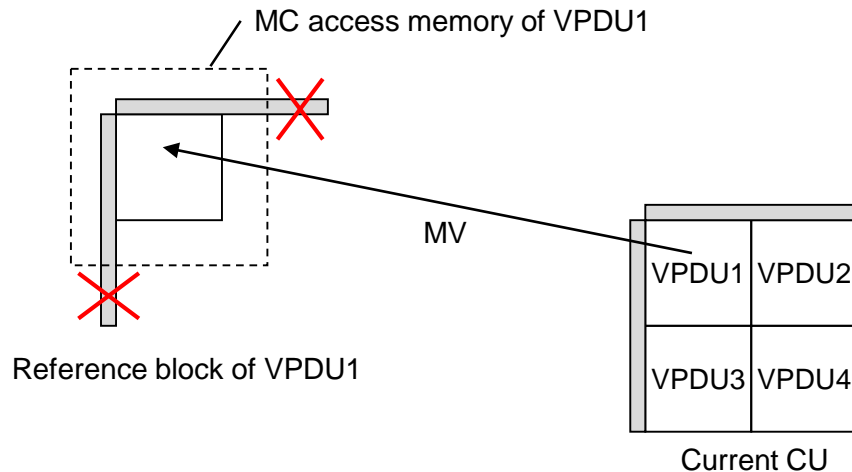
■ Problem when CU size is bigger than VPDU size

$CU \leq VPDU$ (OK)



The neighboring samples of reference block are **included** in MC access memory of current CU.

$CU > VPDU$ (NG)

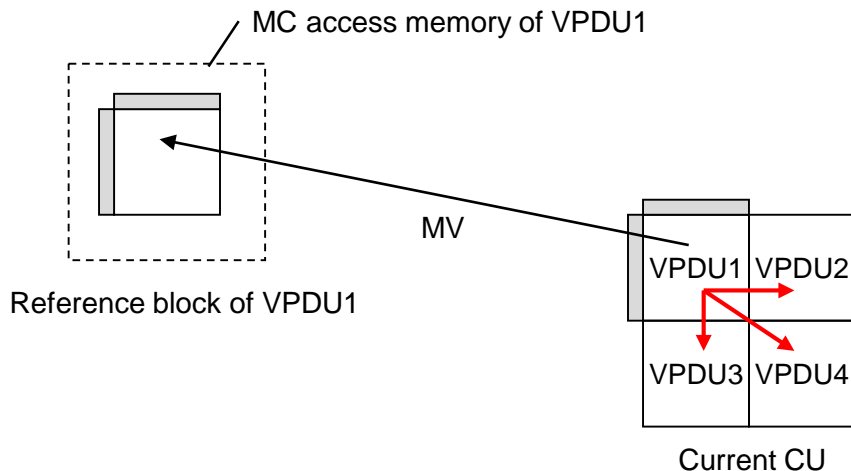


The neighboring samples of reference block are **not included** in MC access memory of VPDU1.

Proposed method (Item1 : VPDU restriction)

■ Solution

- Calculate LIC parameter only for the first VPDU in the CU.
- Share the LIC parameter with other VPDU in the CU.



Proposed method (Item2 : ATMVP restriction)

■ Problem

- LIC issue for ATMVP is similar to issue with VPDU.
(sub-block is used instead of VPDU)

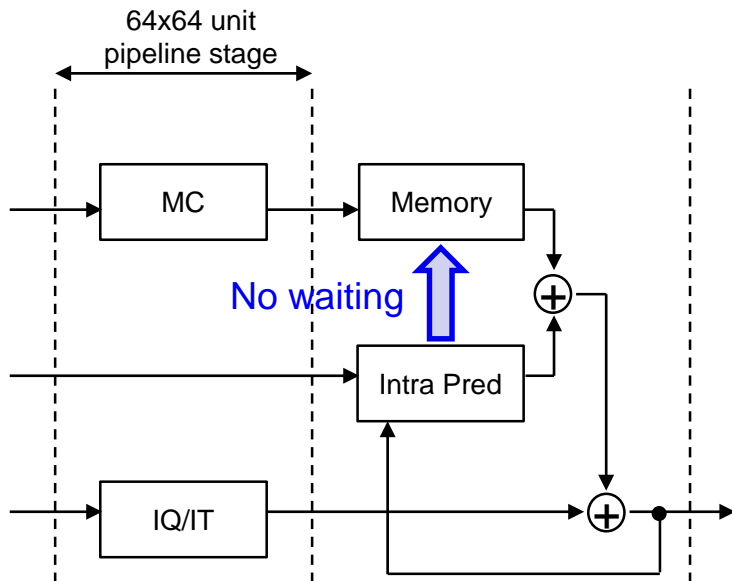
■ Solution

- Disable LIC when ATMVP is selected.
(Same algorithm as VPDU does not make sense since each sub-block has different MV)

Proposed method (Item3 : MH-Intra restriction)

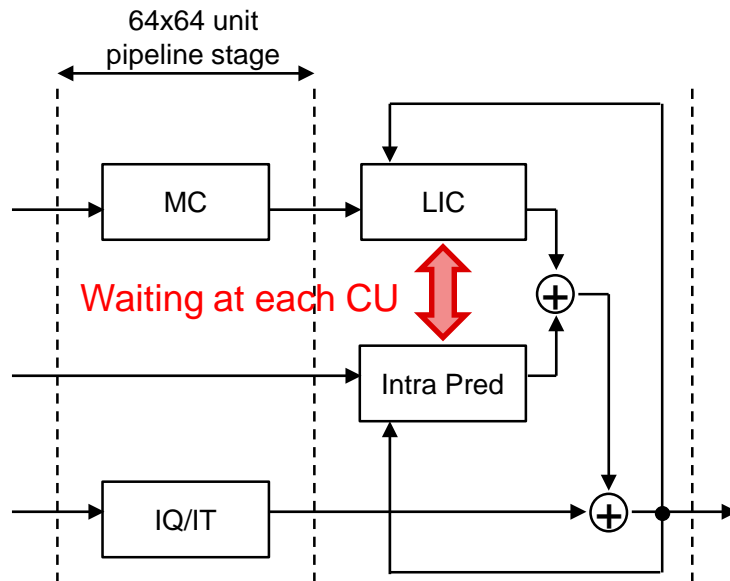
Problem

MH-Intra without LIC (OK)



“Intra Pred” process does not need to wait for inter process (no stage cycle increase).

MH-Intra with LIC (NG)



“LIC” and “Intra Pred” process have to wait for each other at each CU (increase stage cycle unacceptably).

Proposed method (Item3 : MH-Intra restriction)

Solution

- Disable MH-Intra when LIC is selected in small CU.

CU size for disabling MH-Intra with LIC	Worst case number of waiting in 64x64 unit
$\leq 128 \times 128$ (always disable)	1
$< 32 \times 32$	4
$\leq 16 \times 16$	8
$< 16 \times 16$	16
$\leq 8 \times 8$ (no restriction)	64

The minimum CU size of MH-Intra is 8x8.

← Propose it

Best trade-off between gain and complexity according to test.

Summary of the combinations with other tools

LIC with	Proposal	Comments
Affine	N	Same as JEM LIC
ATMVP	N	Disable LIC
HMVP	Y	
PAIR AVG	N	Less correlation
MMVD	Y	
GBi / Bi-pred	Y	
BIO	N	Same as JEM LIC
MHIntra	Y	Large CU only
Triangle	N	Less correlation
CPR	N	Less correlation
VPDU split	Y	Calculate LIC parameter at 1st VPDU only
OBMC	N	It has pipeline issue
DMVR	Y	
Diffusion filter	N	It has pipeline issue

Simulation results

Anchor : VTM-3.0

Test : Proposed LIC (the present proposal)

	Random Access Main 10				
	Y	U	V	EncT	DecT
Class A1	-0.88%	-0.53%	-0.88%	151%	99%
Class A2	-0.32%	-0.13%	-0.20%	126%	100%
Class B	-0.54%	-0.22%	-0.23%	131%	99%
Class C	-0.28%	-0.30%	-0.20%	137%	101%
Class E					
Overall	-0.49%	-0.29%	-0.35%	135%	100%
Class D	-0.01%	0.09%	0.00%	133%	101%
Class F	-0.85%	-0.55%	-0.49%	128%	101%

Low delay B Main10				
Y	U	V	EncT	DecT
-0.70%	-0.93%	-0.51%	148%	99%
-0.45%	-0.44%	-0.49%	160%	103%
-0.13%	-0.20%	-0.44%	105%	101%
-0.47%	-0.59%	-0.49%	140%	101%
-0.06%	-0.08%	-0.17%	150%	102%
-2.68%	-1.79%	-2.24%	150%	101%

Interesting gain with small decoder complexity

Additional result (information only)

Anchor : VTM-3.0

Test : CE10.5.2 LIC (JVET-M0087)

	Random Access Main 10					Low delay B Main10				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	-0.97%	-0.60%	-0.91%	151%	99%					
Class A2	-0.38%	-0.14%	-0.22%	126%	100%					
Class B	-0.60%	-0.22%	-0.24%	131%	99%	-0.77%	-0.85%	-0.80%	149%	100%
Class C	-0.35%	-0.34%	-0.23%	137%	100%	-0.49%	-0.22%	-0.54%	161%	102%
Class E						-0.08%	-0.04%	-0.27%	106%	101%
Overall	-0.56%	-0.31%	-0.37%	135%	99%	-0.51%	-0.44%	-0.58%	140%	101%
Class D	-0.04%	-0.04%	-0.15%	133%	99%	-0.11%	-0.44%	-0.39%	151%	101%
Class F	-0.88%	-0.57%	-0.51%	128%	99%	-2.64%	-2.10%	-1.93%	151%	101%

The present proposal has 0.07% loss compared to CE10.5.2 LIC.
Most of loss comes from MH-Intra restriction.

Additional result (information only)

Anchor : VTM-3.0

Test : Proposed LIC + disable MH-Intra for all CUs using LIC

	Random Access Main 10					Low delay B Main10				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	-0.78%	-0.58%	-0.78%	151%	99%					
Class A2	-0.30%	-0.13%	-0.22%	126%	101%					
Class B	-0.49%	-0.17%	-0.32%	131%	99%	-0.68%	-0.86%	-0.60%	148%	100%
Class C	-0.28%	-0.28%	-0.16%	137%	101%	-0.44%	-0.25%	-0.59%	160%	102%
Class E						-0.03%	-0.18%	-0.25%	105%	103%
Overall	-0.45%	-0.27%	-0.35%	135%	100%	-0.44%	-0.49%	-0.51%	139%	101%
Class D	0.01%	0.01%	-0.13%	133%	100%	-0.04%	0.22%	-0.30%	149%	102%
Class F	-0.87%	-0.62%	-0.51%	128%	101%	-2.66%	-1.50%	-1.90%	150%	101%

It can simplify the combination of LIC and MH-Intra.
But it has 0.04% loss compared to the present proposal.

Additional result (information only)

Anchor : VTM-3.0

Test : Proposed LIC + disable LIC for small CU (≤ 128 samples)

	Random Access Main 10					Low delay B Main10				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	-0.90%	-0.55%	-0.86%	144%	99%					
Class A2	-0.30%	-0.20%	-0.18%	119%	101%					
Class B	-0.51%	-0.11%	-0.23%	124%	99%	-0.71%	-0.77%	-0.59%	138%	99%
Class C	-0.20%	-0.19%	-0.21%	123%	101%	-0.31%	0.00%	-0.13%	137%	102%
Class E						-0.05%	-0.52%	-0.37%	105%	103%
Overall	-0.46%	-0.24%	-0.34%	126%	100%	-0.41%	-0.45%	-0.38%	129%	101%
Class D	0.04%	0.09%	-0.04%	117%	100%	-0.04%	-0.22%	-0.22%	124%	103%
Class F	-0.71%	-0.50%	-0.44%	125%	100%	-2.27%	-1.42%	-1.79%	145%	102%

9% encoder speed-up with 0.03% loss compared to the present proposal.
We think it worth to continue the study.

- We propose to introduce following restrictions on top of CE10.5.2 LIC:
 - Calculate LIC parameter only for the first VPDU in the CU. → 0.01% loss
 - Disable LIC when ATMVP is selected. → 0.01% loss
 - Disable MH-Intra when LIC is selected in small CU ($\leq 16 \times 16$). → 0.05% loss
 - It can solve the pipeline issue for LIC.
 - 0.49%, 0.47% gain for RA, LDB on VTM-3.0.
- ➡ It is proposed to adopt the above three restrictions into test model on top of CE10.5.2.

Thank Technicolor for cross-checking of the proposal.

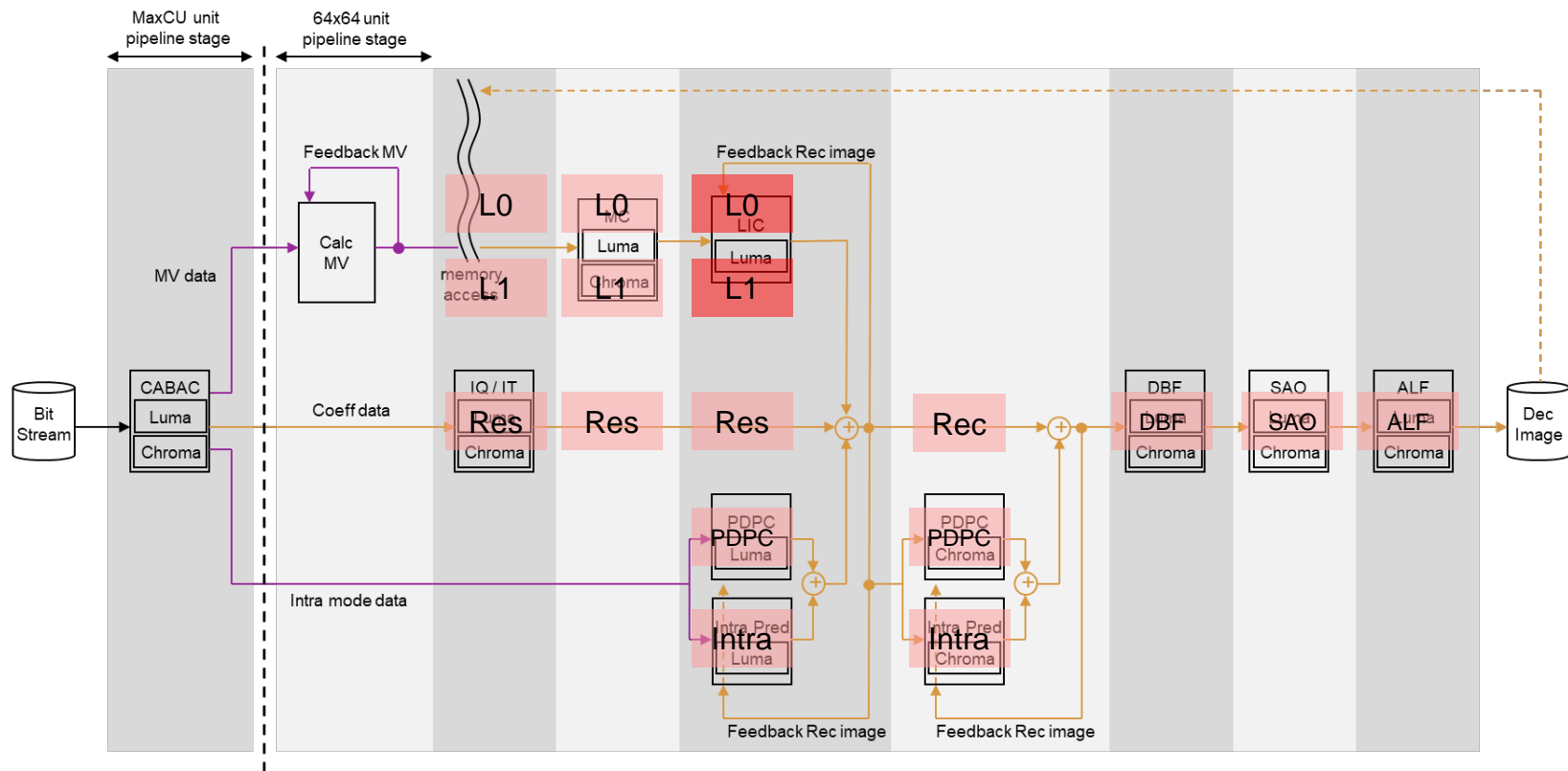
Additional explanation

Without LIC



How about additional memory?

With LIC



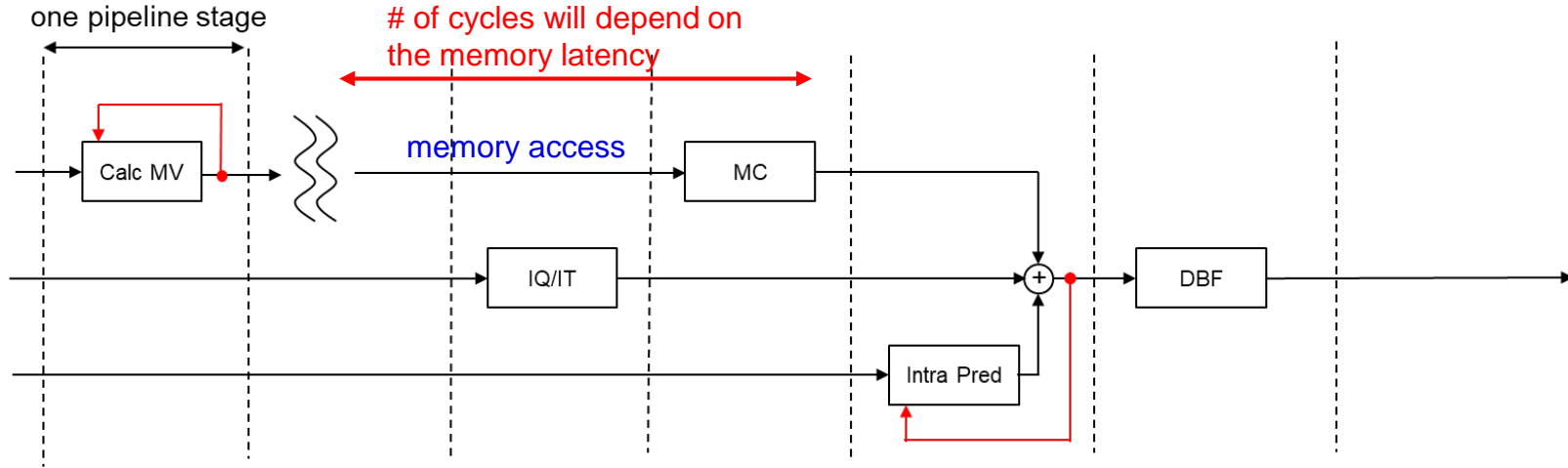
How about additional memory?

Yes, proposed LIC need additional memory.
But the impact is less than 10%.

Some other LIC related proposals solve this issue.

Inter process has to be finished at the stage before intra?

Without LIC

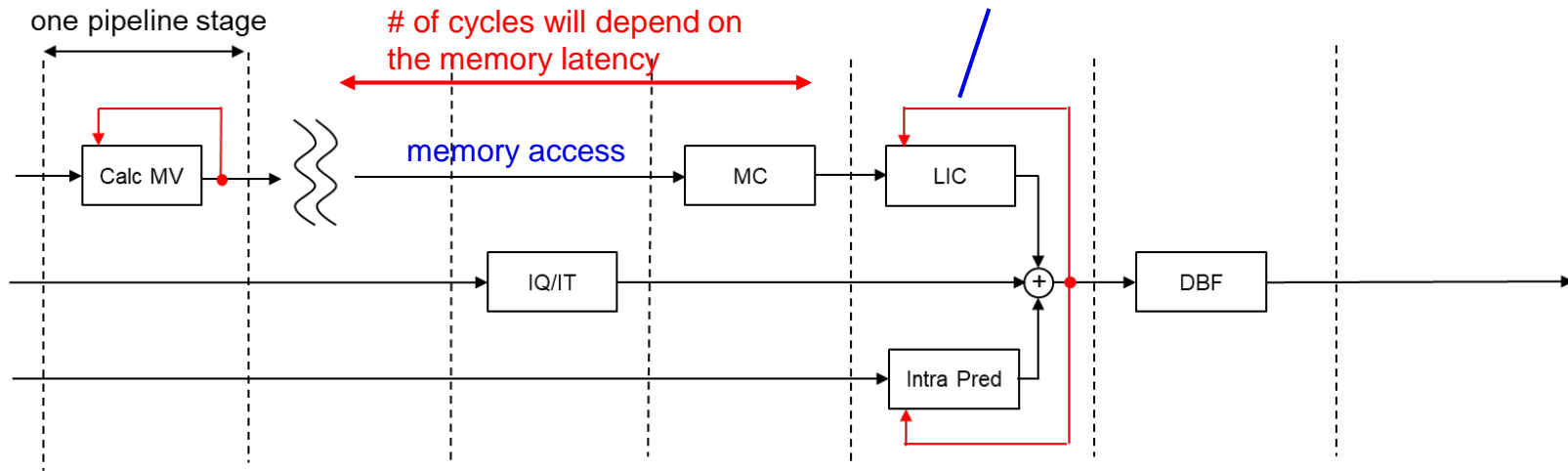


In many architectures, Inter process tend to implement at early stage to avoid the delay cause of memory access latency.

Inter process has to be finished at the stage before intra?

With LIC

of cycle of LIC process is always guaranteed, and it is less than intra process.



Inter process before LIC has same situation, but LIC process itself can be guaranteed the number of cycle. It has no problem if the LIC cycles is small enough compared to intra cycles.