



**JVET-P0540**

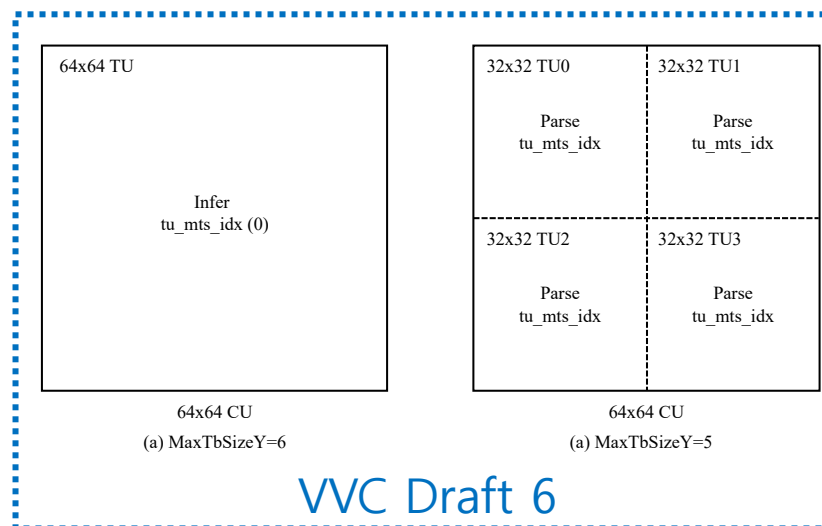
**Non-CE6: Disabling MTS for 64xN and  
Nx64 CUs**

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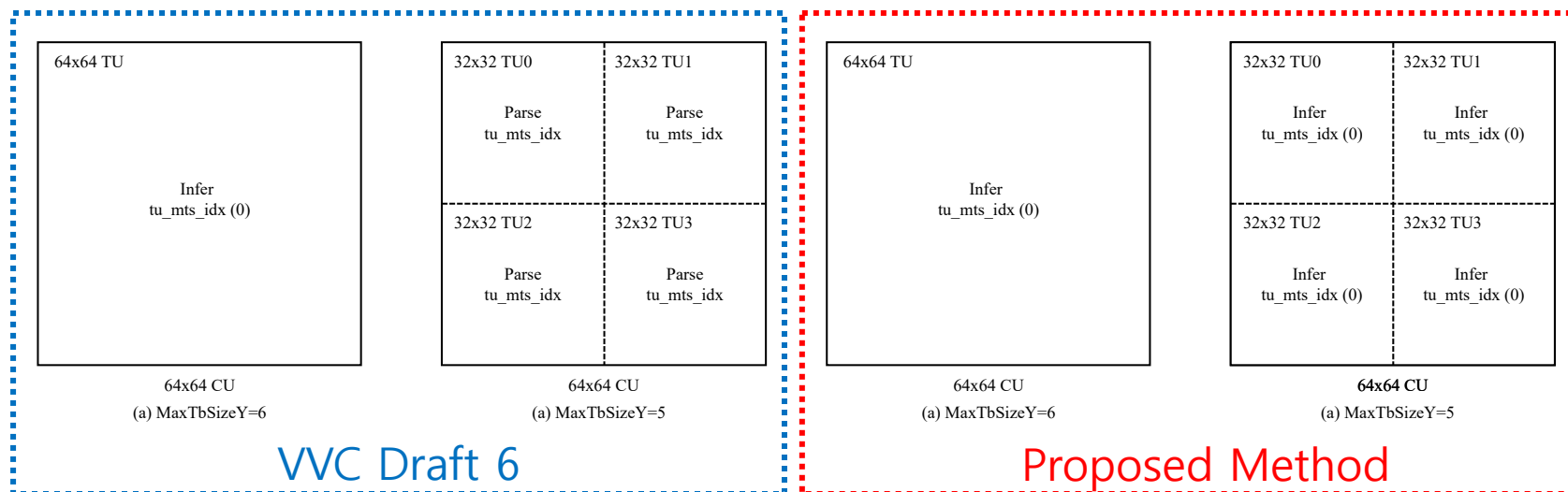
# ○ Introduction

- The maximum transform size is signalled in SPS and it can be configured to either 32 or 64 (`sps_max_luma_transform_size_64_flag`).
- When the maximum transform size is equal to 64, MTS is not allowed for  $64 \times N$  and  $N \times 64$  ( $N \geq 4$ ) CUs.
- When the maximum transform size is equal to 32, MTS is allowed for  $64 \times N$  and  $N \times 64$  ( $N \geq 4$ ) CUs.
  - The transform tree is split into four  $32 \times \text{Max}(32, N)$  and  $\text{Max}(32, N) \times 32$  TUs.
  - MTS is allowed for the implicitly partitioned TUs.
  - MTS index (`tu_mts_idx`) is signalled for each TU.



# ○ Proposed method

- It is proposed to disable MTS for 64xN and Nx64 ( $N \geq 4$ ) CUs when the maximum transform size is equal to 32.
  - {DCT-II, DCT-III} and transform skip mode are allowed for the partitioned TUs.
  - MTS index ( $tu\_mts\_idx$ ) is not coded and it is inferred to be equal to 0.



# Experimental results

## • Test 1: Intra MTS

- Anchor: VTM-6.0 + MaxTbSizeY=32
- Test: VTM-6.0 + MaxTbSizeY=32 + Disable MTS for 64xN and Nx64 CUs

	All Intra Main10					Random access Main10					Low delay B Main10				
	Over VTM-6.0+MaxTbSizeY32					Over VTM-6.0+MaxTbSizeY32					Over VTM-6.0+MaxTbSizeY32				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	-0.04%	-0.06%	-0.05%	100%	100%	-0.06%	-0.26%	-0.28%	100%	100%					
Class A2	-0.01%	-0.09%	-0.02%	100%	100%	-0.01%	0.05%	-0.12%	100%	100%					
Class B	-0.01%	-0.03%	0.05%	100%	100%	-0.02%	-0.14%	-0.03%	100%	100%	-0.01%	0.01%	0.11%	100%	100%
Class C	0.00%	0.01%	-0.01%	100%	100%	0.01%	0.02%	0.00%	100%	100%	-0.03%	-0.16%	-0.16%	100%	100%
Class E	-0.03%	-0.08%	-0.20%	100%	101%						-0.15%	-0.23%	-1.17%	100%	100%
<b>Overall</b>	-0.02%	-0.04%	-0.03%	100%	100%	-0.02%	-0.08%	-0.09%	100%	100%	-0.05%	-0.11%	-0.30%	100%	100%
Class D	0.00%	0.02%	0.03%	99%	100%	0.01%	-0.03%	0.00%	100%	100%	0.03%	0.46%	0.29%	100%	100%
Class F	0.02%	-0.01%	-0.03%	101%	100%	-0.03%	0.04%	-0.22%	100%	100%	-0.07%	-0.29%	0.51%	100%	100%

## • Test 2: Intra & inter MTS

- Anchor: VTM-6.0 + MaxTbSizeY=32 + MTS=3
- Test: VTM-6.0 + MaxTbSizeY=32 + MTS=3 + Disable MTS for 64xN and Nx64 CUs

	Random access Main10					Low delay B Main10				
	Over VTM-6.0+MaxTbSizeY32+MTS3					Over VTM-6.0+MaxTbSizeY32+MTS3				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	0.02%	-0.44%	-0.61%	91%	100%					
Class A2	0.10%	-0.12%	-0.29%	92%	100%					
Class B	0.03%	-0.14%	-0.25%	93%	100%	0.10%	-0.21%	0.00%	92%	100%
Class C	-0.02%	-0.04%	-0.05%	95%	100%	-0.11%	-0.13%	-0.04%	95%	100%
Class E						-0.38%	-1.25%	-1.40%	88%	101%
<b>Overall</b>	0.03%	-0.17%	-0.28%	93%	100%	-0.09%	-0.44%	-0.36%	92%	100%
Class D	-0.02%	-0.09%	-0.06%	97%	100%	-0.06%	0.04%	0.24%	97%	100%
Class F	-0.02%	0.03%	-0.18%	95%	100%	-0.11%	0.17%	-0.34%	94%	100%



# ○ Conclusion

- In this contribution, it is proposed to disallow MTS for  $64 \times N$  and  $N \times 64$  ( $N \geq 4$ ) CUs when the maximum transform size is equal to 32.
  - This would harmonize the maximum CU block size that can utilize MTS as  $32 \times 32$  irrespective of the signaled maximum transform size.
  - It is reported that the proposed method achieves coding efficiency improvements when the maximum transform size is configured to 32 in VTM-6.0.
  - When inter MTS is enabled, the proposed method can significantly reduce encoding time.
- It is recommended to adopt the proposed method into the next version of draft text and reference software.
- Thank Tencent for cross-check

