

JVET-L0382

CE9-related: DMVR with Coarse-to-Fine Search and Block Size Limit

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■ Problem statement

- Various DMVR designs are now studied in CE9.2.
- It is necessary that reducing complexity of DMVR

■ Proposal

1. Coarse-to-Fine search

- With 10 points and 3 stages search for search range 2 in our proposal

2. Block size restriction

- Disallow DMVR at large CU

■ Over -1.0% gain is confirmed with reducing complexity anchor: BMS2.1 rc1 with VTM configuration

- **Bilateral DMVR process is included in BMS2.1 (rc1)**
 - 13 points with 5 stages search in the max. case
- **No block size restriction in BMS2.1**
 - Max. CU size = 128 x 128
- **It is necessary that reducing complexity of DMVR**
 - That is one of topics of CE9.2 (DMVR design)
- **Our proposal is implemented on top of the BMS-2.1 rc1 software**
 - Bilateral search
 - Cost function : MRSAD
 - Interpolation filter : DCTIF

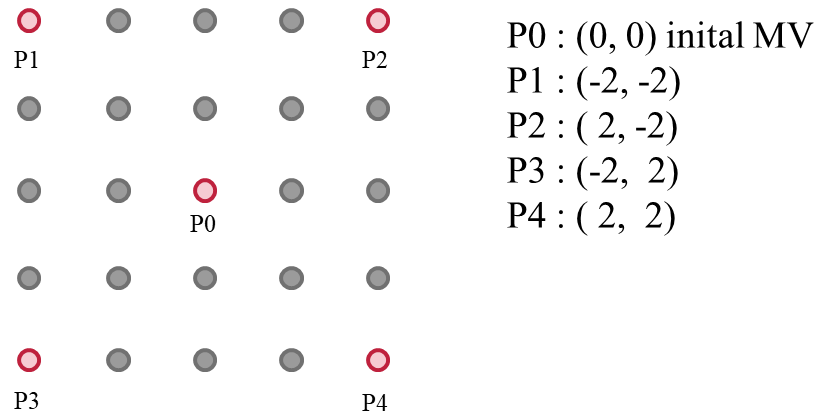
Proposal 1 : Coarse-to-Fine Search

■ 1st Stage

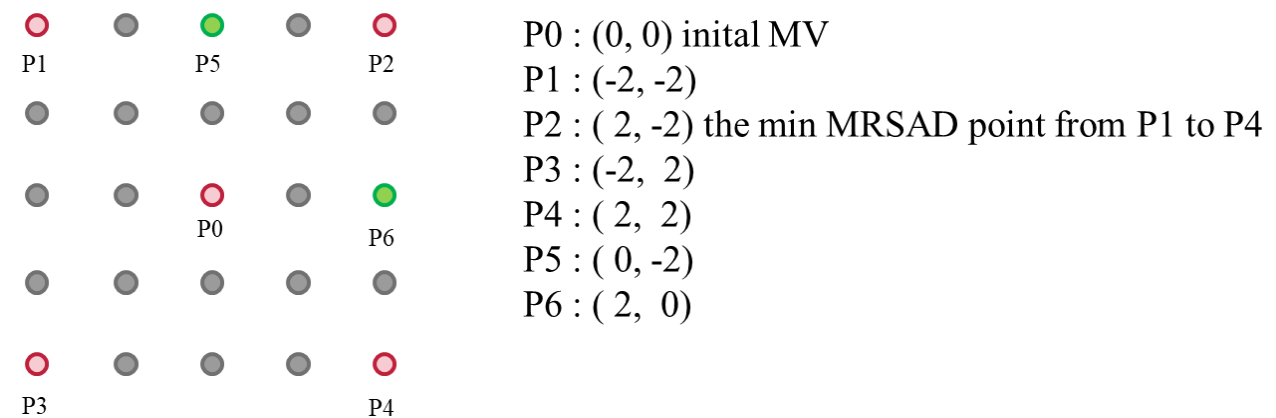
- Calculate MRSAD for 5 points (P0, P1, P2, P3, and P4)

■ 2nd Stage

- Find the minimum MRSAD point Pa among P1, P2, P3, and P4.
 - Pa : (pa_x, pa_y)
- Calculate MRSAD for following 2 points
 - P5 : (0, pa_y)
 - P6 : (pa_x, 0)



1st Stage



2nd Stage

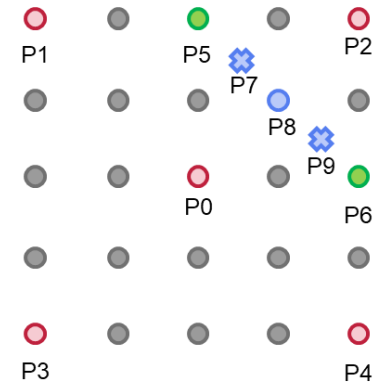
■ 3rd Stage

- Find the 1st and 2nd minimum MRSAD point **Pb** and **Pc** among **P0**, **Pa**, **P5**, and **P6**.
 - **Pb** : (pb_x, pb_y) the min MRSAD point in **P0**, **Pa**, **P5**, and **P6**
 - **Pc** : (pc_x, pc_y) the 2nd min MRSAD point in **P0**, **Pa**, **P5**, and **P6**
- Calculate MRSAD for following 3 points (1 integer pixel and 2 half pixel)
 - **P7** : $(Pc - Pb) / 4 + Pb$
 - **P8** : $(Pc - Pb) / 2 + Pb$
 - **P9** : $(Pc - Pb) * 3 / 4 + Pb$

- The minimum MRSAD point among **P0** to **P9** (actually **Pb**, **P7**, **P8** or **P9**) is decided to final MV point.

- Search points are reduced 13 to 10

- Search stages are reduced 5 to 3



P0 : (0, 0) initial MV
P1 : (-2, -2)
P2 : (2, -2) the min MRSAD point from **P1** to **P4**
P3 : (-2, 2)
P4 : (2, 2)
P5 : (0, -2) the min MRSAD point in **P0**, **P2**, **P5**, **P6**
P6 : (2, 0) the 2nd min MRSAD point in **P0**, **P2**, **P5**, **P6**
P7 : (0.5, -1.5)
P8 : (1, -1)
P9 : (1.5, -0.5)

3rd Stage

- We added following condition to execution condition of DMVR
 - Block size (number of pixels in CU) is equal to or less than 4,096 pixels.
 - e.g. 4,096 pixels = 64 x 64 pixels

- The solution enables to process per 4,096 pixels unit for each CTU.
 - **The solution enables to reduce circuit for MRSAD to 1 / 4**, compared to in case of no CU size restriction (= Max. CU size is 16,384)
 - The solution also enables to reduce memory as pointed out in JVET-L0098

Experimental results for Coarse-to-fine search (Proposal 1) and Block size restriction (Proposal 2)

| | Random Access Main 10 | | | | |
|-----------------|---|--------|--------|------|------|
| | Over BMS-2.1 rc1 with VTM configuration | | | | |
| | Y | U | V | EncT | DecT |
| Class A1 | -1.33% | -1.19% | -1.51% | 104% | 108% |
| Class A2 | -1.56% | -1.73% | -1.76% | 104% | 110% |
| Class B | -0.82% | -0.96% | -1.04% | 105% | 113% |
| Class C | -0.82% | -1.06% | -1.05% | 105% | 120% |
| Overall | -1.07% | -1.19% | -1.28% | 105% | 113% |
| Class D | -0.83% | -1.00% | -1.08% | 106% | 122% |

Experimental results for Coarse-to-fine search (Proposal 1) only

| | Random Access Main 10 | | | | |
|-----------------|---|--------|--------|------|------|
| | Over BMS-2.1 rc1 with VTM configuration | | | | |
| | Y | U | V | EncT | DecT |
| Class A1 | -1.61% | -1.49% | -1.83% | 105% | 116% |
| Class A2 | -1.71% | -1.89% | -1.93% | 105% | 116% |
| Class B | -0.88% | -1.05% | -1.14% | 106% | 121% |
| Class C | -0.82% | -1.05% | -1.05% | 106% | 123% |
| Overall | -1.18% | -1.31% | -1.41% | 105% | 120% |
| Class D | -0.83% | -1.00% | -1.09% | 107% | 123% |

■ Proposal

1. Coarse-to-Fine search : enables to reduce calculation and pipeline stage

- Search points : 13 (BMS2.1 rc1) -> 10
- Search stages : 5 (BMS2.1 rc1) -> 3

2. Block size restriction : enables to reduce circuit for MRSAD

- Enables to reduce circuit for MRSAD to 1 / 4.

■ Over -1.0% gain is confirmed with marginal complexity increment on top of the VTM

■ Proposal is recommended to further study in CE9.