



MEDIATEK

JVET-K0081

CE1.2.1: Constraint for binary and ternary partitions

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Overall Summary

- One constraint is proposed for BT and TT to allow 64x64-L/32x32-C pipelining to be used in VVC hardware decoders
- Four methods are implemented to satisfy the constraint

		Over VTM2.0.1				
		Y	U	V	EncT	DecT
CE1.2.1.1 Encoder-only BT & TT constraints	RA	0.26	0.35	0.25	95%	104%
	LB	0.30	0.23	0.20	98%	101%
CE1.2.1.2 Normative BT & TT constraints	RA	0.15	0.20	0.14	94%	101%
	LB	0.06	0.09	-0.15	98%	100%
CE1.2.1.3 Set maximum BT and TT size to 64	RA	0.35	0.43	0.27	87%	101%
	LB	0.22	0.21	0.13	91%	101%
CE1.2.1.4 Force 128x128 CTU to split into four 64x64 CUs	RA	1.55	1.28	1.15	83%	99%
	LB	0.95	0.75	0.60	87%	99%

Virtual Pipeline Data Unit (VPDU)

- VPDUs are non-overlapping $M \times M$ -luma(L)/ $N \times N$ -chroma(C) units in a picture.
- In hardware decoders, successive VPDUs are processed by multiple pipeline stages at the same time; different stages process different VPDUs simultaneously.
- The VPDU size is roughly proportional to the buffer size in most pipeline stages, so it is very important to keep it small.
- VPDU size can be set to maximum transform block (TB) size for HEVC hardware decoding.

Problem Definition

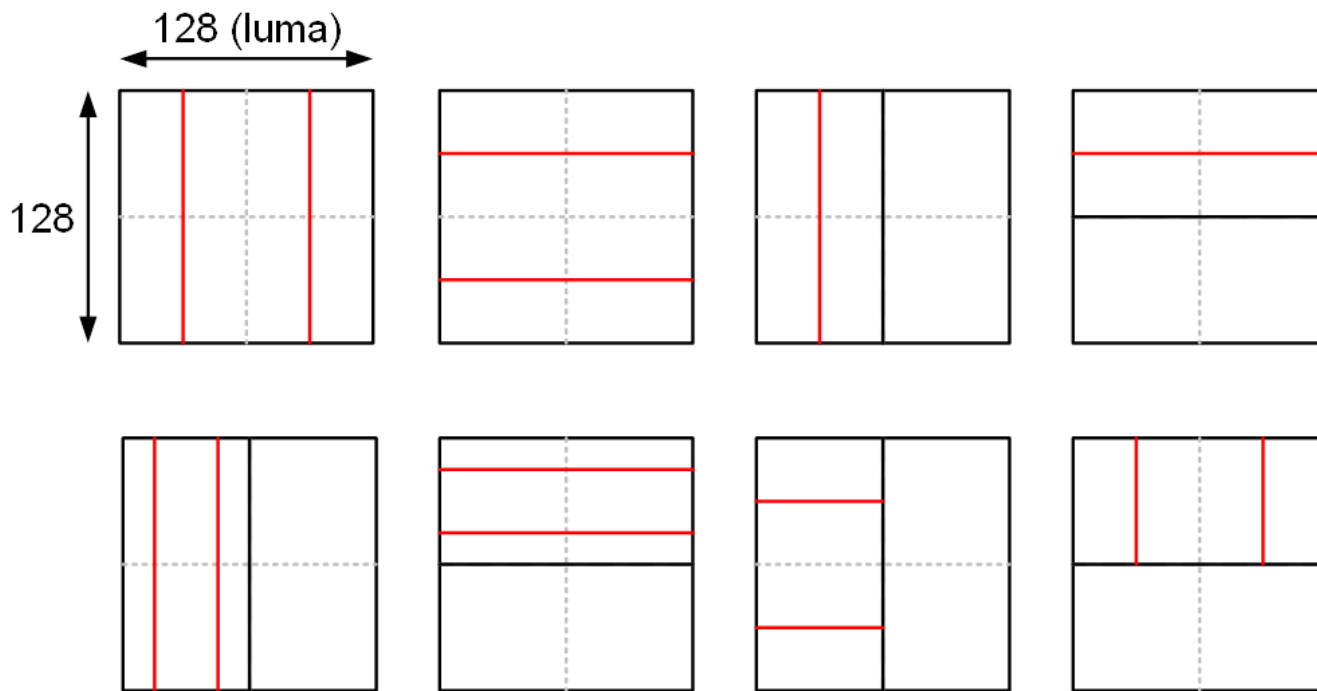
- Enlarging maximum TB size from $32 \times 32\text{-L}/16 \times 16\text{-C}$ to $64 \times 64\text{-L}/32 \times 32\text{-C}$ leads to expected VPDU size equal to $64 \times 64\text{-L}/32 \times 32\text{-C}$.
- However, ternary tree (TT) and binary tree (BT) will result in VPDU size equal to $128 \times 128\text{-L}/64 \times 64\text{-C}$.
- To reduce VPDU size to $64 \times 64\text{-L}/32 \times 32\text{-C}$, one constraint is proposed.

Proposed Method

- Definition of VPDUs: non-overlapping 64x64-L/32x32-C units in a picture
- Condition 1: For each VPDU containing one or multiple CUs, the CUs are completely contained in the VPDU.
- Condition 2: For each CU containing one or more VPDUs, the VPDUs are completely contained in the CU.
- Proposed constraint: For each CTU, the above two conditions shall not be violated, and the processing order of CUs shall not leave a VPDU and re-visit it later.

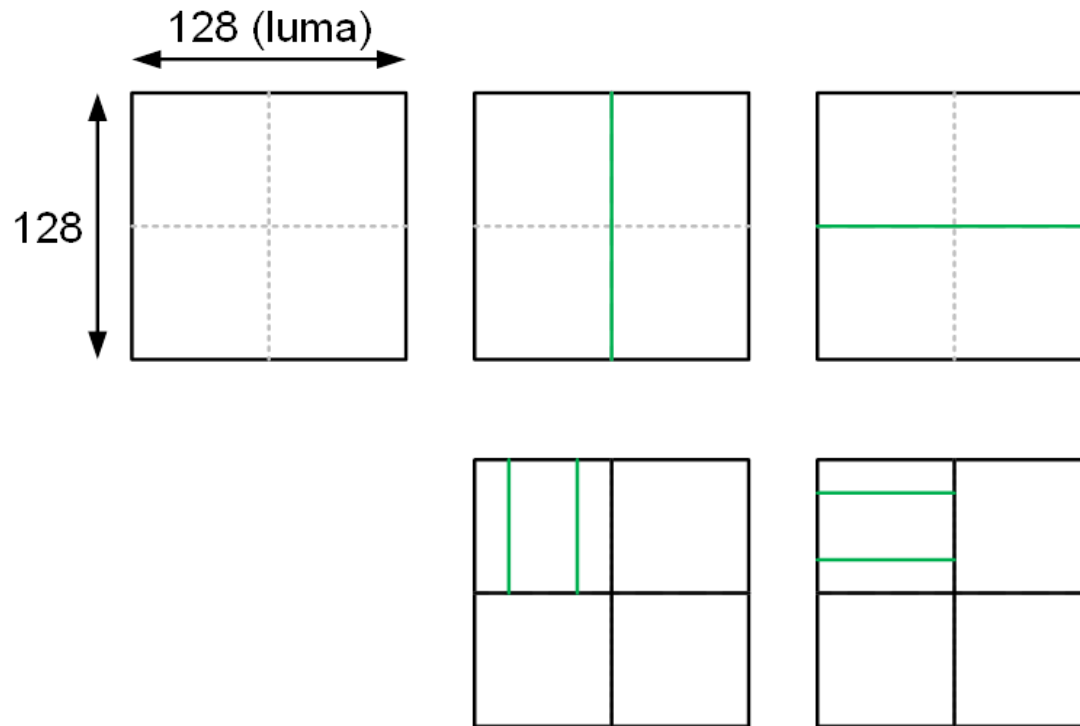
TT and BT Splits Bad for 64x64-L/32x32-C Pipelining

- CTU size: 128x128-luma/64x64-chroma
- VPDU size: 64x64-luma/32x32C (indicated by dashed lines)



TT and BT Splits Good for 64x64-L/32x32-C Pipelining

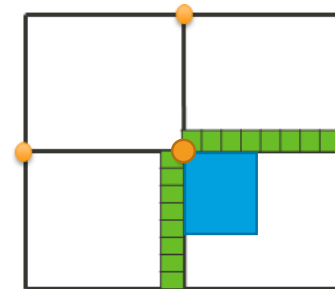
- (VPDUs indicated by dashed lines)



Implementation

- CE1.2.1.1: Encoder only BT & TT constraints

```
If (the above-left position of the current CU is the above-left position of a VPDU) {  
  If (the current CU width is larger than 64 and the current CU width is not multiples of 64)  
    Return FALSE  
  If (the current CU height is larger than 64 and the current CU height is not multiples of 64)  
    Return FALSE  
  If (the VPDU to the left and the VPDU to the top of the current CU are not yet completely encoded)  
    Return FALSE  
  
  Return TRUE  
} Else {  
  If (the current CU is completely contained by a VPDU)  
    Return TRUE  
  Else  
    Return FALSE  
}
```



FALSE: current CU is invalid; TRUE: current CU is valid.

Implementation

- CE1.2.1.2: Normative BT & TT constraints
 - For a 128x128 CTU, it shall not be partitioned by a TT split.
 - For a 128xN or Nx128 CU, it shall not be partitioned by a TT split, where $N \leq 64$.
 - For a 128xN CU, horizontal BT cannot be applied, where $N \leq 64$.
 - For an Nx128 CU, vertical BT cannot be applied, where $N \leq 64$.
- CE1.2.1.3: Set maximum BT and TT size to 64
- CE1.2.1.4: Force QT split when CU width or height is larger than 64

Experimental Results

		Over VTM2.0.1				
		Y	U	V	EncT	DecT
CE1.2.1.1 Encoder-only BT & TT constraints	AI	0.00	0.00	0.00	100%	100%
	RA	0.26	0.35	0.25	95%	104%
	LB	0.30	0.23	0.20	98%	101%
CE1.2.1.2 Normative BT & TT constraints	AI	0.00	0.00	0.00	100%	101%
	RA	0.15	0.20	0.14	94%	101%
	LB	0.06	0.09	-0.15	98%	100%
CE1.2.1.3 Set maximum BT and TT size to 64	AI	0.00	0.00	0.00	100%	100%
	RA	0.35	0.43	0.27	87%	101%
	LB	0.22	0.21	0.13	91%	101%
CE1.2.1.4 Force 128x128 CTU to split into four 64x64 CUs	AI	0.00	0.00	0.00	100%	101%
	RA	1.55	1.28	1.15	83%	99%
	LB	0.95	0.75	0.60	87%	99%

Experimental Results

CE1.2.1.1: Encoder-only
BT & TT constraints

CE1.2.1.2: Normative BT
& TT constraints

CE1.2.1.3: Set maximum
BT and TT size to 64

CE1.2.1.4: Force 128x128
CTU to be split into four
64x64 CUs

	All Intra Main10					All Intra Main10					All Intra Main10					All Intra Main10				
	Over VTM2.0.1					Over VTM2.0.1					Over VTM2.0.1					Over VTM2.0.1				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	0.00%	0.00%	0.00%	101%	99%	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	100%
Class A2	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	101%	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	100%
Class B	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	101%	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	100%
Class C	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	99%	101%	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	100%
Class E	0.00%	0.00%	0.00%	100%	99%	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	100%
Overall	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	101%	0.00%	0.00%	0.00%	100%	100%	0.00%	0.00%	0.00%	100%	100%
Class D	0.00%	0.00%	0.00%	100%	99%	0.00%	0.00%	0.00%	100%	102%	0.00%	0.00%	0.00%	100%	102%	0.00%	0.00%	0.00%	100%	100%

	Random Access Main 10					Random Access Main 10					Random Access Main 10					Random Access Main 10				
	Over VTM2.0.1					Over VTM2.0.1					Over VTM2.0.1					Over VTM2.0.1				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	0.41%	0.60%	0.48%	90%	102%	0.22%	0.32%	0.22%	90%	100%	0.69%	0.88%	0.63%	78%	101%	2.66%	2.32%	2.21%	73%	104%
Class A2	0.52%	0.48%	0.38%	94%	101%	0.38%	0.34%	0.26%	94%	101%	0.67%	0.64%	0.45%	86%	102%	2.87%	2.27%	2.04%	82%	102%
Class B	0.21%	0.30%	0.22%	95%	102%	0.08%	0.16%	0.11%	95%	100%	0.24%	0.28%	0.16%	88%	101%	1.25%	0.96%	0.88%	84%	101%
Class C	0.03%	0.14%	0.03%	98%	99%	0.02%	0.07%	0.04%	98%	101%	0.01%	0.11%	0.01%	95%	100%	0.10%	0.14%	0.04%	94%	100%
Overall	0.26%	0.35%	0.25%	95%	101%	0.15%	0.20%	0.14%	94%	101%	0.35%	0.43%	0.27%	87%	101%	1.55%	1.28%	1.15%	84%	102%
Class D	0.08%	0.15%	0.09%	98%	100%	0.00%	-0.01%	0.03%	98%	100%	0.06%	0.10%	0.01%	94%	99%	0.06%	0.13%	-0.04%	93%	98%

	Low delay B Main10					Low delay B Main10					Low delay B Main10					Low delay B Main10				
	Over VTM2.0.1					Over VTM2.0.1					Over VTM2.0.1					Over VTM2.0.1				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class B	0.15%	0.21%	0.02%	97%	100%	0.06%	0.07%	-0.16%	98%	101%	0.17%	0.08%	0.14%	92%	102%	0.85%	0.49%	0.30%	89%	99%
Class C	0.06%	0.08%	0.03%	99%	99%	0.02%	0.01%	-0.17%	99%	101%	0.05%	0.07%	-0.21%	98%	101%	0.10%	-0.13%	0.11%	97%	99%
Class E	0.85%	0.45%	0.74%	96%	101%	0.10%	0.22%	-0.12%	95%	97%	0.51%	0.60%	0.55%	81%	100%	2.26%	2.35%	1.78%	73%	100%
Overall	0.30%	0.23%	0.20%	98%	100%	0.06%	0.09%	-0.15%	98%	100%	0.22%	0.21%	0.13%	91%	101%	0.95%	0.75%	0.60%	87%	100%
Class D	0.10%	0.49%	-0.55%	100%	99%	0.06%	0.28%	0.01%	99%	100%	0.05%	0.15%	0.13%	98%	99%	0.05%	0.46%	-0.10%	97%	99%

Conclusions

- One constraint is proposed for BT and TT to allow 64x64-L/32x32-C pipelining to be used in VVC hardware decoders
- Four methods are implemented to satisfy the constraint
- Suggest to adopt the method of normative BT & TT constraints in “CE1.2.1.2” to solve the hardware pipelining issue with 0.15% RA & 0.06% LB BD-rates and 6% RA & 2% LB encoding time savings, respectively.
- The method in “CE1.2.1.1” can be applied at decoder as an assertion check of the VPDU constraint