

I0162: Non-CE1, Test2.1: Reduced number of band of fsets per LCU

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Summary of changes

| HM6.0 | Proposed (I0162) |
|--|--|
| Edge OffSet | |
| 4 EOs per LCU | 1 EO per LCU |
| EO is unsigned (2 ctxs): | "EO value -1" is unsigned (2 ctxs) |
| Band OffSet | |
| Left Band position (5 bits CABAC by pass mode) | |
| 4 BOs per LCU | |
| BO is signed (3 ctxs) | BO is signed (2 ctxs, shared with EO) Sing flag is encoded with CABAC bypass mode |

Specification Changes

7.3.4.2. Sample adaptive offset CABAC syntax

| | |
|--|------------|
| sao_offset_cabac(rx, ry, cIdx) { | Descriptor |
| sao_type_idx[cIdx][rx][ry] | ae(v) |
| sao_offset[cIdx][rx][ry] | ae(v) |
| sao_offset[cIdx][rx][ry]++ | |
| if(sao_type_idx[cIdx][rx][ry] == 4) { | |
| sao_band_position[cIdx][rx][ry] | u(5) |
| for(i = 0; i < 4; i++) | |
| sao_offset[cIdx][rx][ry][i] | se(v) |
| sao_sign_flag_offset | u(1) |
| if (sao_sign_flag_offset) sao_offset[cIdx][rx][ry] = -sao_offset[cIdx][rx][ry] ; | |
| } else if(sao_type_idx[cIdx][rx][ry] != 0){ | |
| sao_offset[cIdx][rx][ry][0] | ae(v) |
| sao_offset[cIdx][rx][ry][1] | ae(v) |
| sao_offset[cIdx][rx][ry][2] | ae(v) |
| sao_offset[cIdx][rx][ry][3] | ae(v) |
| sao_offset[cIdx][rx][ry][2] = -sao_offset[cIdx][rx][ry][2] | |
| sao_offset[cIdx][rx][ry][3] = -sao_offset[cIdx][rx][ry][3] | |
| } | |
| } | |

Experimental results

- ❖ CE1 SW is used as an anchor
- ❖ All 8 test cases (I-main, I-HE10, RA-main, RA-HE10, LD-main, LD-HE10, LDP-main, LDP-HE10) are included
- ❖ Class F is excluded from averaging

| LCU size | 1 EO or 4 BOs per LCU | | | 1 EO or 1 BO per LCU | | |
|--------------|-----------------------|------------|------------|----------------------|------------|------------|
| | Y, BD-rate | U, BD-rate | V, BD-rate | Y, BD-rate | U, BD-rate | V, BD-rate |
| 64x64 | -0.1% | -0.1% | 0.0% | 0.0% | 0.2% | 0.3% |
| 32x32 | -0.3% | -0.3% | -0.4% | -0.3% | -0.2% | -0.1% |
| 16x16 | -0.2% | -0.1% | -0.1% | -0.4% | 0.0% | 0.1% |

Visual Quality (1)



- ❖ BasketballDrill, LD(main), LCU size 64, QP=37, frame 17: CE1 anchor (left), Proposed (right).

Visual Quality (2)



- ❖ SlideEditing, LD(main), LCU size 64, QP=37, frame 31: SAO off (left), CE1 anchor (middle), Proposed (right).

Visual Quality (1)



- ❖ Kimono, LD(main), LCU size 64, QP=37, frame 159: CE1 anchor (left), Proposed (right).

Conclusion

❖ Based on reported test results

- no drop if LCU size is 64x64
- 0.3% BD rate reduction if LCU size is 32x32;
- 0.4% BD rate reduction if LCU size is 16x16;

Samsung, Qualcomm, and MediaTek propose to reduce both number of edge and band offsets to 1 per LCU. This helps

- to reduce both average and worst case memory size for offset storage
- helps throughput since less number of bins needed to be parsed.

Thank you !