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Specialists Group on Coding for Visual Telephony

Source: PictureTel Corp.

Title: Some notes on Reed-Solomon codes

1 INTRODUCTION

A Reed-Solomon error correction code operates on an alphabet of size q, and the blocklength is q-1 symbols. If each symbol is defined to be an octet, i.e., q=256, the blocklength is 255 octets (2040 bits). A shorter blocklength can be chosen by truncating the code.

To achieve the capability to correct t symbols, 2t parity symbols are required. A double error correcting code (t=2) uses 4 octets of parity and can correct any 2 erroneous octets in a block. Hence, the code can correct any two random bit errors. It can also correct a burst that is confined to two symbols; a 9-bit burst error can always be corrected.

As shown in this document, a double-error correcting Reed-Solomon code has very attractive properties:

* Good performance for random bit errors
* Good performance for short error bursts
* Small overhead
* Easy implementation

2 PERFORMANCE

For random bit errors, the probability of having an uncorrectable error in a block of n B-bit symbols is

$$\text{pblock} = P(>t \text{ symbol errors})$$

$$= 1 - \sum_{i=0}^{t} P(i \text{ symbol errors})$$

$$= 1 - \sum_{i=0}^{t} \binom{n}{i} (1-\text{psym})^{n-i} \, \text{psym}^{i}$$

where the symbol error probability psym is

$$psym = 1 - (1-ber)^{B}$$

and ber is the bit error probability. The mean time between uncorrectable errors

$$MTBE = \frac{n\ B}{R\ pblock}$$

is plotted in Fig. 1 for t=2, B=8 bits/symbol, and R=320 kb/s. Curves for two blocklengths are plotted, the maximum blocklength n=255 and a truncated code, n=128.

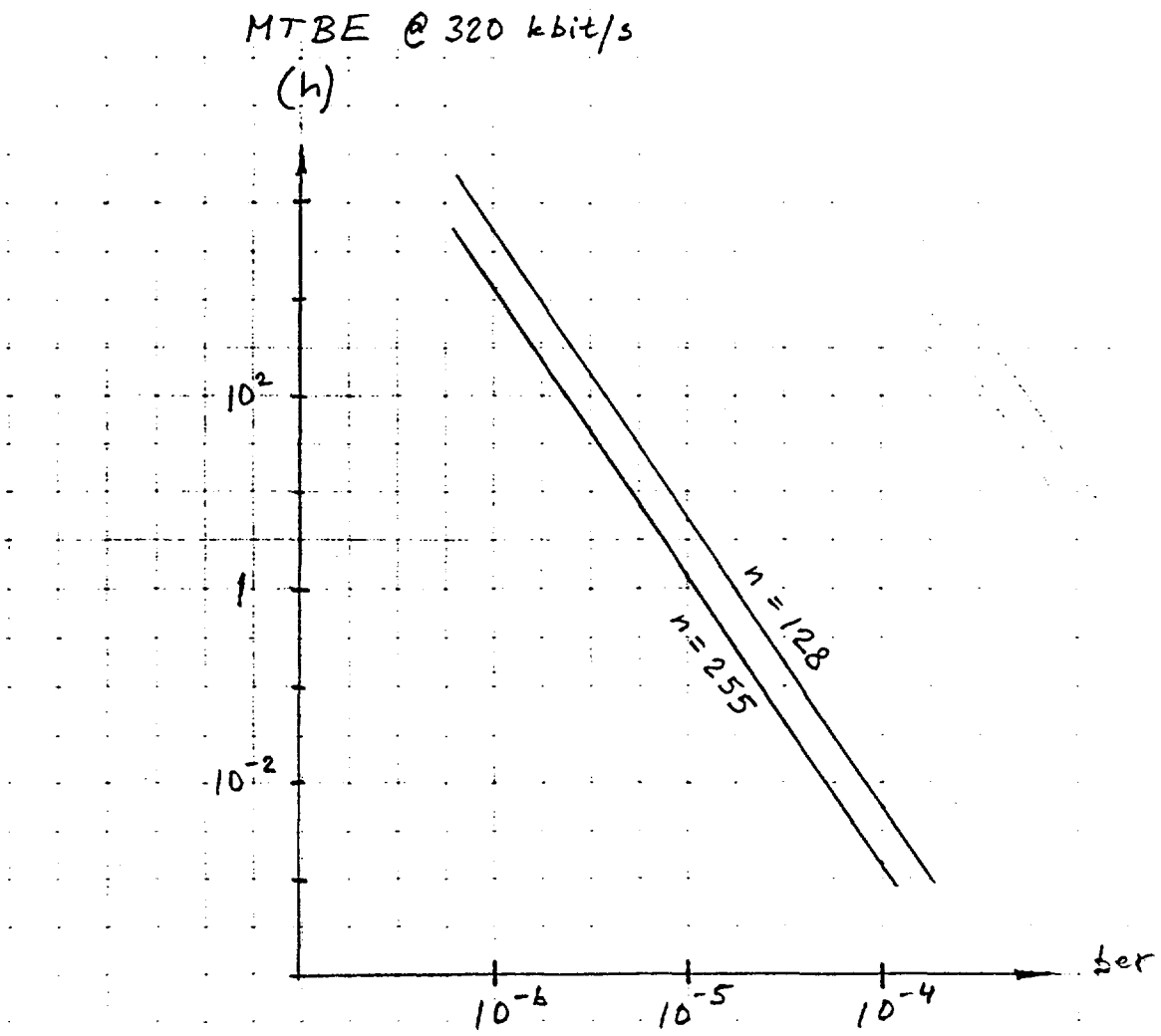

Figure 1. Mean time between errors for double-error correcting Reed-Solomon code at 320 kbit/s; B = 8 bit/symbol.

For approximate computations, the formula

$$\text{pblock} = \binom{n}{t+1} (B \cdot \text{ber})^{t+1}$$

can be used.

Redundancy and delay are listed in Table 1.

Table 1. Redundancy and delay for t=2 (double-error correcting) Reed-Solomon codes with 8 bits/symbol.

Blocklength (octets)	n=255	n=128
Blocklength (bits)	2040	1024
Redundancy (%)	1.57	3.12
Delay @ 320 kbit/s (ms)	6.38	3.20

3 IMPLEMENTATION

3.1 Encoder

In the encoder, the parity symbols are computed from the information symbols as outlined in Figure 2. Essentially, a polynomial division is performed by the circuit. Each lookup table performs a multiply by a constant. The registers are initialized to zero at the beginning of a block. At the end of the block, the parity symbols are clocked out from the registers.

Four table look-ups and four XOR operations are performed per symbol. The number of operations per second for double-error correcting Reed-Solomon codes are listed in Table 2.

Table 2. Computational requirements for parity symbol generation; t=2, B=8 bits/symbol.

Rate (kbit/s)	320	1920
Table lookups (k ops/s)	160	960
XOR's (k ops/s)	160	960

3.2 Decoder

The decoder starts by calculating syndromes according to Figure 3. At the beginning of the block, the registers are initialized to zero. At the end of the block, the four syndromes are available in the registers. The number of operations is the same as for generating the parity symbols.

If the syndromes are not zero, one or more symbols were erroneous. The errors are found by the following steps:

1. Generate an error locator polynomial.

2. Find the zeroes of the error locator polynomial to obtain the error locations.

3. Calculate the error values.

For double-error correction, these steps correspond to less than 150 operations per block. They are most easily implemented in software.

Reference: R E Blahut, Theory and Practice of Error Control Codes, Addison-Wesley 1983.

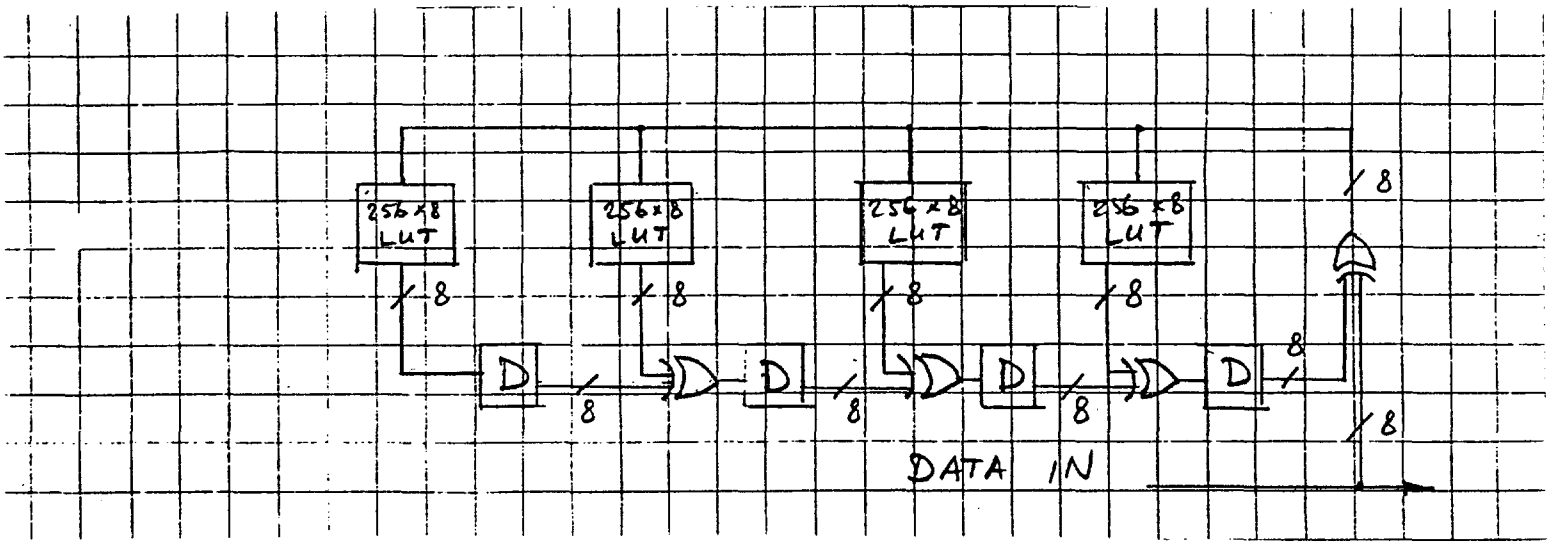

Figure 2. Parity symbol generation

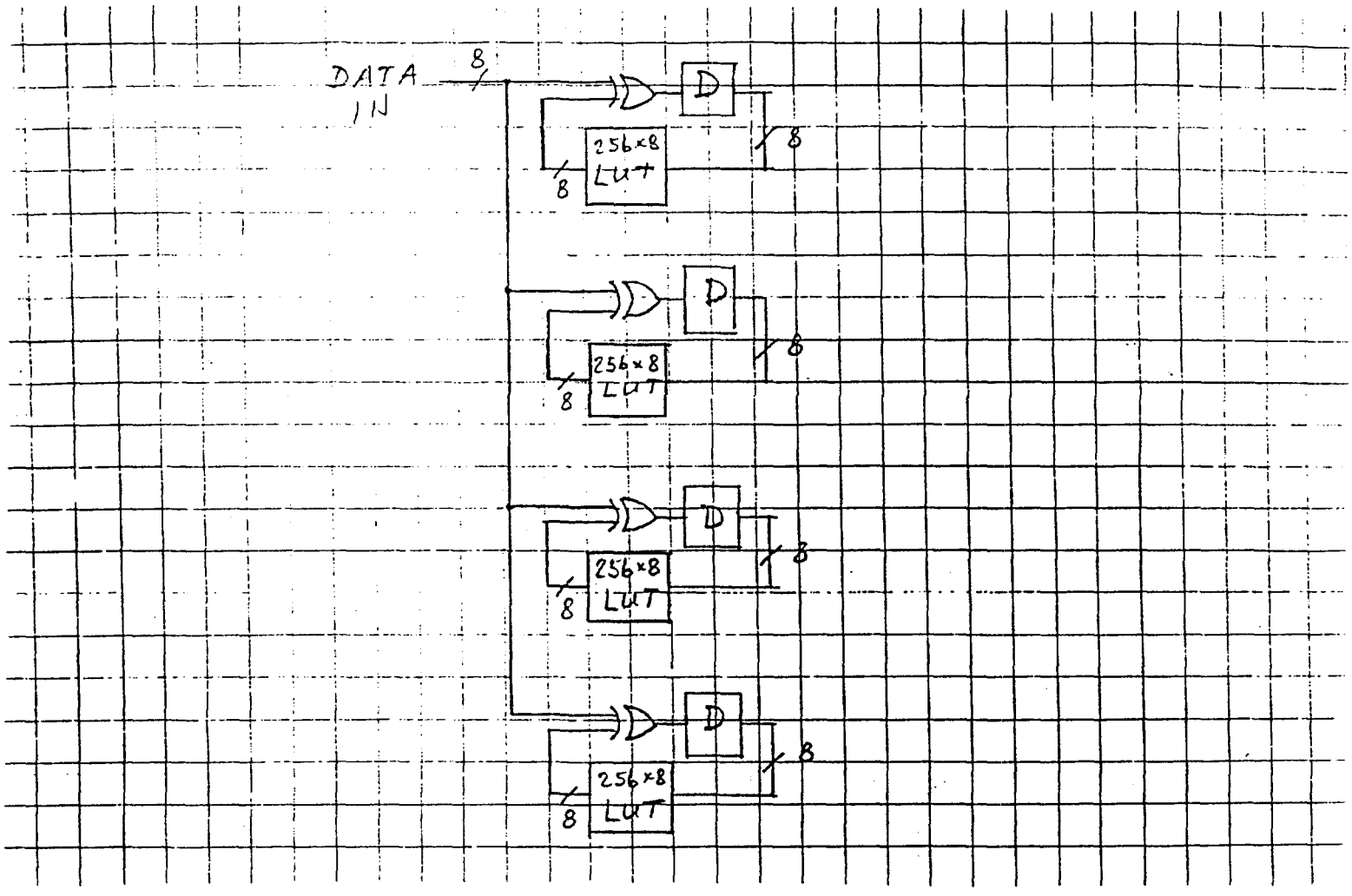

Figure 3. Syndrome generation