Telecommunication Standardization Sector
Study Group 15
Experts Group for Video Coding and Systems
in ATM and Other Network Environments
(Rapporteur's Group on Part of Q.2/15)

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Title : Hardware Experiment on Bit Errors
Purpose : Information

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1. Introduction

The specification of H.32X error resilience for ATM network is one of the study items in Experts Group. A hardware experiment has been done to investigate the influence of bit errors to coded pictures. In order to cover the wide range of the transmission rate in ATM network, a HDTV codec has been used whose video coding rate is flexible.

2. Experiments

The specifications of the HDTV codec applied are listed in Table 1, and Figure 1 shows the experiment system. The ATM network simulator in Figure 1 has the capability of generating random bit errors (error rate: $10^{-3} \sim 10^{-8}$) according to Poisson process. The area of bit errors is limited to Infomation Field (48 bytes) of ATM cells except ATM cell header and SDH layer. The next two kinds of sequences were examined in the experiment.

Sequence A: Color Bars (still picture, coded at 6Mbps)
Sequence B: Canal Scene (motion picture, coded at 100Mbps)

Each Sequence was refreshed by Intra mode in about 0.4 second. The degradation of coded pictures was observed at the bit error rate $10^{-5} \sim 10^{-8}$ with or without the error correction described in Table 1. Table 2 indicates the average interval time between points when the degradation was visually noticed. The difference between reference values and EC off values in Table 2 is considered mainly due to cyclic refreshment and error concealment in the CODEC. Some of the pictures will be demonstrated in the meeeting.

3. Conclusion

Accoding to Table 2, the average interval time at the bit error rate 10^{-9} is supposed to be less than 30 minutes $\sim$ 1 hour in both Sequence A and Sequence B. The value might be worse by the errors in ATM cell header or SDH layer which performs scramble and descramble to ATM cell payload.

The results of this document support the argument of AVC-657 that bit error correction is mandatory at the bit error rate 10^{-9} namely Best Case.

Table 1 HDTV CODEC Specifications

Video Coding	H.261 base
Media Multiplex	VC Multiplex
AAL	Type 1
T/R Interface	155.52Mbps, including SDH
Error Correction*	2 bytes per 112 bytes can be corrected in the user area (47 bytes in a cell). The Function can be switched on or off.

* 4 cells for Error Correction are added to 108 Video cells using RS(112,108).

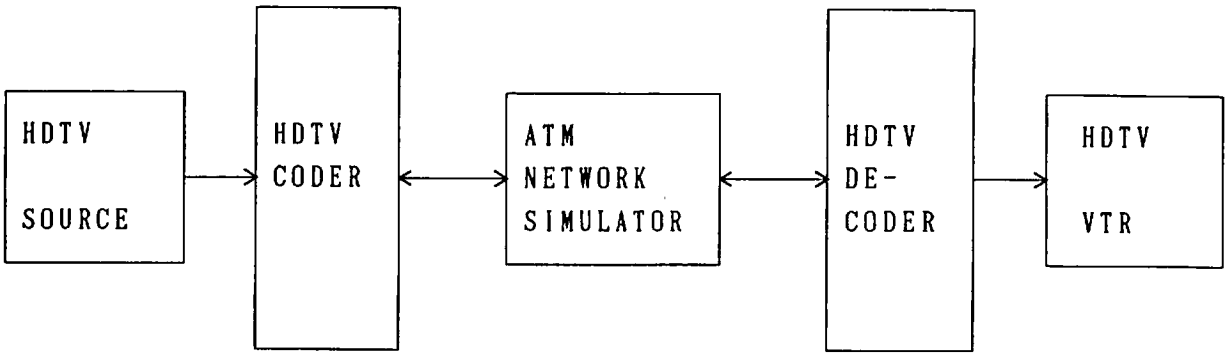

Figure 1 Experiment system

Tabel 2 Experiment Results

	Sequence A (6Mbps)			Sequence B (100Mbps)		
Bit Error Rate	reference value	EC off	EC on	reference value	EC off	EC on
10^{-8}	20 sec.	150 sec.	xxx	1 sec.	2 sec.	xxx
10^{-7}	2 sec.	15 sec.	xxx	0.1 sec.	less than 1 sec.	xxx
10^{-6}	0.2 sec.	2 sec.	xxx	0.01 sec.	less than 1 sec.	xxx
10^{-5}	0.02 sec.	less than 1 sec.	xxx	0.001 sec.	less than 1 sec.	80 sec.

EC: Error Correction

xxx: not noticed in the observation of 5 minutes order

reference value = 1 / (bit error rate * coding bit rate)

Demonstration by VCR

	Test Sequence	Bit Error Rate	Error Correction
No.1	A (6Mbps)	10^{-8}	off
No.2	A	10^{-7}	off
No.3	A	10^{-6}	off
No.4	A	10^{-5}	off
No.5	A	10^{-5}	on
No.6	B(100Mbps)	10^{-8}	off
No.7	B	10^{-7}	off
No.8	B	10^{-6}	off
No.9	B	10^{-5}	off
No.10	B	10^{-5}	on