



CE8-related: Simple BVD coding scheme without adding more context

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- Proposed Method 1
- Proposed Method 2
- Complexity Analysis
- Experimental Results
- Conclusion

- IBC mode

- Merge list:

A	B	C	D	E	F
---	---	---	---	---	---

- ABVP list:

A	B
---	---

- **Redundancy** between Merge and ABVP in IBC mode

- Merge:

A	B
---	---

- ABVP:

A	B
---	---

 + Zero BVD

- Proposed: Remove Zero BVD (BUGFIX)

- Proposed: Remove Zero BVD
 - Encoder side
 - **Terminate** RD process when BVD is zero (less EnT)
 - Encoder/Decoder side
 - Two optional modifications

<code>abs_mvd_greater0_flag[0]</code>
<code>abs_mvd_greater0_flag[1]</code>



Modification 1

<code>abs_mvd_greater0_flag[0]</code>
<code>if(!abs_mvd_greater0_flag[0])</code>
<code>abs_mvd_greater0_flag[1]</code>

Modification 2

<code>abs_mvd_greater0_flag[1]</code>
<code>if(!abs_mvd_greater0_flag[1])</code>
<code>abs_mvd_greater0_flag[0]</code>

- Proposed: Remove Zero BVD
 - Two optional modifications

Modification 1

<code>abs_mvd_greater0_flag[0]</code>
<code>if(!abs_mvd_greater0_flag[0])</code>
<code>abs_mvd_greater0_flag[1]</code>

Modification 2

<code>abs_mvd_greater0_flag[1]</code>
<code>if(!abs_mvd_greater0_flag[1])</code>
<code>abs_mvd_greater0_flag[0]</code>

- In SCC sequence
 - More zero value in **y**-axis than x-axis
 - More **greater0_flag[0]** can skip coding/parsing under **modification 2**
 - Choose **modification 2**

- Proposed: Remove Zero BVD + binarization modification
 - Binarization modification from JVET-N0458
 - abs_mvd_minus2**: from **EG1** to **EG3**

Syntax structure	Syntax element	Binarization	
		Process	Input parameters
mvd_coding()	abs_mvd_greater0_flag[]	FL	cMax = 1
	abs_mvd_greater1_flag[]	FL	cMax = 1
	abs_mvd_minus2[]	(Input == MODE_IBC) ? EG3 : EG1	CuPredMode[][]
	mvd_sign_flag[]	FL	cMax = 1

- Reuse MVD syntax and context
 - Won't introduce more context
- Similar parsing process

MVD parsing process

```

mvd_coding( x0, y0, refList ,cpldx ) {
  abs_mvd_greater0_flag[ 0 ]
  abs_mvd_greater0_flag[ 1 ]
  if( abs_mvd_greater0_flag[ 0 ] )
    abs_mvd_greater1_flag[ 0 ]
  if( abs_mvd_greater0_flag[ 1 ] )
    abs_mvd_greater1_flag[ 1 ]
  if( abs_mvd_greater0_flag[ 0 ] ) {
    if( abs_mvd_greater1_flag[ 0 ] )
      abs_mvd_minus2[ 0 ]
    mvd_sign_flag[ 0 ]
  }
  if( abs_mvd_greater0_flag[ 1 ] ) {
    if( abs_mvd_greater1_flag[ 1 ] )
      abs_mvd_minus2[ 1 ]
    mvd_sign_flag[ 1 ]
  }
}
    
```

same

Proposed BVD parsing process

```

bvd_coding( x0, y0, refList ,cpldx ) {
  abs_mvd_greater0_flag[ 1 ]
  if( !abs_mvd_greater0_flag[ 1 ] )
    abs_mvd_greater0_flag[ 0 ]
  if( abs_mvd_greater0_flag[ 0 ] )
    abs_mvd_greater1_flag[ 0 ]
  if( abs_mvd_greater0_flag[ 1 ] )
    abs_mvd_greater1_flag[ 1 ]
  if( abs_mvd_greater0_flag[ 0 ] ) {
    if( abs_mvd_greater1_flag[ 0 ] )
      abs_mvd_minus2[ 0 ]
    mvd_sign_flag[ 0 ]
  }
  if( abs_mvd_greater0_flag[ 1 ] ) {
    if( abs_mvd_greater1_flag[ 1 ] )
      abs_mvd_minus2[ 1 ]
    mvd_sign_flag[ 1 ]
  }
}
    
```

- Method 1

AI over VTM5.0					
	Y	U	V	EncT	DecT
Class A1	-0.04%	-0.07%	0.09%	139%	98%
Class A2	-0.78%	-1.06%	-0.95%	144%	98%
Class B	-0.78%	-0.69%	-0.86%	153%	98%
Class C	-0.28%	-0.29%	-0.25%	155%	103%
Class E	-1.27%	-1.23%	-1.33%	158%	102%
Overall	-0.63%	-0.65%	-0.66%	150%	100%
Class D	-0.55%	-0.46%	-0.62%	148%	101%
Class F	-0.12%	-0.11%	-0.08%	99%	98%
Class SCC	-0.43%	-0.38%	-0.41%	99%	98%

RA over VTM5.0					
	Y	U	V	EncT	DecT
Class A1	0.11%	-0.11%	0.22%	104%	99%
Class A2	-0.06%	-0.38%	-0.11%	104%	99%
Class B	-0.14%	-0.35%	-0.52%	107%	99%
Class C	0.17%	-0.18%	-0.10%	112%	101%
Class E					
Overall	0.01%	-0.26%	-0.18%	107%	100%
Class D	0.14%	-0.09%	0.11%	112%	101%
Class F	-0.12%	-0.05%	0.06%	100%	99%
Class SCC	-0.18%	-0.20%	-0.28%	100%	99%

Thank LGE for the cross-checking

- Method 2

AI over VTM5.0					
	Y	U	V	EncT	DecT
Class A1	-0.04%	-0.01%	0.01%	140%	99%
Class A2	-0.79%	-1.06%	-1.00%	144%	98%
Class B	-0.78%	-0.67%	-0.89%	155%	99%
Class C	-0.30%	-0.24%	-0.19%	156%	104%
Class E	-1.30%	-1.26%	-1.35%	159%	104%
Overall	-0.64%	-0.63%	-0.68%	151%	101%
Class D	-0.56%	-0.50%	-0.54%	149%	106%
Class F	-0.26%	-0.32%	-0.37%	100%	100%
Class SCC	-0.74%	-0.70%	-0.71%	100%	99%

RA over VTM5.0					
	Y	U	V	EncT	DecT
Class A1	0.10%	-0.20%	0.16%	104%	98%
Class A2	-0.05%	-0.30%	-0.07%	104%	98%
Class B	-0.12%	-0.28%	-0.75%	107%	99%
Class C	0.18%	-0.22%	-0.25%	112%	102%
Class E					
Overall	0.02%	-0.25%	-0.30%	107%	100%
Class D	0.10%	-0.20%	-0.17%	112%	101%
Class F	-0.20%	-0.12%	-0.15%	100%	100%
Class SCC	-0.41%	-0.37%	-0.40%	100%	100%

- JVET-O0325 proposed two simple BVD coding scheme
 - Method 1: **Remove zero BVD** to reduce redundancy in IBC mode
 - Method 2: 1 + **binarization modification** from JVET-N0458
 - Both method **won't introduce new context**
- Experimental results reportedly show
 - Method 1
 - AI: -0.63% (CTC), -0.12% (Class F), -0.43% (TGM)
 - RA: 0.01% (CTC), -0.12% (Class F), -0.18% (TGM)
 - Method 2
 - AI: -0.64% (CTC), -0.26% (Class F), -0.74% (TGM)
 - RA: 0.02% (CTC), -0.20% (Class F), -0.41% (TGM)
- Based on the above results, it is suggested to adopt the modification into VVC

THANKS !

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