

JVET-N0078

CE2-5.6: Simplifications for inherited affine merging candidates at CTU row boundaries

- Authors:

MediaTek:

Yu-Ling Hsiao, Tzu-Der Chuang, Chih-Wei Hsu,
Ching-Yeh Chen, Yu-Wen Huang, Shaw-Min Lei

Bytedance:

Kai Zhang, Li Zhang, Hongbin Liu, Jizheng Xu

- Presneter: Chih-Wei Hsu

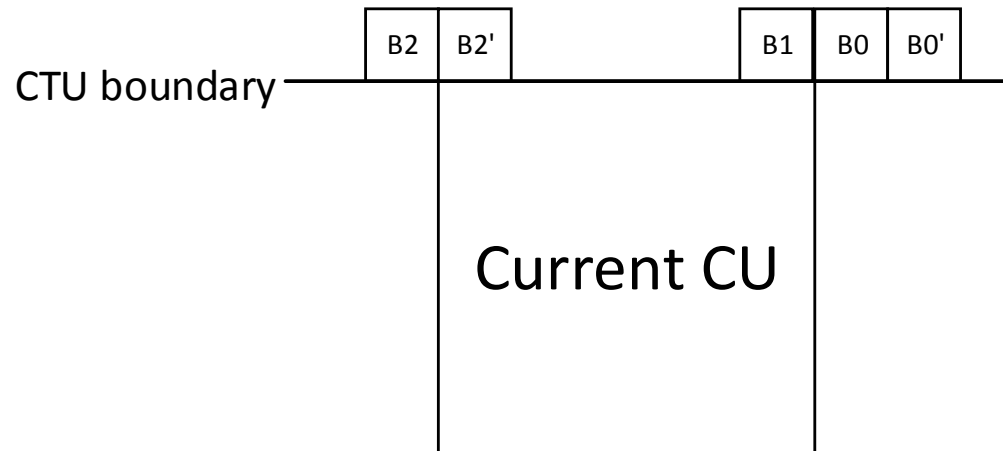
Overall Summary

- Simplifications for inherited affine candidates at CTU row boundaries
 - CU width and x position information line buffer can be removed
 - Use two subblock MVs with a fixed distance for affine inheritance

Over VTM-4.0 (%)		Y	U	V	EncT	DecT	
1	Fixed distance equal to 4 (CE2.5.6.a)	RA	0.02	-0.05	-0.04	100%	100%
		LB	0.01	-0.12	0.03	99%	101%
2	Fixed distance equal to 8 (CE2.5.6.b)	RA	0.00	-0.08	0.04	100%	100%
		LB	0.02	-0.02	0.10	100%	99%
3	Fixed distance equal to 16 (CE2.5.6.c)	RA	0.00	-0.04	-0.01	100%	99%
		LB	-0.02	0.03	-0.25	100%	101%

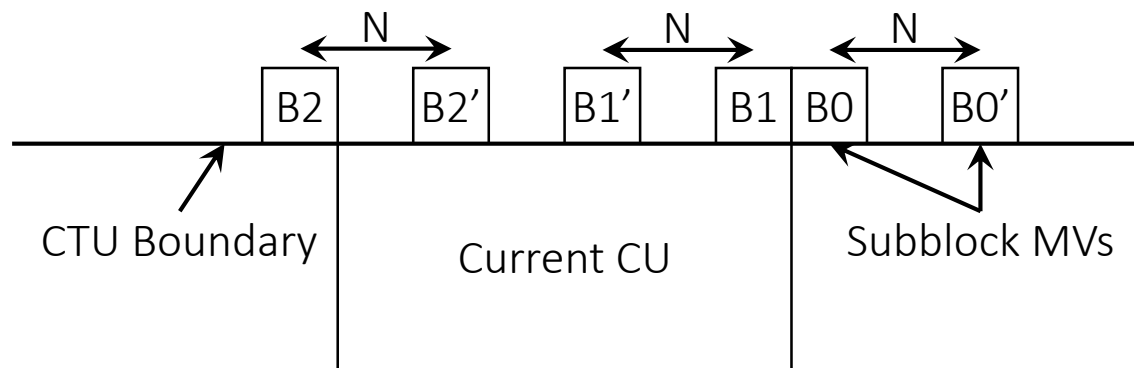
Proposed Methods (1/2) (CE2.5.6.a)

- **Two subblock MVs** with a fixed distance for affine inheritance at CTU row boundaries
 - B0 and B0', B1 and B0, and B2 and B2' are used for deriving 4-parameter inherited affine candidates
 - Distance between blocks is 4
 - CU width and x position information line buffer is not needed



Proposed Methods (2/2) (CE2.5.6.b and c)

- **Two subblock MVs** with a fixed distance for affine inheritance at CTU row boundaries
 - B0 and B0', B1 and B1', and B2 and B2' are used for deriving 4-parameter inherited affine candidates
 - Distance between blocks is N (8 or 16)
 - CU width and x position information line buffer is not needed



Simulation Results (1/3)

Fixed distance equal to 4 (CE2.5.6.a)

	Random access Main10				
	Over VTM-4.0				
	Y	U	V	EncT	DecT
Class A1	0.03%	-0.11%	0.06%	100%	101%
Class A2	0.01%	0.00%	0.03%	100%	101%
Class B	0.01%	-0.03%	-0.08%	99%	100%
Class C	0.02%	-0.06%	-0.12%	99%	99%
Class E					
Overall	0.02%	-0.05%	-0.04%	100%	100%
Class D	0.00%	-0.10%	-0.05%	99%	95%
Class F	0.01%	0.05%	0.02%	99%	100%

	Low delay B Main10				
	Over VTM-4.0				
	Y	U	V	EncT	DecT
Class A1					
Class A2					
Class B	0.02%	-0.37%	0.12%	98%	101%
Class C	-0.01%	0.23%	-0.01%	100%	101%
Class E	0.02%	-0.17%	-0.09%	100%	100%
Overall	0.01%	-0.12%	0.03%	99%	101%
Class D	-0.01%	-0.13%	-0.19%	100%	103%
Class F	-0.17%	-0.15%	0.31%	100%	103%

Simulation Results (2/3)

Fixed distance equal to 8 (CE2.5.6.b)

	Random access Main10				
	Over VTM-4.0				
	Y	U	V	EncT	DecT
Class A1	0.02%	-0.09%	0.09%	100%	101%
Class A2	0.00%	-0.11%	0.06%	100%	99%
Class B	0.00%	-0.06%	0.08%	100%	99%
Class C	0.00%	-0.09%	-0.08%	99%	100%
Class E					
Overall	0.00%	-0.08%	0.04%	100%	100%
Class D	0.01%	0.03%	-0.06%	100%	100%
Class F	0.00%	0.03%	0.01%	100%	99%

	Low delay B Main10				
	Over VTM-4.0				
	Y	U	V	EncT	DecT
Class A1					
Class A2					
Class B	0.01%	-0.11%	0.17%	100%	100%
Class C	-0.01%	0.11%	0.00%	100%	100%
Class E	0.06%	-0.03%	0.12%	100%	96%
Overall	0.02%	-0.02%	0.10%	100%	99%
Class D	0.03%	0.29%	-0.29%	101%	101%
Class F	-0.10%	0.01%	-0.28%	100%	99%

Simulation Results (3/3)

Fixed distance equal to 16 (CE2.5.6.c)

	Random access Main10				
	Over VTM-4.0				
	Y	U	V	EncT	DecT
Class A1	0.02%	-0.04%	0.07%	100%	100%
Class A2	-0.02%	-0.02%	0.00%	100%	98%
Class B	-0.01%	-0.07%	-0.05%	100%	100%
Class C	0.02%	0.00%	-0.03%	99%	99%
Class E					
Overall	0.00%	-0.04%	-0.01%	100%	99%
Class D	0.00%	0.00%	0.01%	100%	100%
Class F	0.00%	0.05%	-0.02%	100%	98%

	Low delay B Main10				
	Over VTM-4.0				
	Y	U	V	EncT	DecT
Class A1					
Class A2					
Class B	0.01%	0.15%	-0.33%	100%	102%
Class C	-0.02%	-0.13%	-0.06%	100%	100%
Class E	-0.06%	0.07%	-0.37%	100%	99%
Overall	-0.02%	0.03%	-0.25%	100%	101%
Class D	0.01%	-0.14%	0.18%	101%	101%
Class F	-0.09%	-0.33%	0.00%	100%	100%

Conclusions

- Proposed to simplify inherited affine candidates at CTU row boundaries
- Coding efficiency impact is minor
- No additional buffer is needed in addition to the subblock MVs buffer (shared with non-affine mode)
- Thanks Foxconn and Qualcomm for cross-checking