MEDIATEK

CE1.6.1: Coding large size CUs (JVET-K0227)

Shih-Ta Hsiang, ChingYeh Chen, Chen-Yen Lai, Yu-Wen Huang, Shawmin Lei

Presented by Shih-Ta Hsiang

Overall Summary

- This contribution reports the results of CE1.6.1.1 and CE1.6.1.2 for handling a coding unit (CU) of width or height larger than the maximum transform size
  - In CE1.6.1.1, the CU is inferred to be further partitioned by a quadtree split when the width or height of the current CU is larger than the maximum transform size.
  - In CE1.6.1.2, the CU is inferred to have zero residual in a B or P slice when the width or height of the current CU is larger than the maximum transform size.
  - For both methods, each CU always contains one transform unit (TU) and extra implementation to process the CUs containing more than one TU is not needed.
- Average luma BD-rates under the VTM-1.0 CTCs
  - CE1.6.1.1 : -0.01%, 0.90%, and 0.64% for the AI, RA, and LB settings
  - CE1.6.1.2 : -0.01%, 0.07%, and 0.02% for the AI, RA, and LB settings

Problem in VVC-1.0

- When both width and height of the current CU is less than or equal to the maximum transform size, the resulting CU partition is also employed for prediction and transform processing
  - Each CU only contains exactly one prediction unit (PU) and one TU
- When the width or height of the current CU is larger than the maximum transform size, the CU is inferred to be further partitioned into multiple TUs by tiling with the maximum transform blocks
  - Needs extra implementation to process the CUs containing more than one TU

Proposed Method in CE1.6.1.1

- When the width or height of the current CU is larger than the maximum transform size, the current CU is inferred to be further partitioned by quadtree split without explicitly signaling.
- The maximum allowed CU size is equal to the maximum allowed transform block size

Proposed Method in CE1.6.1.2

- When the width or height of the current CU is larger than the maximum transform size in a B or P slice, the current CU is inferred to have zero residual
  - The CU is inferred to be coded in either skip mode or AMVP mode.
  - The syntax element pred_mode_flag is inferred to be equal to 0 without explicitly signaling.
  - The syntax element merge_flag is inferred to be equal to 0 without explicitly signaling after the syntax element cu_skip_flag is signaled to be equal to 0.
  - The maximum allowed CU size is equal to the CTU size.
- When the width or height of the current CU is larger than the maximum transform size in an I slice, the current CU is inferred to be further partitioned by quadtree split.

Simulation Results for CE1.6.1.1

	All Intra Main10									
	Over VTM-1.0					Over BMS-1.0				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	-0.02%	-0.05%	0.01%	101%	100%	-0.02%	0.00%	0.00%	101%	100%
Class A2	-0.01%	0.00%	0.03%	101%	100%	0.00%	-0.04%	-0.06%	100%	100%
Class B	-0.01%	-0.02%	-0.02%	100%	99%	-0.01%	0.06%	0.09%	100%	100%
Class C	0.01%	-0.02%	-0.06%	100%	100%	0.00%	0.07%	0.08%	100%	100%
Class E	-0.01%	-0.05%	0.02%	100%	99%	-0.03%	0.04%	-0.17%	100%	100%
Overall	-0.01%	-0.03%	-0.01%	100%	100%	-0.01%	0.03%	0.00%	100%	100%
Class D	0.00%	0.02%	-0.01%	100%	98%	-0.01%	0.08%	0.05%	100%	101%
Class F (optional)	0.00%	-0.01%	-0.01%	101%	100%	-0.02%	-0.05%	-0.22%	100%	100%

	Random Access Main 10									
	Over VTM-1.0					Over BMS-1.0				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	1.99%	1.88%	2.03%	71%	102%	1.93%	1.87%	2.10%	74%	99%
Class A2	1.27%	1.04%	1.11%	73%	101%	1.78%	1.38%	1.42%	79%	99%
Class B	0.71%	0.63%	0.54%	76%	101%	0.95%	0.88%	0.86%	82%	100%
Class C	0.02%	0.06%	0.02%	85%	100%	0.15%	0.33%	-0.11%	88%	99%
Class E										
Overall	0.90%	0.81%	0.81%	77%	101%	1.10%	1.03%	0.96%	81%	99%
Class D	-0.01%	0.05%	-0.04%	87%	100%	0.05%	0.19%	-0.20%	90%	99%
Class F (optional)	0.20%	0.31%	0.47%	82%	102%	0.30%	0.25%	0.17%	87%	102%

	Low delay B Main10									
	Over VTM-1.0					Over BMS-1.0				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1										
Class A2										
Class B	0.43%	0.42%	0.45%	79%	101%	0.76%	0.65%	0.77%	80%	100%
Class C	0.05%	-0.01%	0.14%	87%	98%	0.11%	0.09%	0.04%	88%	99%
Class E	1.78%	1.96%	1.28%	73%	101%	2.19%	2.42%	2.28%	73%	99%
Overall	0.64%	0.66%	0.55%	80%	100%	0.90%	0.91%	0.90%	80%	99%
Class D	-0.05%	0.07%	-0.18%	88%	99%	0.09%	0.32%	0.14%	88%	99%
Class F (optional)	-0.08%	-0.10%	-0.13%	84%	102%	0.22%	0.09%	0.25%	84%	101%

Simulation Results for CE1.6.1.2

	All Intra Main10									
	Over VTM-1.0					Over BMS-1.0				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	-0.02%	-0.05%	0.01%	101%	100%	-0.02%	0.00%	0.00%	101%	100%
Class A2	-0.01%	0.00%	0.03%	101%	100%	0.00%	-0.04%	-0.06%	100%	100%
Class B	-0.01%	-0.02%	-0.02%	100%	99%	-0.01%	0.06%	0.09%	100%	100%
Class C	0.01%	-0.02%	-0.06%	100%	100%	0.00%	0.07%	0.08%	100%	100%
Class E	-0.01%	-0.05%	0.02%	100%	99%	-0.03%	0.04%	-0.17%	100%	100%
Overall	-0.01%	-0.03%	-0.01%	100%	100%	-0.01%	0.03%	0.00%	100%	100%
Class D	0.00%	0.02%	-0.01%	100%	98%	-0.01%	0.08%	0.05%	100%	101%
Class F (optional)	0.00%	-0.01%	-0.01%	101%	100%	-0.02%	-0.05%	-0.22%	100%	100%

	Random Access Main 10									
	Over VTM-1.0					Over BMS-1.0				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	0.23%	0.47%	0.53%	95%	100%	0.41%	0.44%	0.69%	98%	98%
Class A2	0.04%	0.01%	0.13%	95%	100%	0.13%	0.02%	0.15%	98%	100%
Class B	0.05%	0.20%	0.06%	95%	98%	0.08%	0.14%	0.15%	98%	99%
Class C	0.00%	0.00%	-0.01%	97%	99%	0.06%	0.09%	-0.20%	99%	99%
Class E										
Overall	0.07%	0.16%	0.15%	96%	99%	0.15%	0.16%	0.16%	98%	99%
Class D	0.01%	-0.01%	-0.02%	97%	101%	0.08%	-0.06%	-0.27%	99%	100%
Class F (optional)	0.02%	0.07%	0.22%	94%	99%	0.01%	0.01%	-0.08%	98%	100%

	Low delay B Main10									
	Over VTM-1.0					Over BMS-1.0				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1										
Class A2										
Class B	0.04%	0.33%	0.18%	95%	100%	0.07%	0.07%	0.49%	98%	99%
Class C	0.04%	-0.07%	0.13%	96%	99%	-0.01%	0.01%	-0.04%	98%	100%
Class E	-0.03%	0.38%	-0.27%	92%	98%	-0.36%	0.55%	0.18%	96%	100%
Overall	0.02%	0.21%	0.05%	95%	99%	-0.06%	0.17%	0.24%	98%	100%
Class D	0.00%	0.17%	-0.43%	97%	99%	0.03%	0.39%	-0.11%	98%	100%
Class F (optional)	-0.08%	-0.27%	0.51%	93%	99%	0.19%	0.51%	0.32%	97%	99%

Conclusions

- Experimental results show that the proposed method in CE1.6.1.1 can speed up encoding run time substantially while suffering some performance loss in compression efficiency.
- Experimental results show that the proposed method in CE1.6.1.2 exhibit no significant loss in compression efficiency while slightly improving performance in encoding run time under the Random Access and Low Delay B settings.
- Both methods do not need to handle CUs containing more than one TU.



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Results for coding large CUs in skip mode (BMS tools off)

	Random Access Main 10									
	Over VTM-1.0					Over BMS-1.0				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	1.28%	1.04%	1.30%	78%	100%	21.64%	48.24%	51.27%	20%	39%
Class A2	0.88%	0.56%	0.57%	79%	102%	25.47%	29.65%	20.86%	24%	38%
Class B	0.52%	0.31%	0.24%	82%	104%	19.07%	29.85%	32.27%	22%	45%
Class C	0.07%	-0.01%	0.06%	90%	99%	14.92%	20.25%	24.10%	23%	48%
Class E										
Overall	0.62%	0.42%	0.47%	83%	102%	19.76%	30.93%	31.61%	22%	43%
Class D	0.06%	0.14%	-0.03%	92%	99%	15.92%	18.05%	20.31%	22%	47%
Class F (optional)	0.13%	0.19%	0.32%	81%	99%	12.71%	20.77%	20.81%	18%	58%

	Low delay B Main10									
	Over VTM-1.0					Over BMS-1.0				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1										
Class A2										
Class B	0.31%	0.21%	0.22%	85%	100%	12.45%	12.02%	13.07%	23%	50%
Class C	0.08%	-0.09%	0.18%	91%	98%	10.26%	9.45%	10.87%	27%	58%
Class E	0.30%	0.49%	0.00%	75%	98%	13.04%	11.10%	13.84%	22%	56%
Overall	0.23%	0.18%	0.15%	84%	99%	11.87%	10.93%	12.53%	24%	54%
Class D	-0.04%	-0.13%	-0.06%	92%	99%	12.41%	10.14%	10.75%	31%	60%
Class F (optional)	-0.01%	-0.17%	0.77%	79%	98%	12.12%	15.86%	16.57%	21%	64%

Results for coding large CUs in the skip mode for non-lowdelay Inter slices, and in the skip or AMVP mode for lowdelay inter slices (BMS tools off)

	Random Access Main 10									
	Over VTM-1.0					Over BMS-1.0				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	1.23%	1.02%	1.17%	81%	102%	21.59%	48.27%	51.10%	21%	39%
Class A2	0.85%	0.52%	0.60%	82%	101%	25.44%	29.60%	20.90%	24%	38%
Class B	0.51%	0.30%	0.24%	83%	99%	19.06%	29.85%	32.26%	22%	43%
Class C	0.06%	0.01%	0.02%	90%	99%	14.91%	20.26%	24.04%	23%	48%
Class E										
Overall	0.60%	0.41%	0.44%	84%	100%	19.73%	30.93%	31.56%	22%	42%
Class D	0.04%	0.04%	-0.01%	92%	100%	15.90%	17.95%	20.30%	22%	47%
Class F (optional)	0.12%	0.17%	0.30%	82%	99%	12.71%	20.74%	20.78%	18%	58%

	Low delay B Main10									
	Over VTM-1.0					Over BMS-1.0				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1										
Class A2										
Class B	0.04%	0.33%	0.18%	95%	100%	12.15%	12.17%	13.03%	26%	50%
Class C	0.04%	-0.07%	0.13%	97%	98%	10.22%	9.44%	10.83%	28%	58%
Class E	-0.03%	0.38%	-0.27%	92%	99%	12.69%	10.93%	13.56%	27%	57%
Overall	0.02%	0.21%	0.05%	95%	99%	11.64%	10.95%	12.43%	27%	54%
Class D	0.00%	0.17%	-0.43%	97%	99%	12.47%	10.49%	10.30%	32%	60%
Class F (optional)	-0.08%	-0.27%	0.51%	93%	99%	12.03%	15.70%	16.65%	24%	64%