

JVET-K0130

CE6-related: Type4 only AMT

K. Abe, T. Toma

Panasonic Corporation

- AMT provides interesting gains, but the impact on the hardware is significant.

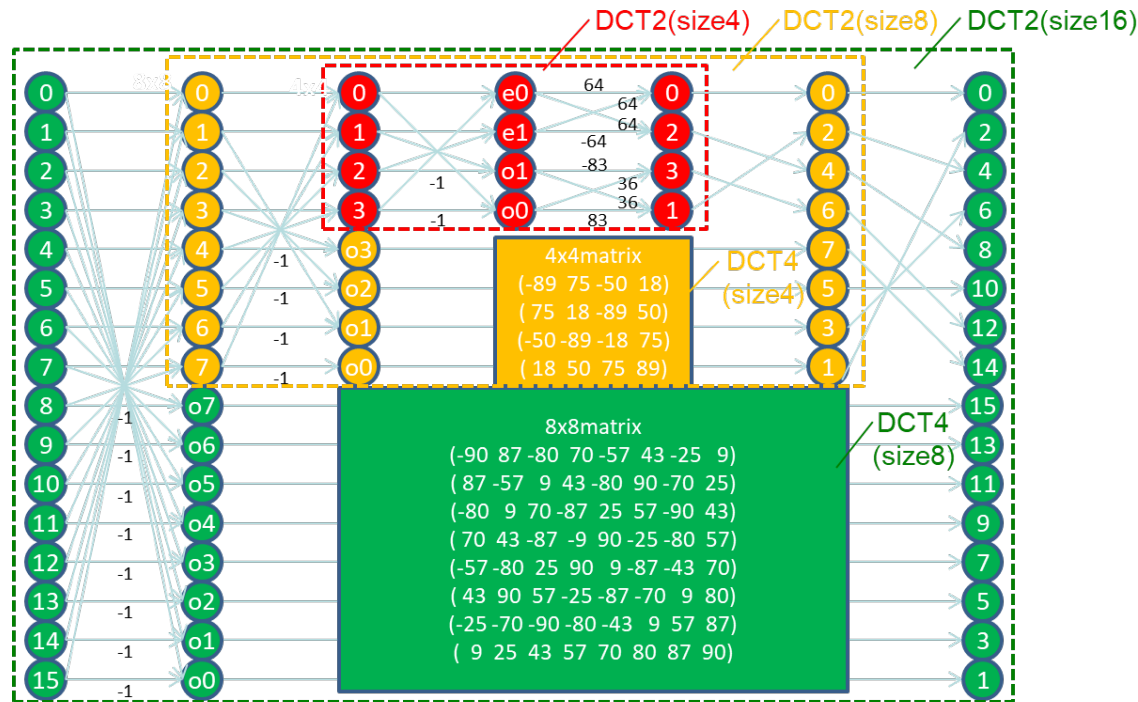
Gain : 3.5% for AI, 2.2% for RA (VTM configuration)

Circuit : DCT2 partial butterfly + DCT5/DCT8/DST1/DST7 x num of trans size

➡ We propose a new AMT without additional circuit from DCT2.

Background

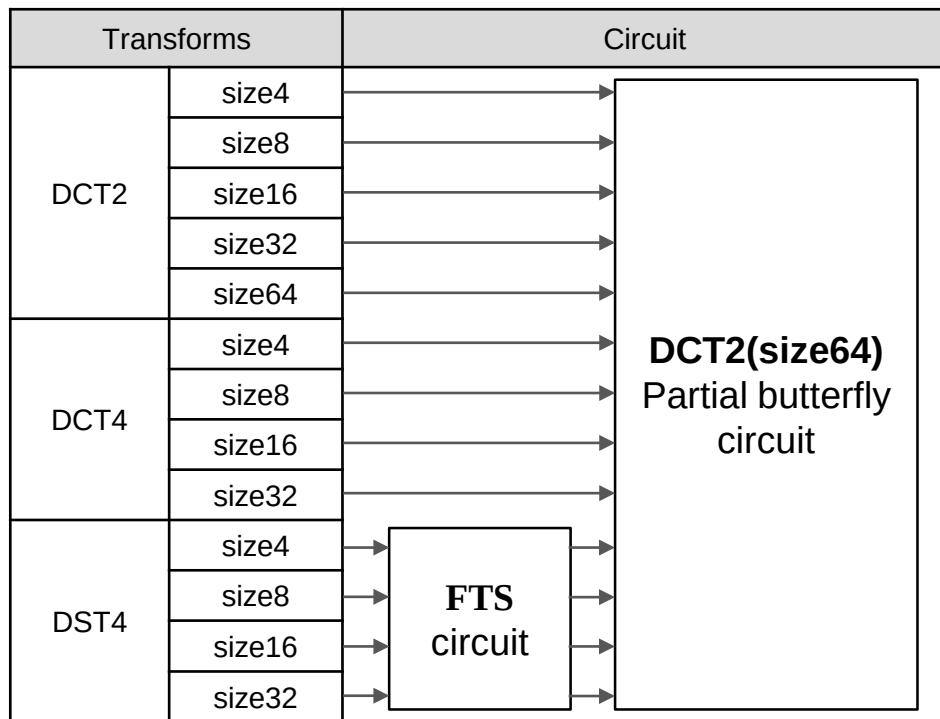
■ Analysis of HEVC DCT2 partial butterfly circuit (It is common for VVC)



The partial butterfly circuit of DCT2(size16) includes DCT2(size4/8) and DCT4(size4/8). This relationship also applies to size32 or size64.

Background

■ Capability of reusing a DCT2 partial butterfly circuit



DST4 = F T S

DCT4 (blue line to T)

flipping (red line to F)

sign changing (red line to S)

where

$$\mathbf{F}_{m,n} = \begin{cases} 1, & \text{if } n = N - 1 - m, \\ 0, & \text{otherwise,} \end{cases}$$
$$\mathbf{S}_{m,n} = \begin{cases} (-1)^m, & \text{if } n = m, \\ 0, & \text{otherwise.} \end{cases}$$

Proposed method

The proposed method is based on the existing AMT with the following two restrictions:

(restriction1) Only DCT4 and DST4 can be selected as AMT for both intra and inter CU.

(restriction2) The maximum AMT size is limited to 32.

amt_flag	amt_idx		Luma				Chroma	
			size > 32		size <= 32			
	hor	ver	hor	ver	hor	ver	hor	ver
0	—	—	DCT2	DCT2	DCT2	DCT2	DCT2	DCT2
1	0	0	—	—	DST4	DST4		
	0	1	—	—	DST4	DCT4		
	1	0	—	—	DCT4	DST4		
	1	1	—	—	DCT4	DCT4		

Note : Signaling of the syntax is skipped when it is not needed.
AMT core selection does not depend on intra directions.

Simulation results

Anchor : VTM configuration (BMS-1.1 software)

Test1 : Enable proposed AMT, Test2 : Enable conventional AMT (implemented in BMS)

(Test1)	All Intra Main10					Random Access Main 10					Low delay B Main10				
	Over VTM-1.1 (proposed AMT)					Over VTM-1.1 (proposed AMT)					Over VTM-1.1 (proposed AMT)				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	-2.57%	-0.69%	-0.60%	204%	120%	-1.19%	0.16%	0.20%	148%	107%					
Class A2	-2.59%	-1.28%	-1.30%	212%	117%	-1.42%	0.37%	0.62%	141%	106%					
Class B	-2.78%	-1.46%	-1.34%	218%	118%	-1.97%	-0.21%	-0.42%	148%	104%	-1.65%	0.71%	0.49%	149%	109%
Class C	-3.06%	-1.47%	-1.70%	227%	111%	-2.02%	-0.26%	-0.42%	155%	101%	-1.51%	0.41%	0.65%	151%	105%
Class E	-3.93%	-3.01%	-2.83%	201%	115%						-0.92%	1.09%	1.64%	130%	104%
Overall	-2.97%	-1.56%	-1.54%	214%	116%	-1.72%	-0.03%	-0.09%	149%	104%	-1.42%	0.71%	0.83%	145%	106%
Class D	-3.03%	-1.25%	-1.32%	239%	108%	-1.97%	-0.01%	-0.52%	155%	97%	-1.46%	0.39%	0.51%	146%	104%
Class F	-1.68%	-1.12%	-1.16%	214%	107%	-1.37%	-0.39%	-0.46%	162%	100%	-1.13%	-0.19%	0.31%	151%	102%

(Test2)	Over VTM-1.1 (conventional AMT)					Over VTM-1.1 (conventional AMT)					Over VTM-1.1 (conventional AMT)				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	-3.29%	-1.32%	-1.22%	204%	129%	-1.91%	0.08%	0.15%	174%	114%					
Class A2	-3.16%	-1.65%	-1.43%	210%	121%	-2.05%	0.14%	0.47%	159%	108%					
Class B	-3.46%	-1.44%	-1.42%	216%	124%	-2.49%	-0.27%	-0.58%	165%	108%	-1.92%	0.83%	0.37%	170%	113%
Class C	-3.12%	-0.90%	-1.16%	224%	113%	-2.06%	0.03%	-0.20%	170%	103%	-1.30%	0.95%	0.93%	165%	107%
Class E	-4.40%	-2.74%	-2.65%	198%	121%						-1.34%	2.05%	1.92%	153%	105%
Overall	-3.46%	-1.55%	-1.53%	211%	121%	-2.17%	-0.04%	-0.12%	167%	108%	-1.57%	1.18%	0.94%	164%	109%
Class D	-3.00%	-0.66%	-0.74%	233%	110%	-1.82%	0.51%	-0.15%	166%	103%	-1.24%	0.71%	0.86%	154%	105%
Class F	-1.88%	-0.83%	-0.89%	210%	110%	-1.57%	-0.34%	-0.41%	180%	106%	-1.04%	0.10%	0.20%	171%	106%

Simulation results

Anchor : BMS configuration (BMS-1.1 software)

Test : Enable proposed AMT

	All Intra Main10					Random Access Main 10					Low delay B Main10				
	Over BMS-1.1 (proposed AMT)					Over BMS-1.1 (proposed AMT)					Over BMS-1.1 (proposed AMT)				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	0.70%	1.30%	1.12%	99%	96%	0.69%	0.89%	0.75%	84%	97%					
Class A2	0.56%	0.75%	0.35%	99%	96%	0.59%	0.87%	0.43%	90%	98%					
Class B	0.58%	0.49%	0.53%	100%	97%	0.41%	0.54%	0.47%	90%	99%	0.15%	-0.07%	-0.13%	90%	97%
Class C	0.03%	-0.12%	-0.12%	101%	99%	-0.02%	0.00%	-0.11%	93%	99%	-0.30%	-0.29%	-0.56%	93%	100%
Class E	0.34%	0.12%	0.02%	100%	97%						-0.01%	0.10%	0.81%	91%	98%
Overall	0.44%	0.47%	0.37%	100%	97%	0.39%	0.53%	0.36%	90%	99%	-0.04%	-0.10%	-0.04%	91%	98%
Class D	0.00%	-0.20%	-0.31%	101%	100%	-0.14%	-0.07%	-0.12%	95%	98%	-0.27%	-0.54%	-0.34%	96%	101%
Class F	0.16%	-0.05%	-0.16%	101%	99%	0.12%	-0.20%	-0.09%	93%	98%	-0.19%	0.10%	-0.50%	90%	98%

Additional information

■ Problem

Proposed AMT disables size64 AMT (restriction 2).

It may lead to some performance loss when the picture size is increased.

■ Simulation results

Anchor : VTM configuration (BMS-1.1 software)

Test : Enable proposed AMT + size64 DST4 / DCT4

	All Intra Main10					Random Access Main 10					Low delay B Main10				
	Over BMS-1.1 (proposed AMT + size64AMT)					Over BMS-1.1 (proposed AMT + size64AMT)					Over BMS-1.1 (proposed AMT + size64AMT)				
	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT	Y	U	V	EncT	DecT
Class A1	-2.60%	-0.86%	-0.75%	206%	121%	-1.47%	0.12%	0.18%	176%	111%					
Class A2	-2.61%	-1.30%	-1.35%	213%	117%	-1.53%	0.52%	0.71%	160%	107%					
Class B	-2.79%	-1.52%	-1.44%	220%	120%	-2.07%	-0.27%	-0.39%	167%	106%	-1.86%	0.61%	0.71%	173%	111%
Class C	-3.06%	-1.50%	-1.64%	229%	112%	-2.06%	-0.24%	-0.41%	172%	103%	-1.58%	0.58%	0.53%	166%	107%
Class E	-3.94%	-3.04%	-3.05%	202%	117%						-1.11%	0.64%	1.00%	154%	106%
Overall	-2.98%	-1.62%	-1.62%	215%	117%	-1.84%	-0.03%	-0.06%	169%	106%	-1.58%	0.60%	0.72%	166%	108%
Class D	-3.03%	-1.23%	-1.30%	238%	110%	-1.98%	-0.04%	-0.45%	168%	105%	-1.49%	-0.05%	0.50%	155%	104%
Class F	-1.67%	-1.07%	-1.12%	213%	108%	-1.41%	-0.48%	-0.49%	182%	105%	-1.13%	-0.03%	0.16%	172%	105%

➡ Size64 AMT obtains some gains for Class A and B, but the trade-off gain vs hardware impact is not interesting enough.

Conclusions

- The proposed AMT is based on the existing AMT with the following modifications:
 - DCT4 and DST4 can be selected as AMT for both intra and inter CU.
 - The maximum AMT size is limited to 32 (half of the maximum DCT2).
- 2.97%, 1.72%, 1.42% gain for AI, RA, LDB for VTM.

➡ It is proposed to adopt into test model.

1. It requires only DCT2 partial butterfly circuit.
 - Can be realized by HEVC based HW architecture.
2. Transform core selection algorithm is also simplified.
 - Good for basis for further gain improvement.

Thank KDDI for cross-checking of the proposal test.