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Title: Clocking in the audiovisual communication systems
Purpose: Discussion

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1. Introduction

This document tries to give some analysis regarding the clocking of the audiovisual communication systems in different network environments which was raised in D.846 (WP1/15) by France Telecom at the last Working Party 1/15 meeting (AVC-1005 [1] of this meeting). Point-to-point and multipoint cases are discussed.

2. System model

Figure 1 enumerates all the possible clock sources in a point-to-point audiovisual communication. One or more of them may be independent, while others may be slaved to an independent clock.

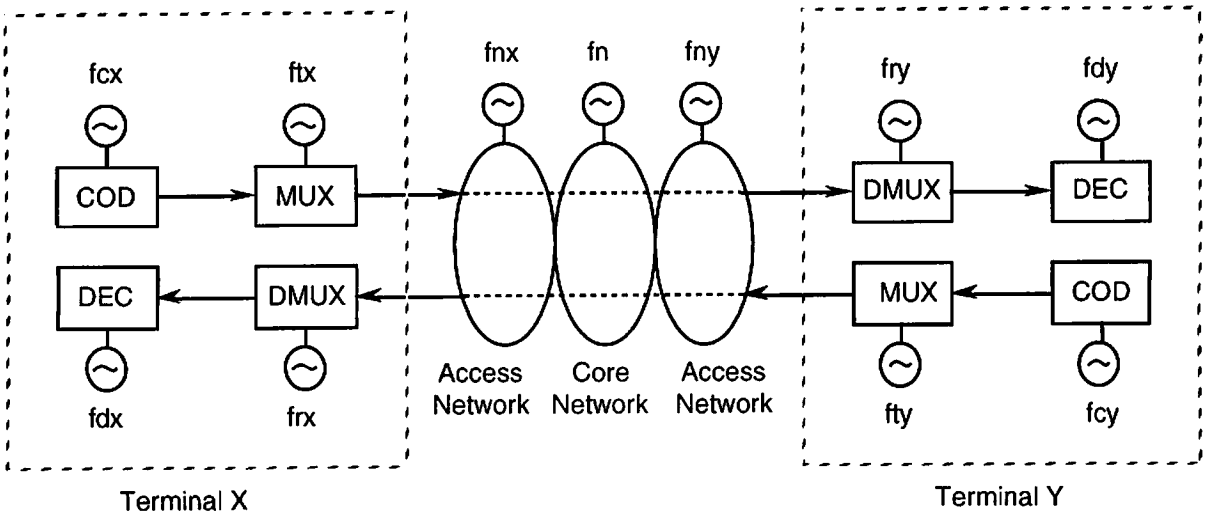

Figure 1 System model focusing on different clock sources

Table 1 Definition

Clock	Definition	Example
fcx	encoder clock (sampling frequency) of Terminal X	8 kHz sampling frequency for the G.711 encoder
fdx	decoder clock of Terminal X	8 kHz for the G.711 decoder
ftx	transmission clock for the multiplexed stream of Terminal X	64 kbit/s for the H.221 multiplexed stream
frx	receiving clock of the demultiplexer of Terminal X	64 kbit/s for the H.221 multiplexed stream
fnx	network clock of the access network accommodating Terminal X	- 10 Mbit/s for the Ethernet - 155.52 Mbit/s (2430 x 64 kbit/s) for ATM
fn	network clock of the core network	multiple of 8 kHz, very stable Cesium based for the public network
fny	network clock of the access network accommodating Terminal Y	- 10 Mbit/s for the Ethernet - 25.6 Mbit/s for ATM25
fry	receiving clock of the demultiplexer of Terminal Y	64 kbit/s for the H.221 multiplexed stream
fdy	decoder clock of Terminal Y	8 kHz for the G.711 decoder
fcy	encoder clock (sampling frequency) of Terminal Y	8 kHz sampling frequency for the G.711 encoder
fty	transmission clock for the multiplexed stream of Terminal Y	64 kbit/s for the H.221 multiplexed stream

3. Case studies

The following three cases are listed in Table 2:

- H.320 on N-ISDN
- H.323 on non guaranteed QoS LAN (Ethernet)
- H.310 native (H.262/H.222.1) mode on B-ISDN

Table 2 Some examples

Clock	H.320 on N-ISDN H.322 on GQoS LAN	H.323 on NGQoS-LAN (Ethernet), point-to-point inside a LAN	H.310 native mode on B-ISDN
fcx	derived from frx, locked with fn	internal clock source independent of frx (Note 2)	internal clock source independent of frx
fdx	derived from frx, locked with fn	internal clock source independent of frx, fcx (Note 1)	locked with fcy
ftx	derived from frx, locked with fn	=fnx??	e.g. 6144 kbit/s (96x64 kbit/s), may or may not be derived from fnx
frx	derived from fnx=fn	=fnx??	locked with fty, e.g. by the adaptive clock method
fnx	locked with fn	10 Mbit/s, independent of fn	locked with fn
fn	a multiple of 8 kHz, very stable Cesium based	a multiple of 8 kHz, very stable Cesium based	a multiple of 8 kHz, very stable Cesium based
fny	locked with fn	10 Mbit/s, independent of fn, fnx	locked with fn
fry	derived from fny=fn	=fny?	locked with ftx, e.g. by the adaptive clock method
fdy	derived from fry, locked with fn	internal clock source independent of fry, fcy	locked with fcx
fcy	derived from fry, locked with fn	internal clock source independent of fry	internal clock source independent of fry, independent of fcx
fty	derived from fry, locked with fn	=fny?	e.g. 6144 kbit/s (96x64 kbit/s), may or may not be derived from fny

Note 1 - when communicating with the H.323/H.320 gateway, fdx should be locked with fcy ?
Note 2 - when communicating with the H.323/H.320 gateway, fcx should be derived from fdx ?

A basic clocking method is that the encoder has its own clock and the decoder has a clock slaved to the encoder clock. Audiovisual signals are reproduced with a constant delay.

Another basic clocking method is the decoder having its clock independent of the encoder clock. In this method, audiovisual signals are reproduced with a variable delay and slips (buffer overflow or underflow) may happen time to time, hence reproduced audio will contain some clicks or other noises. For video signals, picture dropping or repetition may take place due to the variable delay nature of the system.

NOTE - The decoding clock should be faster than the encoding clock, otherwise receiving buffer overflow may destroy pictures for a while.

An extreme case is H.320 on N-ISDN where every clock is locked with the network's 8 kHz based stable clock.

Another extreme case is H.323 where every clock is presumably independent,. Respective media signals are packetized, received in buffers and read out with clocks independent of the sending side clocks. How to cope with buffer overflows or underflows are left to implementation (?). When an H.323 terminal communicates with an H.320 terminal on N-ISDN, H.323 clocks need be synchronized with the N-ISDN network clock or can still be independent (?).

The H.310 native mode (use of H.222.1) corresponds to the first basic method mentioned above. There are two independent clocks; one is the source 27 MHz, the other is transmission clock such as 6.144 MHz. Both of them are reproduced at the receiving side; the former by PCR timestamps, the latter by e.g. the adaptive clock method.

4. Multipoint communications

H.231/H.243 multipoint communications assume an MCU where endpoints are connected in a star shape. Each connection between the MCU and an endpoint is equivalent to an H.320 point-to-point communication. All clocks are synchronized with the network clock so that mixed audio is served without interruption, otherwise bitstream switching may necessitate bit clock and H.221 framing resynchronization. This is the reason H.243 requires that "All terminals shall synchronize their outgoing transmissions to the bit rate incoming from the local MCU when they receive MCC from the MCU." in Section 5/H.243.

The now historical digital primary rate H.120/H.130/H.140 system (2 Mbit/s) assumed asynchronous networks as well as synchronous networks. In multipoint communications, all the transmission clocks have to be locked with the network clock (if one or more synchronous network terminals are participating) or the MCU internal clock. For this purpose, bit 8 in TS0 of odd frames is used; if it is set to zero, the sending clock must be locked with the receiving clock (from the network), otherwise the terminal can use its own transmitting clock. The MCU always set this indication bit to zero regardless of the networks involved so that all the terminal clocks are locked with a single clock. See Section 3.1/H.140 "Clock synchronisation".

In case of H.323 multipoint, is there any requirement for the clock synchronization? Or since it assumes packet based asynchronous environments, there is no such need even for multipoint communications?

In case of H.310 native mode multipoint, perhaps respective synchronizations of the transmission clock (e.g. 6.144 MHz) and the source 27 MHz clock may be necessary for audio mixing, video switching/mixing to achieve high quality reproduction. This point is yet to be confirmed.

5. Conclusion

This document intends to stimulate the study on the subject matter. Particularly the following awaits further study:

- Identification of independent and dependent clocks in Figure 1.
- If the independent clock strategy is applied, audiovisual quality degradation takes place due to clock slips. Do we need some guidelines to restrict it to a certain range?
- If the clock loopback strategy (e.g. fcx being derived from fdx) is applied, we will need an indication bit (actually this is a command) to switch between master clock and slave clock.

END

References

[1] AVC-1005 "Proposal for amendment of H.320, H.32x Draft Recommendations", France Telecom, May 1996