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DATA COMMUNICATION OVER THE TELEPHONE NETWORK

GENERAL DATA COMMUNICATIONS INTERFACE LAYER 1 SPECIFICATION

ITU-T Recommendation V.230

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation V.230 was published in Fascicle VIII.1 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation V.230

GENERAL DATA COMMUNICATIONS INTERFACE LAYER 1 SPECIFICATION

(Melbourne, 1988)

1 General

This Recommendation defines the layer 1 characteristics of a General Data Communications Interface (GDCI) between Data Circuit-Terminating Equipment (DCE) and/or Data Terminal Equipment (DTE). Applications include DTE-DCE interfaces, DCE-DCE interfaces, and possible DTE-DTE interfaces (see Figure 1/V.230). The interface specification is based on the ISDN basic user-network interface defined in Recommendation I.430. The differences between the GDCI and the ISDN basic user-network interface provide for the different wiring configurations expected for these interfaces, and they provide a means by which equipment conforming to V.230 can identify whether it has been connected to an interface operating according to V.230 or to an interface operating according to I.430. The characteristics of the GDCI have been chosen so that it is possible to design terminals which are compatible with both I.430 and V.230, and so that inadvertent connection of I.430 equipment to a V.230 passive bus or of GDCI equipment to an I.430 passive bus will not result in passive bus malfunction.

Note - DTE-DTE interfaces are not defined by CCITT.

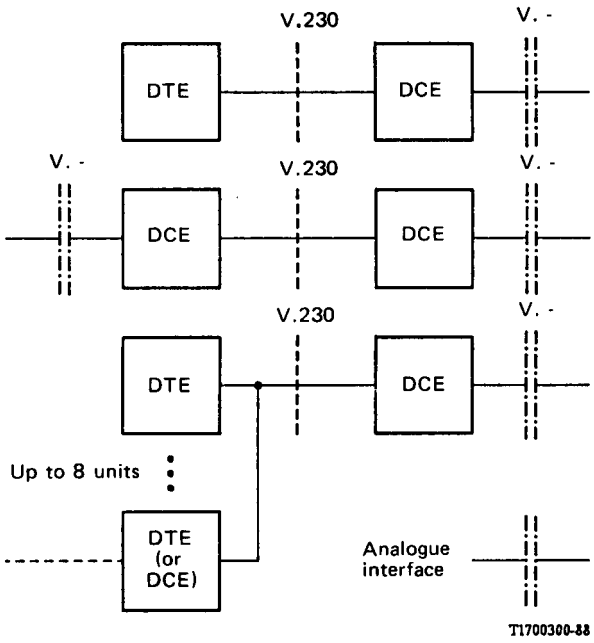


FIGURE 1/V.230

GDCI applications

2 Service characteristics

2.1 *Services required from the physical medium*

Layer 1 of this interface requires a balanced metallic transmission medium, for each direction of transmission, capable of supporting 192 kbit/s.

2.2 *Services provided to layer 2*

Layer 1 provides the following services to layer 2 and the management entity.

2.2.1 *Transmission capability*

Layer 1 provides the transmission capability, by means of appropriately encoded bit streams, for the BV and DV channels and the related timing and synchronization functions.

Note - The BV and DV channels correspond to the B and D channels, respectively, as defined in the I-Series Recommendations. Use of the BV and DV channels is defined in Recommendations V.yy and V.zz (V.yy and V.zz: still under study).

2.2.2 *Activation/deactivation*

Layer 1 provides the signalling capability and the necessary procedures to enable equipment to be deactivated when required and reactivated when required. The activation and deactivation procedures are defined in § 6.2.

2.2.3 *D-channel access*

Layer 1 provides the signalling capability and the necessary procedures to enable equipment to gain access to the common resource of the DV channel in an orderly fashion while meeting the performance requirements of the DV-channel signalling system. These DV-channel access control procedures are defined in § 6.1

2.2.4 *Maintenance*

Layer 1 provides the signalling capability, procedures and necessary functions at layer 1 to enable the maintenance functions to be performed.

2.2.5 *Status indication*

Layer 1 provides an indication to the higher layers of the status of layer 1.

2.3 *Primitives between layer 1 and other entities*

Primitives represent, in an abstract way, the logical exchange of information and control between layer 1 and other entities. They neither specify nor constrain the implementation of entities or interfaces.

The primitives to be passed across the layer 1/2 boundary or to the management entity and parameter values associated with these primitives are defined and summarized in Table 1/V.230. For a description of the syntax and use of the primitives, refer to Recommendation X.211 and relevant detailed description in § 6.

TABLE 1/V.230

Primitives associated with layer 1

Generic name	Specific name		Parameter		Message unit contents
	Request	Indication	Priority indicator	Message unit	
L1 < - - > L2					
PH-DATA	X (Note 1)	X	X (Note 2)	X	Layer 2 peer-to-peer message
PH-ACTIVATE	X	X	-	-	
PH-DEACTIVATE	X	X	-	-	
M < - - > L1					
MPH-ERROR	-	X*	-	X	*Type of error or recovery from a previously reported error
MPH-ACTIVATE	X	X	-	-	
MPH-DEACTIVATE	X	X	-	-	
MPH- INFORMATION	-	X	-	X	Connected Attached V-DCE Attached V-DTE Attached NT Attached TE Disconnected

Note 1 - PH-Data Request implies underlying negotiation between layer 1 and layer 2 for the acceptance of the data.

Note 2 - Priority indication applies only to the request type.

3 Modes of operation

Both point-to-point and point-to-multipoint modes of operation, as described below, are intended to be accommodated by the layer 1 characteristics of the GDCI. In this Recommendation, the modes of operation apply only to the layer 1 procedural characteristics of the interface and do not imply any constraints on modes of operation at higher layers.

3.1 *Point-to-point operation*

Point-to-point operation at layer 1 implies that only one source (transmitter) and one sink (receiver) are active at any one time in each direction of transmission at an S or T reference point. (Such operation is independent of the number of interfaces which may be provided on a particular wiring configuration - see § 4.)

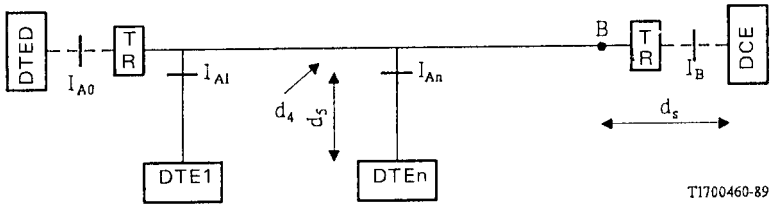
3.2 *Point-to-multipoint operation*

Point-to-multipoint operation at layer 1 allows more than one equipment (source and sink pair) to be simultaneously active at a GDCI. (The multipoint mode of operation may be accommodated, as discussed in § 4, with point-to-point or point-

to-multipoint wiring configurations.)

4 Types of wiring configuration

The electrical characteristics of the GDCI are determined on the basis of certain assumptions about the various wiring configurations which may exist in the user premises. These assumptions are identified in two major configuration descriptions, §§ 4.1 and 4.2, together with additional material contained in Annex A to this Recommendation. Figure 2/V.230 shows a general reference configuration for wiring in the user premises.



TR Terminating resistor

I Electrical interface

B Location of IB when the terminating resistor (TR) is include in the DCE

FIGURE 2/V.230

Reference configuration for wiring in the user premises location

4.1 *Point-to-point configuration*

A point-to-point wiring configuration implies that only one source (transmitter) and one sink (receiver) are interconnected on an interchange circuit.

4.2 *Point-to-multipoint configuration*

A point-to-multipoint wiring configuration allows more than one source to be connected to the same sink or more than one sink to be connected to the same source on an interchange circuit. Such distribution systems are characterized by the fact that they contain no active logic elements performing functions (other than possibly amplification or regeneration of the signal).

The equipment connected to interface point I_B must operate in the "master timing mode" discussed in § 6.6. This equipment is normally a V-DCE. The equipment connected to interface points I_{A0} through I_{An} must operate in the "slave timing mode". These are normally V-DTEs, although a V-DCE may be connected to this point to achieve a DCE-to-DCE connection on the GDCI. Use of a V-DTE as the master timing mode equipment is for further study.

4.3 *Wiring polarity integrity*

For a point-to-point wiring configuration, the two wires of the interchange circuit pair may be reversed. However, for a point-to-multipoint wiring configuration, the wiring polarity integrity of the interchange circuit (slave-to-master direction) must be maintained between slave mode equipment.

In addition, the wires of the optional pairs, which may be provided for powering, may not be reversed in either configuration.

4.4 *Location of the interfaces*

The wiring in the user premises is considered to be one continuous cable run with jacks for the equipment attached directly to the cable or using stubs less than 1 meter in length. The jacks are located at interface points I_A and I_B (see Figure 2/V.230). One interface point, I_A, is adjacent to the master mode equipment. The other interface point, I_B, is adjacent to the master mode equipment. However, in some applications, the equipment may be connected to the wiring without the use of a jack or with a jack which accommodates multiple interfaces. The required electrical characteristics (described in § 8) for I_A and I_B are different in some aspects.

4.5 *Wiring associated with the equipment*

The wiring connecting the V-DCE or V-DTE to associated jacks or to other equipment affects the interface electrical characteristics. Equipment that is not permanently connected to the interface wiring may be equipped with one of the following means of connection to the interface point:

- a hard wired connecting cord (of not more than 10 m in the case of a V-DTE and not more than 3 m in the case of a V-DCE) equipped with a suitable plug, or
- a jack with a connecting cord (of not more than 10 m in the case of a V-DTE and not more than 3 m in the case of a V-DCE) equipped with a suitable plug at each end, or
- two jacks with suitable connecting cords or cables which may be used to form a "daisy-chain" connection from one equipment unit to the next, provided that the connecting cords and cables meet the distance limitations set in Annex A. In this case, the electrical interface exists inside the equipment, where the two jacks are wired together with each pin on one jack connected to the like-numbered pin on the other jack and to the internal circuitry of the equipment.

The requirements of V.230 apply to the interface point (I_A or I_B), and the cord forms part of the associated equipment. Note that the equipment may attach directly to the interface wiring without a detachable cord.

Although an equipment may be provided with a cord of less than 5 m in length, it shall meet the requirements of this Recommendation with a cord having a minimum length of 5 m. As specified above, the equipment cord may be detachable. Such a cord may be provided as part of the equipment, or the equipment may be designed to conform to the electrical characteristics specified in § 8 with a "standard ISDN basic access TE cord" conforming to the requirements specified in § 8.9 of Recommendation I.430, and having the maximum permitted capacitance.

The use of an extension cord, of up to 25 m in length, with an equipment in point-to-point operation, is permitted. (The total attenuation of the wiring and of the cord in this case should not exceed 6 dB.)

5 Functional characteristics

The following paragraphs show the functions for the interface.

5.1 *Interface functions*

5.1.1 *BV channel*

This function provides, for each direction of transmission, two independent 64 kbit/s channels for use as BV channels.

5.1.2 *Bit timing*

This function provides bit (signal element) timing at 192 kbit/s to enable the equipment to recover information from the aggregate bit stream.

5.1.3 *Octet timing*

This function provides 8 kHz timing for the equipment.

5.1.4 *Frame alignment*

This function provides information to enable equipment to recover the time division multiplexed channels.

5.1.5 *DV channel*

This function provides, for each direction of transmission, one DV channel at a bit rate of 16 kbit/s.

5.1.6 *DV channel access procedure*

This function is specified to enable slave mode equipment to gain access to the common resource of the DV channel in an orderly controlled fashion. The functions necessary for these procedures include an echoed DV channel at a bit rate of 16 kbit/s in the direction master to slave equipment. For the definition of the procedures relating to DV channel access, see § 6.1.

5.1.7 *Power feeding*

This function provides for the capability to transfer power across the interface. The direction of power transfer depends on the application. In a typical application, it may be desirable to provide for power transfer from the V-DCE towards V-DTEs in order to, for example, power an adaptor for a unit which does not conform to V.230. (In some applications, unidirectional power feeding or no power feeding at all, across the interface, may apply.) Other Recommendations concerning power feeding capability are contained in § 9.

5.1.8 *Activation and deactivation*

Activation is necessary to initialize an equipment when power is applied, or when it is connected to the GDCI. Deactivation and activation may also be used to control entry to and exit from a low power consumption mode. The procedures and precise conditions under which these actions take place are specified in § 6.2. For many applications, it will be appropriate for the equipment to remain in the active state at all times after initial activation.

5.2 *Interchange circuits*

Two interchange circuits, one for each direction of transmission, shall be used to transfer digital signals across the interface. All of the functions described in § 5.1, except for power feeding, shall be carried by means of a digitally multiplexed signal structured as defined in § 5.4.

5.3 *Connected/disconnected indication*

The criterion used by equipment to determine whether it is connected or disconnected at the interface is reception of valid incoming frames.

The layer 1 entity within the equipment shall inform the management entity of the connection status using the MPH-INFORMATION INDICATION primitive. The method for determining the message unit contents is discussed in § 6.2.

5.4 *Frame structure*

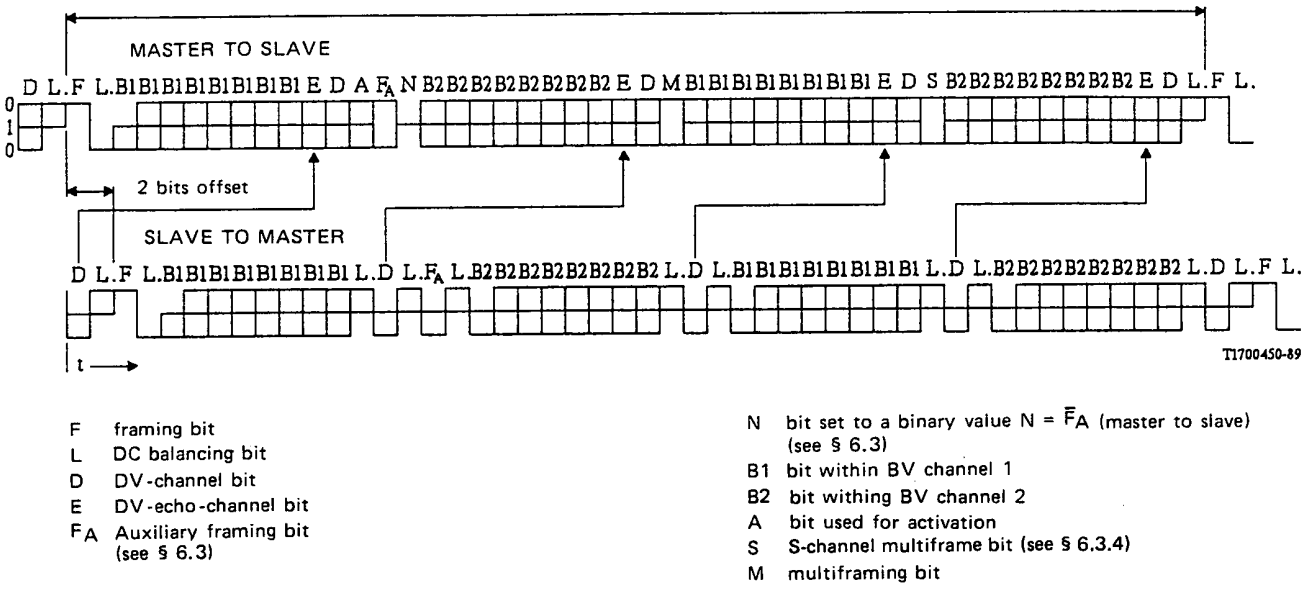
In both directions of transmission, the bits shall be grouped into frames of 48 bits each. The frame structure shall be identical for all configurations (point-to-point and point-to-multipoint).

5.4.1 *Bit rate*

The nominal transmitted bit rate at the interfaces shall be 192 kbit/s in both directions of transmission.

5.4.2 *Binary organization of the frame*

The frame structures are different for each direction of transmission. Both structures are illustrated diagramatically in Figure 3/V.230.



Note 1 - Dots demarcate those parts of the frame that are independently DC-balanced.

Note 2 - The F_A bit in the direction slave to master is used as a Q bit in every fifth frame if the Q channel capability is applied (see § 6.3.3).

Note 3 - The nominal 2-bit offset is as seen from the slave mode equipment (I_A in Figure 1/V.230). The corresponding offset at the master mode equipment may be greater due to delay in the interface cable and varies by configuration.

FIGURE 3/V.230

Frame structure at the GDCI

5.4.2.1 *Slave to master*

Each frame consists of the following groups of bits; each individual group is DC-balanced by its last bit (L bit):

Bit position	*Group*
1 and 2	framing signal with balance bit
3-11	BV1 channel (first octet) with balance bit
12 and 13	DV-channel bit with balance bit
14 and 15	F_A auxiliary framing bit or Q bit with balance bit
16-24	BV2 channel (first octet) with balance bit
25 and 26	DV-channel bit with balance bit
27-35	BV1 channel (second octet) with balance bit

36 and 37	DV-channel bit with balance bit
38-46	BV2 channel (second octet) with balance bit
47 and 48	DV channel bit with balance bit

5.4.2.2 *Master to slave*

Frames transmitted by the master contain an echo channel (E bits) used to retransmit the DV bits received from the slaves. The DV-echo channel is used for DV-channel access control. The last bit of the frame (L bit) is used for balancing each complete frame.

The bits are grouped as follows:

Bit position	*Group*
1 and 2	framing signal with balance bit
3-10	BV1 channel (first octet)
11	E, DV-echo-channel bit
12	DV-channel bit
13	bit A used for activation
14	F_A auxiliary framing bit
15	N bit (coded as defined in § 6.3)
16-23	BV2 channel (first octet)
24	E, DV-echo-channel bit
25	DV-channel bit
26	M, multiframing bit
27-34	BV1 channel (second octet)
35	E, DV-echo-channel bit
36	DV-channel bit
37	S, layer 1 multiframe channel bit
38-45	BV2 channel (second octet)
46	E, DV-echo-channel bit
47	DV-channel bit
48	frame balance bit

5.4.2.3 *Relative bit positions*

At the slave mode equipment, timing in the direction to the master mode equipment shall be derived from the frames received from the master mode equipment.

The first bit of each frame transmitted from a slave equipment towards the master equipment shall be delayed, nominally, by two bit periods with respect to the first bit of the frame received from the master equipment. Figure 3/V.230 illustrates the relative bit positions for both transmitted and received frames.

5.5 *Line code*

For both directions of transmission, pseudo-ternary coding is used with 100% pulse width as shown in Figure 4/V.230. Coding is performed in such a way that a binary ONE is represented by no line signal; whereas, a binary ZERO is represented by a positive or negative pulse. The first binary ZERO following the framing balance bit is of the same polarity as the framing balance bit. Subsequent binary ZEROs must alternate in polarity. A balance bit is a binary ZERO if the number of binary ZEROs following the previous balance bit is odd. A balance bit is a binary ONE if the number of binary ZEROs following the previous balance bit is even.

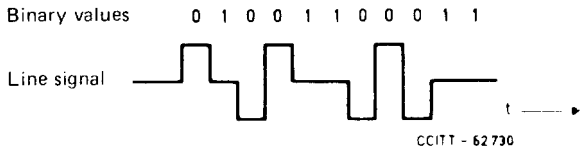


FIGURE 4/V.230

Pseudo-ternary code - example of application

5.6 *Timing considerations*

Equipment may employ one of two timing sources, if available, for transmission of frames across the interface:

- timing derived from an internal source or from an external source conveyed to the equipment by other means (e.g. timing derived from the receive line timing by a V-DCE). This is referred to as "master timing mode". Exactly one equipment on a GDCI bus must operate in this mode.
- timing derived from the receive side of the interface ("loopback timing"). This is referred to as "slave timing mode".

6 Interface procedures

6.1 *DV-channel access procedure*

The following procedure allows for a number of slave mode equipments connected in a multipoint configuration to gain access to the DV channel in an orderly fashion. The procedure always ensures that, even in cases where two or more equipments attempt to access the DV channel simultaneously, one, but only one, of the equipments will be successful in completing transmission of its information. This procedure relies upon the use of layer 2 frames delimited by flags consisting of the binary pattern "01111110" and the use of zero bit insertion to prevent flag imitation (see Recommendation I.441).

The procedure also permits equipment to operate in a point-to-point manner.

6.1.1 *Interframe (layer 2) time fill*

When a slave mode equipment has no layer 2 frames to transmit, it shall send binary ONEs on the DV channel, i.e., the interframe time fill in the slave-to-master direction shall be all binary ONEs.

When a master timing mode equipment has no layer 2 frames to transmit, it shall send binary ONEs or HDLC flags on the DV channel, i.e., the interframe time fill in the master-to-slave direction shall be either all binary ONEs or repetitions of the octet "01111110". When the interframe time fill is HDLC flags, the flag which defines the end of a frame may define the start of the next frame.

6.1.2 *D-echo channel*

The master timing mode equipment, on receipt of a DV-channel bit, shall reflect the binary value, in the next available DV-echo-channel bit position towards the slave mode equipment.

6.1.3 *DV-channel monitoring*

Slave mode equipment, while in the active condition, shall monitor the DV-echo channel, counting the number of consecutive binary ONEs. If a ZERO bit is detected, the equipment shall restart counting the number of consecutive ONE bits. The current value of the count is called C.

Note - C need not be incremented after the value eleven has been reached.

6.1.4 *Priority mechanism*

Layer 2 frames are transmitted using one of two priority classes. Priority class 1 frames are given priority over priority class 2 frames. Furthermore, to ensure that within each priority class all competing equipments are given a fair access to the DV channel, once an equipment has successfully completed the transmission of a frame, it is given a lower level of priority within that class. The equipment is given back its normal level within a priority class when all equipments have had an opportunity to transmit information at the normal level within that priority class.

The priority class of a particular layer 2 frame may be a characteristic of the equipment which is preset at manufacture or at installation, or it may be passed down from layer 2 as a parameter of the PH-DATA REQUEST primitive. A dual mode (GDCI/ISDN) terminal may thus use the PH-DATA REQUEST primitive to establish the proper priorities for its operation.

The priority mechanism is based on the requirement that slave mode equipment may start layer 2 frame transmission only when C (see § 6.1.3) is equal to, or exceeds, the value X_1 for priority class 1 or is equal to, or exceeds, the value X_2 for priority class 2. The value of X_1 shall be eight for the normal level and nine for the lower level of priority. The value of X_2 shall be ten for the normal level and eleven for the lower level of priority.

In a priority class, the value of the normal level of priority is changed into the value of the lower level of priority (i.e., higher value) when the equipment has successfully transmitted a layer 2 frame of that priority class.

The value of the lower level of priority is changed back to the value of the normal level of priority when C (see § 6.1.3) equals the value of the lower level of priority (i.e., higher value).

6.1.5 *Collision detection*

While transmitting information in the DV channel, slave mode equipment shall monitor the received DV-echo channel and compare the last transmitted bit with the next available DV-echo bit. If the transmitted bit is the same as the received echo, the equipment shall continue its transmission. If, however, the received echo is different from the transmitted bit, the equipment shall cease transmission immediately and return to the DV-channel monitoring state.

6.1.6 *Priority system*

Annex B describes an example of how the priority system may be implemented.

6.2 *Activation/deactivation*

6.2.1 *Definitions*

6.2.1.1 *Slave mode equipment states (normally DTE)*

6.2.1.1.1 State F1 (inactive): In this inactive state, the equipment is not transmitting. This state is entered upon loss of power.

6.2.1.1.2 State F2 (sensing): This state is entered after the equipment has been powered on, but has not determined the type of signal (if any) being received.

6.2.1.1.3 State F3 (deactivated): This is the deactivated state of the physical protocol. Neither the master nor the slave equipment is transmitting.

6.2.1.1.4 State F4 (awaiting signal): When the equipment is requested to initiate activation by means of an ACTIVATE REQUEST primitive, it transmits a signal (INFO 1) and waits for a response.

6.2.1.1.5 State F5 (identifying input): At the first receipt of any signal from the master mode equipment, the slave mode equipment ceases to transmit INFO 1 and awaits identification of signal INFO 2 or INFO 4.

6.2.1.1.6 State F6 (synchronized): When the equipment receives an activation signal (INFO 2) from the master, it responds with a signal (INFO 3) and waits for normal frames (INFO 4).

6.2.1.1.7 State F7 (identifying interface): This is a transition state during entry to normal activation. When this state is entered, a timer (T4) is started, and the appropriate (DTE or DCE) identification character is transmitted on the multiframe Q channel. This state continues until either a V-series identification character is received on the multiframe S channel or T4 times out.

6.2.1.1.8 State F8 (lost framing): This is the condition where the equipment has lost frame synchronization and is awaiting re-synchronization by receipt of INFO 2 or INFO 4 or deactivation by receipt of INFO 0.

6.2.1.1.9 State F9 (activated): This is the normal active state with the protocol activated in both directions. Both the master and slave mode equipments are transmitting normal frames.

6.2.1.2 *Master mode equipment states (normally DCE)*

6.2.1.2.1 State G1 (deactive): In this deactivated state, the equipment is not transmitting.

6.2.1.2.2 State G2 (pending activation): In this partially active state, the master mode equipment sends INFO 2 while waiting for INFO 3. This state will be entered after receiving an ACTIVATE REQUEST primitive, or on the receipt of INFO 0 or lost framing while in state G3 or G5. Then the choice to eventually deactivate is up to higher layers within the equipment.

6.2.1.2.3 State G3 (identifying interface): This is a transition state during entry to normal activation. When this state is entered, a timer (T4) is started, and the appropriate (DTE or DCE) identification character is transmitted on the multiframe S channel. This state continues until either a V-series identification (DTE or DCE) is received on the multiframe Q channel or T4 times out.

6.2.1.2.4 State G4 (pending deactivation): When the equipment wishes to deactivate, it may wait for a timer to expire before returning to the deactivated state.

6.2.1.2.5 State G5 (active): This is the normal active state where the master and slave mode equipment are transmitting INFO 4 and INFO 3 respectively. A deactivation may be initiated by a DEACTIVATE REQUEST primitive, or the equipment may remain in the active state all the time, under non-fault conditions.

6.2.1.3 *Activate primitives*

The following primitives should be used between layers 1 and 2 and between layer 1 and the management entity in the activation procedures. For use in state diagrams, etc., abbreviations of the primitive names are also given.

PH-ACTIVATE REQUEST (PH-AR)

PH-ACTIVATE INDICATION (PH-AI)

MPH-ACTIVATE REQUEST (MPH-AR)

MPH-ACTIVATE INDICATION (MPH-AI)

6.2.1.4 *Deactivate primitives*

The following primitives should be used between layers 1 and 2 and between layer 1 and the management entity in the deactivation procedures. For use in state diagrams, etc., abbreviations of the primitive names are also given.

MPH-DEACTIVATE REQUEST (MPH-DR)

MPH-DEACTIVATE INDICATION (MPH-DI)

PH-DEACTIVATE REQUEST (PH-DR)

PH-DEACTIVATE INDICATION (PH-DI)

6.2.1.5 *Management primitives*

The following primitives should be used between layer 1 and the management entity. For use in state diagrams, etc., abbreviations of the primitive names are also given.

MPH-ERROR INDICATION (MPH-EI)
Message unit contains type of error or recovery from a previously reported error.

MPH-INFORMATION INDICATION (MPH-II)

Message unit contains information regarding the physical layer conditions. The provisionally defined parameters are: connected, disconnected, attached DTE, attached DCE, attached TE, and attached NT.

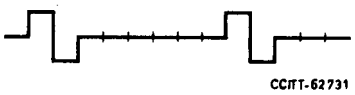
Note - Implementation of primitives in equipment is not for recommendation.

6.2.2 *Signals*

The identifications of specific signals across the GDCI are given in Table 2/V.230. Also included is the coding for these signals.

TABLE 2/V.230

Definition of INFO signals (Note 1)

Signals from MASTER TO SLAVE		Signals from SLAVE TO MASTER	
INFO 0	No signal	INFO 0	No signal
		INFO 1 (Note 2)	A continuous signal with the following pattern: Positive ZERO, negative ZERO, six ONEs  Nominal bit rate = 192 kbit/s
INFO 2 (Note 3)	Frame with all bits of BV, DV and DV-echo channels set to binary ZERO. Bit A set to binary ZERO. N and L bits set according to the normal coding rules.	INFO 3	Synchronized frames with operational data on BV and DV channels.
INFO 4	Frames with operational data on BV, DV and DV-echo channels. Bit A set to binary ONE.		

Note 1 - For configurations where the wiring polarity may be reversed (see § 4.3) signals may be received with the polarity of the binary ZEROs inverted. All receivers should be designed to tolerate wiring polarity reversals.

Note 2 - Slave mode equipment which does not need the capability to initiate activation of a deactivated V.230 interface need not have the capability to send INFO 1. In all other respects, this equipment shall be in accordance with § 6.2. It should be noted that in the point-to-multipoint configuration more that one slave mode equipment transmitting simultaneously will produce a bit pattern, as received by the master mode equipment, different from that described above, e.g., two or more overlapping (asynchronous) instances of INFO 1.

Note 3 - During the transmission of INFO 2 or INFO 4, the F bits and the M/bits from the master mode equipment provide the Q-bit pattern designation as described in § 6.3.3.

6.2.3 *Activation/deactivation procedure for slave mode equipment*

6.2.3.1 *General procedures*

All slave mode equipment conforms to the following procedures (these statements are an aid to understanding; the complete procedures are specified in § 6.2.3.2):

a) Equipment, when first connected, when power is applied, or upon the loss of frame alignment (see § 6.3.1.1) shall transmit INFO 0. However, an equipment that is disconnected but powered could be transmitting INFO 1 when connected.

b) Equipment transmits INFO 3 when frame alignment is established (see § 6.3.1.2). However, the satisfactory transmission of operational data cannot be assured prior to the receipt of INFO 4.

c) Equipment shall, when power is removed, initiate the transmission of INFO 0 before frame alignment is lost.

6.2.3.2 *Specification of the procedure*

The procedure for equipment to follow during activation/deactivation is shown in the form of a finite state matrix Table 3/V.230. The use of the primitives at the layer 1/2 boundary and at the layer 1 /management entity boundary are also included. Those primitives serve to identify the connection status, and to identify whether other equipment connected to the passive bus is operating according to V.230 or I.430.

TABLE 3/V.230

Activation/deactivation layer 1 finite state matrix for GDCI slave (DTE)

Event \ State name	Inactive	Seizing	Deactivated	Awaiting signal	Identifying input	Synchronized	Identifying interface	Lost framing	Activated
State number	F1	F2	F3	F4	F5	F6	F7	F8	F9
INFO sent	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0	INFO 3
Loss of power	/	F1	MPH-II(d); F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1
App. of power	F2	/	/	/	/	/	/	/	/
MPH-Act. Req. or PH-Act. Req	/	|	ST.T3 F4	|	|	-	|	-	|
Expiry T3	/	/	-	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	MPH-DI PH-DI; F3	-	-	-
Rec. INFO 0	/	MPH-II(c); F3	-	-	-	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	MPH-DI, PH-DI, MPH-EI2 F3	MPH-DI, PH-DI; F3
Rec. any signal (Note 1)	/	-	-	F6	-	/	/	-	/
Rec. INFO 2	/	MPH-II(c); F6	F6	/	F6	-	MPH-EI1; F6	MPH-EI2 F6	MPH-EI1; F6

TABLE 3/V.230 *(cont.)*

State name	Inactive	Seizing	Deactivated	Awaiting signal	Identifying input	Synchronized	Identifying interface	Lost framing	Activated
State number	F1	F2	F3	F4	F5	F6	F7	F8	F9
Event / INFO sent	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0	INFO 3
Rec. INFO 4 (Note 2)	/	MPH-II(c), MF-Q, ST.T4 F7	Send MF-Q ST.T4; F7	/	Send MF-Q ST.T4; F7	MPH-E12, Send MF-Q, ST.T4; F7	-	MPH-E12, Send MF-Q, ST.T4; F7	-
Rec. MF-S (DTE)	/	/	/	/	/	/	PH-AI, MPH-AI, MPH-II (a-DTE); F9	/	Send MF-Q; -
Rec. MF-S(DCE)	/	/	/	/	/	/	PH-AI, MPH-AI, MPH-II (a-DCE); F9	/	Send MF-Q; -
Expiry T4	-	-	-	-	-	-	PH-AI, MPH-AI, MPH-II (a-NT); F9	-	-
Lost framing	/	/	/	/	/	MPH-EI1; F8	MPH-EI1; F8	-	MPH-EI1; F8

–	No change, no action
|	Impossible by the definition of the layer 1 service
/	Impossible situation
a, b; Fn	Issue primitives or take actions "a" and "b" and then go to state "Fn"
PH-AI	Primitive PH - ACTIVATE INDICATION
PH-DI	Primitive PH - DEACTIVATE INFORMATION
MPH-AI	Primitive MPH - ACTIVATE INDICATION
MPH-DI	Primitive MPH - DEACTIVATE INDICATION
MPH-EI1	Primitive MPH - ERROR INDICATION REPORTING ERROR
MPH-EI2	Primitive MPH - ERROR INDICATION REPORTING RECOVERY
MPH-II(c)	Primitive MPH - INFORMATION INDICATION (connected)
MPH-II(d)	Primitive MPH - INFORMATION INDICATION (disconnected)
MPH-II(a-DCE)	Primitive MPH - INFORMATION INDICATION (attached, V-series DCE)
MPH-II(a-DTE)	Primitive MPH - INFORMATION INDICATION (attached, V-series DTE)
MPH-II(a-NT)	Primitive MPH - INFORMATION INDICATION (attached, I-series NT)
MF-Q	Multiframe V-series equipment ID on Q-channel (either DTE or DCE ID)
MF-S	Multiframe V-series equipment ID on Q-channel
ST.T3	Start timer T3
ST.T4	Start timer T4

Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals which are available all the time. The multiframe signals must be sent for a fixed number of multiframe periods, provisionally 6 periods.

Note 1 - This event reflects the case where a signal is received and the equipment has not (yet) determined whether it is INFO 2 or INFO 4.

Note 2 - Timer 4 (T4) is a supervisory timer which provides for the master timing mode equipment(s) to recognize the multiframe identification signal and reply. If no reply is received before T4 times out, connection to an I-series NT is assumed. The value of T4 is provisionally 500 ms.

6.2.4 *Activation/deactivation for master mode equipment*

6.2.4.1 *Activating/deactivating equipment*

The procedure is shown in the form of a finite state matrix Table 4/V.230. The primitives at the layer 1/2 boundary and layer 1/management entity boundary are also shown. Those primitives serve to identify the connection status, and to identify whether other equipment connected to the passive bus is operating according to V.230 or I.430.

6.2.4.2 *Non-activating/non-deactivating equipment*

The behaviour of such equipment is the same as that of an activating/deactivating equipment never receiving DEACTIVATE REQUEST primitive. States G1 (deactive), G4 (pending deactivation) and timers 1 and 2 may not exist for such equipment.

6.2.5 *Timer values*

Timers are defined in the finite state matrix tables for both the master and slave mode GDCI equipment. The following values are defined for timers:

- Timer 1 in master mode equipment: values from 2 s (for GDCI only application) to 30 s (for dual mode GDCI or ISDN application) are acceptable.
- Timer 2 in master mode equipment: values from 25 to 100 ms are acceptable. The value may be zero if the equipment does not provide for deactivation.
- Timer 3 in slave mode equipment: value must be selected longer than the worst case time to activate the equipment. The value should be at least one second longer than the value of T1 in the master equipment connected to the GDCI.
- Timer 4: This is the time allowed for other equipment in the GDCI to recognize a V-series equipment ID on the multiframe (S or Q) channel and to respond. This should normally take less than 30 ms, so the value of T4 is provisionally set to 50 ms.

6.2.6 *Activation and deactivation times*

Slave mode equipment in the deactivated state (F3) shall, upon receipt of INFO 2, establish frame synchronization and begin transmission of INFO 3 within 100 ms. It shall recognize receipt of INFO 4 within two frames (in the absence of errors).

Slave mode equipment in the "waiting for signal" state (F4) shall, upon the receipt of INFO 2, cease the transmission of INFO 1 and initiate the transmission of INFO 0 within 5 ms and then respond to INFO 2, within 100 ms, as above. (Note that in Table 3/V.230, the transition from F4 to F5 is indicated as the result of the receipt of "any signal" which is in recognition of the fact that the equipment may not know that the signal being received is INFO 2 until after it has recognized the presence of a signal.)

Master mode equipment use of the "deactivated" and "pending activation" states remains a topic for future study. If these states and transitions are implemented, the timing recommendations of I.430 § 6.2.6.2 should be followed.

6.2.7 *Multiframe identification codes*

Two characters must be selected from the unassigned values on the multiframe Q channel to identify a V-series DTE and a V-series DCE operating in the slave timing mode. Similarly, one character must be selected from the unassigned values on the multiframe S channel (SC1) to identify a V-series DCE operating in the master timing mode.

Since there are only 16 characters available on each of these multiframe channels, the selection must be done carefully. The following character codes have provisionally been selected for the purpose of identifying V-series equipment using a GDCI:

Value ($S_{11}S_{12}S_{13}S_{14}$ or $Q_1Q_2Q_3Q_4$)	Meaning
1101 on Q channel	V-DTE, slave mode
1100 on Q channel	V-DCE, slave mode
0110 on S channel	V-DCE, master mode

Note - These codes are unassigned in the current US Draft Specification.

TABLE 4/V.230

Activation/deactivation layer 1 finite state matrix for CDCI master (DCE)

Event \ State name	Deactive	Pending activation	Identifying interface	Pending deactivation	Active
State number	G1	G2	G3	G4	G5
INFO sent	INFO 0	INFO 2	INFO 4	INFO 0	INFO 4
MPH -Act. Req. or PH-Act. Req.	Start T1; G2	|	|	Start T1; G2	|
MPH-Deact. Req. or PH-Deact. Req.	|	Start T2; PH-DI; G4	Start T2; PH-DI; G4	|	Start T2; PH-DI; G4
Expiry T1 (Note 1)	-	Start T2; PH-DI; G4	/	-	/
Expiry T2 (Note 2)	-	-	-	G1	-
Rec. INFO 0	-	-	MPH-DI, MPH-EI; G2	G1	MPH-DI, MPH-EI; G2
Rec. INFO 1	Start T1; G2	-	/	-	/
Rec. INFO 3	/	Stop T1, Start T4, Send MF-S; G3 (Note 3)	-	-	-
Rec. MF-Q (DTE)	/	/	PH-AI, MPH-AI, MPH-II(a-DTE); G5	-	Send MF-S; -
Rec. MF-Q (DCE)	/	/	PH-AI, MPH-AI, MPH-II(a-DTE); G5	-	Send MF-S; -
Expiry T4	-	-	PH-AI, MPH-AI, MPH-II(a-TE); G5	-	-
Lost framing	/	/	MPH-DI MPH-EI G2	-	MPH-DI, MPH-EI; G2

–	No change, no action
|	Impossible by the definition of the layer 1 service
/	Impossible situation
a, b; Gn	Issue primitives or take actions "a" and "b" then go to state "Gn"
PH-AI	Primitive PH - ACTIVATE INDICATION
PH-DI	Primitive PH - DEACTIVATE INDICATION
MPH-AI	Primitive MPH - ACTIVATE INDICATION

MPH-DI	Primitive MPH - DEACTIVATE INDICATION
MPH-EI	Primitive MPH - ERROR INDICATION REPORTING ERROR
MPH-II(a-DCE)	Primitive MPH - INFORMATION INDICATION (attached, V-series DCE)
MPH-II(a-DTE)	Primitive MPH - INFORMATION INDICATION (attached, V-series DTE)
MPH-II(a-TE)	Primitive MPH - INFORMATION INDICATION (attached, I-series TE)
MF-S	Multiframe V-series equipment ID on S-channel (currently only a DCE ID is defined)
MF-Q	Multiframe V-series equipment ID on Q-channel (DCE or DTE)

Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals which are available all the time. The multiframe signals must be sent for a fixed number of multiframe periods, provisionally 6 periods.

Note 1 - Timer 1 (T1) is a supervisory timer which has to take into account the overall time to activate.

Note 2 - Timer 2 (T2) prevents unintentional reactivation. Its value is normally between 25 ms and 100 ms. This implies that a slave timing mode equipment must recognize INFO 0 and react on it within 25 ms. If the master timing mode equipment is able to unambiguously recognize INFO 1, or if the master timing mode equipment does not use the MPH-DEACTIVATE REQUEST primitive, then the value of T2 may be 0.

Note 3 - Timer 4 (T4) is a supervisory timer which provides time for the slave timing mode equipment(s) to recognize the multiframe identification signal and reply. If no reply is received before T4 times out, connection to an I-series TE is assumed. The value of T4 is provisionally 50 ms.

6.3 *Frame alignment procedures*

The first bit of each frame is the framing bit, *f*; it is a binary ZERO.

The frame alignment procedure makes use of the fact that the framing bit is represented by a pulse having the same polarity as the preceding pulse (line code violation). This allows rapid reframing.

According to the coding rule, both the framing bit and the first binary ZERO bit following the framing balance bit (in the same frame) produce a line code violation. To guarantee secure framing, the auxiliary framing bit pair F_A and N in the direction master-to-slave or the auxiliary framing bit F_A with the associated balancing bit L in the direction slave-to-master are introduced. This ensures that there is a line code violation at 14 bits or less from the framing bit F, due to F_A or N being a binary ZERO bit (master-to-slave) or to F_A being a binary ZERO bit (slave-to-master) if the F_A bit position is not used as a Q bit. The framing procedures do not depend on the polarity of the framing bit F, and thus are not sensitive to wiring polarity.

The coding rule for the auxiliary framing bit pair F_A and N, in the direction master-to-slave, is such that N is the binary opposite of F_A ($N = F_A$). The F_A and L bits in the direction slave-to-master are always coded such that the binary values of F_A and L are equal.

6.3.1 *Frame alignment procedure in the direction master-to-slave to slave timing mode equipment*

Frame alignment, on initial activation of the slave mode equipment, shall comply with the procedures defined is § 6.2.

6.3.1.1 *Loss of frame alignment*

Loss of frame alignment may be assumed when a time period equivalent to two 48-bit frames has elapsed without having detected valid pairs of line code violations obeying the ≤ 14 bit criterion as described above. The slave timing mode equipment shall cease transmission immediately.

6.3.1.2 *Frame alignments*

Frame alignment may be assumed to occur when three consecutive pairs of line code violations obeying the ≤ 14 bit criterion have been detected.

6.3.2 *Frame alignment in the direction slave-to-master timing mode equipment*

The criterion of a line code violation at 13 bits or less from the framing bit (F) shall apply except if the Q channel (see § 6.3.3) is provided, in which case the 13-bit criterion applies in four out of five frames.

6.3.2.1 *Loss of frame alignment*

The master mode equipment may assume loss of frame alignment if a time equivalent to at least two 48-bit frames has elapsed since detecting consecutive violations according to the 13-bit criterion, if all F_A bits have been set to binary ZERO. Otherwise, a time period equivalent to at least three 48-bit frames shall be allowed before assuming loss of frame alignment. On detection of loss of frame alignment, the master equipment shall continue transmitting towards the slave equipment.

6.3.2.2 *Frame alignment*

The master timing mode equipment may assume that frame alignment has been regained when three consecutive pairs of line code violations obeying the 13-bit criterion has been detected.

6.3.3 *Multi-framing*

A multi-frame described in the following paragraphs is intended to provide extra layer 1 capacity in the slave-to-master direction through the use of an extra channel between the slave and master equipment (Q channel).

The use of the Q bits shall be the same in point-to-point as in point-to-multipoint configurations. Future standardization for the use of Q bits is for further study. (There is no inherent collision detection mechanism provided, and any collision detection mechanism that is required for any application of the Q bits will be outside the scope of this Recommendation.)

6.3.3.1 *General mechanism*

a) Q bit identification: The Q bits (slave mode to master mode equipment) are defined to be the bits in the F_A bit position of every fifth frame. The Q bit positions in the slave-to-master direction are identified by binary inversions of the F_A/N bit pair (F_A = binary ONE, N = binary ZERO) in the master-to-slave direction. The provison for identification of the Q-bit positions in the master-to-slave direction permits all slave mode equipment to synchronize transmission in Q-bit positions, thereby avoiding interference of F_A bits from one equipment with the Q bits of a second equipment in passive bus configurations.

b) Multi-frame identification: A multi-frame, which provides for structuring the Q bits in groups of four (Q1-Q4), is established by setting the M bit, in position 26 of the master-to-slave frame, to binary ONE in every twentieth frame. This structure provides for 4-bit characters in a single channel, slave-to-master.

6.3.3.2 *Q-bit position identification algorithm*

The Q-bit position identification algorithm is illustrated in Table 5/V.230. Two examples of how such an identification algorithm can be realized are as follows. The slave mode equipment Q-bit identification algorithm may be simply the transmission of a Q-bit in each frame in which a binary ONE is received in the F_A-bit position of the master-to-slave frame (i.e., echoing of the received F_A bits). Alternatively, to minimize the Q-bit transmission errors that could result from errors in the F_A bits of master-to-slave frames, a slave mode equipment may synchronize a frame counter to the Q-bit rate and transmit Q bits in every fifth frame, i.e., in frames in which F_A should be present. Q bits would be transmitted only after counter synchronization to the binary ONEs in the F_A bit positions of the master-to-slave frames is achieved (and only if such bits are received). When the counter is not synchronized (not achieved or lost), a slave mode equipment which uses such an algorithm shall transmit binary ZEROs in Q-bit positions. The algorithm used by a slave mode equipment to determine when synchronization is defined to be achieved or the algorithm used to determine when it is defined to be lost is not described in this Recommendation.

No special Q-bit identification is required in the master mode equipment because the maximum round trip delay of the master-to-slave-to-master is a small fraction of a frame, and therefore, Q-bit identification is inherent in the master timing mode equipment.

TABLE 5/V.230

Q-bit position identification and multiframe structure

Frame number	MASTER TO SLAVE F_A bit position	SLAVE TO MASTER F_A bit position (1, 2)	MASTER TO SLAVE M bit
1	ONE	Q1	ONE
2	ZERO	ZERO	ZERO
3	ZERO	ZERO	ZERO
4	ZERO	ZERO	ZERO
5	ZERO	ZERO	ZERO
6	ONE	Q2	ZERO
7	ZERO	ZERO	ZERO
8	ZERO	ZERO	ZERO
9	ZERO	ZERO	ZERO
10	ZERO	ZERO	ZERO
11	ONE	Q3	ZERO
12	ZERO	ZERO	ZERO
13	ZERO	ZERO	ZERO
14	ZERO	ZERO	ZERO
15	ZERO	ZERO	ZERO
16	ONE	Q4	ZERO
17	ZERO	ZERO	ZERO
18	ZERO	ZERO	ZERO
19	ZERO	ZERO	ZERO
20	ZERO	ZERO	ZERO
1	ONE	Q1	ONE
2	ZERO	ZERO	ZERO
etc.			

Note 1 - If the Q bits are not used by a slave mode equipment, the Q bits shall be set to binary ONE.

Note 2 - Where multiframe identification is not provided with a binary ONE in an appropriate M bit, but where Q-bit positions are identified, Q bits 1 through 4 are not distinguished.

6.3.3.3 *Slave timing mode equipment multiframe identification*

The first frame of the multiframe is identified by the M bit equal to a binary ONE. Slave mode equipment shall use the M bit equal to a binary ONE to identify the start of the multiframe.

The algorithm used by a slave mode equipment to determine when synchronization or loss of synchronization of the multiframe is achieved is not described in this Recommendation.

6.3.4 *S channel structuring algorithm*

The algorithm for structuring the S bits (master-to-slave frame bit position 37) into an S channel uses the same combination of the F_A bit inversions and the M bit that is used to structure the Q channel as described in § 6.3.3. The S channel structure, shown in Table 6/V.230, provides for five subchannels, SC1 through SC5. Each subchannel SCn is comprised of the bits SCn1 through SCn4 which provides for the transfer of one 4-bit character per multiframe (5 ms). This Recommendation discusses the use of subchannel SC1 only. Subchannels SC2 through SC5 are reserved for future use, and shall be coded with all binary ZEROs. The coding and use of the 4-bit character of SC1 are discussed in § 6.2.7.

TABLE 6/V.230

S-channel structure

Frame number	F_A bit	M bit	S bit
1	ONE	Q1	SC11
2	ZERO	ZERO	SC21
3	ZERO	ZERO	SC31
4	ZERO	ZERO	SC41
5	ZERO	ZERO	SC51
6	ONE	ZERO	SC12
7	ZERO	ZERO	SC22
8	ZERO	ZERO	SC32
9	ZERO	ZERO	SC42
10	ZERO	ZERO	SC52
11	ONE	ZERO	SC13
12	ZERO	ZERO	SC23
13	ZERO	ZERO	SC33
14	ZERO	ZERO	SC43
15	ZERO	ZERO	SC53
16	ONE	ZERO	SC14
17	ZERO	ZERO	SC24
18	ZERO	ZERO	SC34
19	ZERO	ZERO	SC44
20	ZERO	ZERO	SC54
1	ONE	ONE	SC11
2	ZERO	ZERO	SC21
etc.			

Note - Subchannels SC2 through SC5 are reserved for future standardization and are set to all binary ZEROs.

6.4 *Idle channel code on the BV channels*

A slave mode equipment shall send binary ONEs in any BV channel which is not assigned to it.

7 Layer 1 maintenance

Test loopbacks, similar to those defined in Recommendation I.430, are for further study.

8 Electrical characteristics

8.1 *Bit rate*

8.1.1 *Nominal rate*

The nominal bit rate is 192 kbit/s.

8.1.2 *Tolerance*

The tolerance (free running mode) is ± 100 ppm.

8.2 *Jitter and bit-phase relationship between slave mode equipment input and output*

8.2.1 *Test configurations*

The jitter and phase deviation measurements are carried out with four different waveforms at the slave mode equipment input, in accordance with the following configurations:

i) point-to-point configuration with 6 dB attenuation measured between the two terminating resistors at 96 kHz (high capacitance cable),

ii) short passive bus with 8 units (including the unit under test) clustered at the far end from the signal source (high capacitance cable),

iii) a) and b) short passive bus with the unit under test adjacent to the signal source and the other seven units clustered at the far-end from the signal source (high and low capacitance cable);

iv) ideal test signal condition, with one source connected directly to the receiver of the unit under test (i.e., without artificial line).

Examples of waveforms that correspond to the configurations i), ii), iiia) and iiib) are given in Figures 5/V.230 to 8/V.230. Test configurations which can generate these signals are given in Annex C.

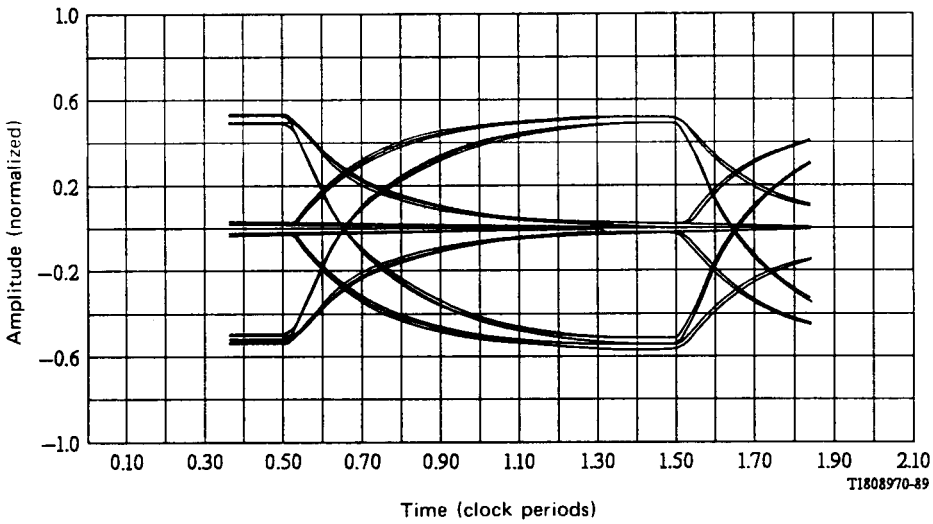


FIGURE 5/V.230

Waveform for test configuration i) - point-to-point (6 dB)
(C = 120 nF/km)

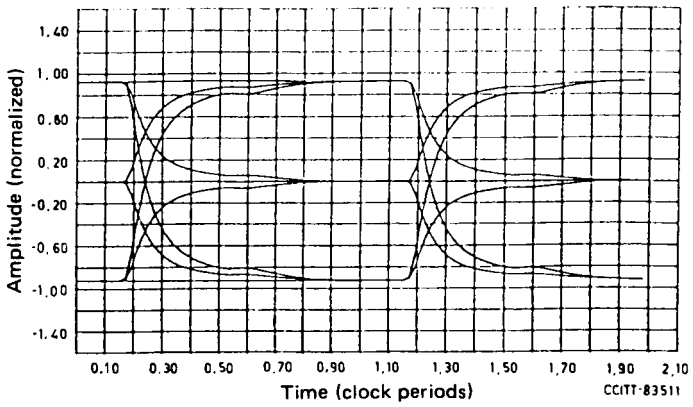


FIGURE 6/V.230

Waveform for test configuration ii) - short passive bus with 8 clustered slave mode equipments at the far end (C = 120 nF/km)

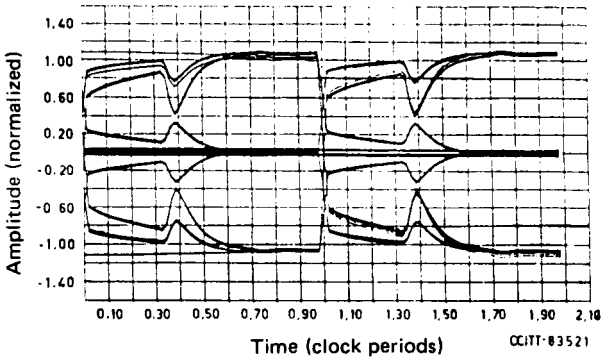


FIGURE 7/V.230

Waveform for test configuration iii a) - short passive bus with 1 slave mode equipment near to the matter mode equipment and 7 slave mode equipments at the far end (C = 120 nF/km)

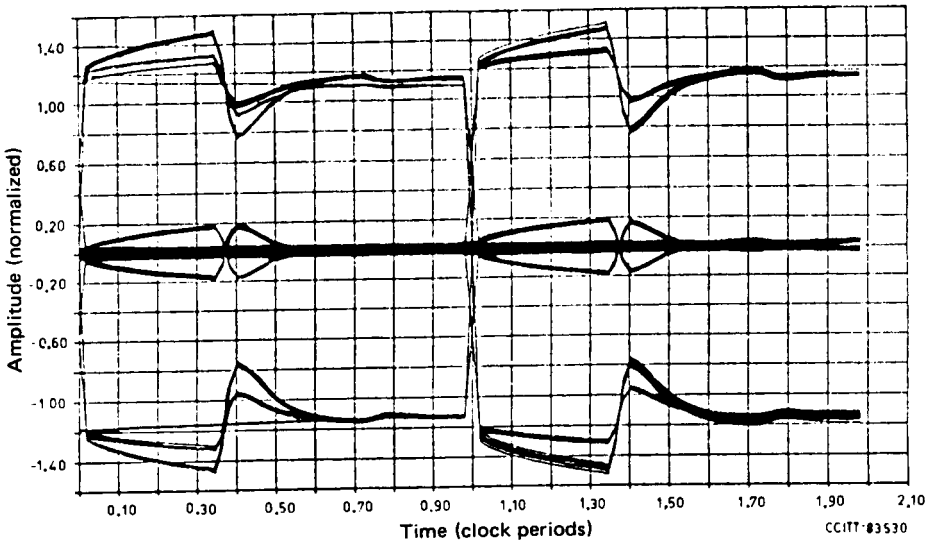


FIGURE 8/V.230

Waveform for test configuration iii b) - short passive but with 1 slave mode equipment near to the waster mode equipment and 7 slave mode equipments at the far end (C = 30 nF/km)

8.2.2 *Timing extraction jitter*

Timing extraction jitter, as observed at the slave mode equipment output, shall be within -7% to + 7% of a bit period, when the jitter is measured using a high pass filter with a cut-off frequency (3 dB point) of 30 Hz under the test conditions described in § 8.2.1. The limitation applies with an output data sequence having binary ZEROs in both BV channels and with input data sequences described in a) to c) following. The limitation applies to the phase of all zero-volt crossings of all adjacent binary ZEROs in the output data sequence.

a) A sequence consisting of continuous frames with all binary ONEs in DV, DV-echo and both BV channels.

b) A sequence, repeated continuously for at least 10 seconds, consisting of:

- 40 frames with continuous octets of "10101010" (the first bit to be transmitted is binary ONE) in both BV channels and continuous binary ONEs in DV and DV-echo channels followed by:
- 40 frames with continuos binary ZEROs in DV, DV-echo and both BV channels.

c) A sequence consisting of a pseudo-random pattern with a length of $2^{19} - 1$ in DV, DV-echo and both BV channels. (This pattern may be generated with a shift register with 19 stages with the outputs of the first, the second, the fifth and the nineteenth stages added together (modulo 2) and fed back to the input.)

8.2.3 *Total phase deviation, input to output*

The total phase deviation (including effects of timing extraction in the slave mode equipment), between the transitions of signal elements at the output of the slave mode equipment and the transitions of signal elements associated with the signal applied to the input, should not exceed the range of - 7% to + 15% of a bit period. This limitation applies to the output signal transitions of each frame with the phase reference defined as the average phase of the crossing of zero volts which occurs between the framing pulse and its associated balance pulse at the start of the frame and the corresponding crossings at the start of the three preceding frames of the input signal. For the purposes of demonstrating compliance of an equipment, it is sufficient to use (as the input signal phase reference) only the crossing of zero volts between the framing pulse and its associated balance pulse of the individual frame. This latter method, requiring a simpler test set, may create additional jitter at frequencies higher than about 1 kHz and is therefore more restrictive. The limitation applies to the phase of the zero-volt crossings of all adjacent binary ZEROs in the output data sequence, which shall be as defined in § 8.2.2. The limitation applies under all test conditions described in § 8.2.1, with the additional input signal conditions specified in a) to d) following, and with superimposed jitter as specified in Figure 9/V.230 over the range of frequencies from 5 Hz to 2 kHz. The limitation applies for input bit rates of 192 kbit/s ± 100 ppm.

a) A sequence consisting of continuous frames with all binary ONEs in the DV, DV-echo and both BV channels.

b) A sequence consisting of continuous frames with the octet "10101010" (the first bit to be transmitted is binary ONE) in both BV channels and binary ONEs in DV and DV-echo channels.

c) A sequence of continuous frames with binary ZEROs in DV, DV-echo and both BV channels.

d) A sequence of continuous frames with a pseudo-random pattern, as described in § 8.2.2 c), in DV, and both BV channels.

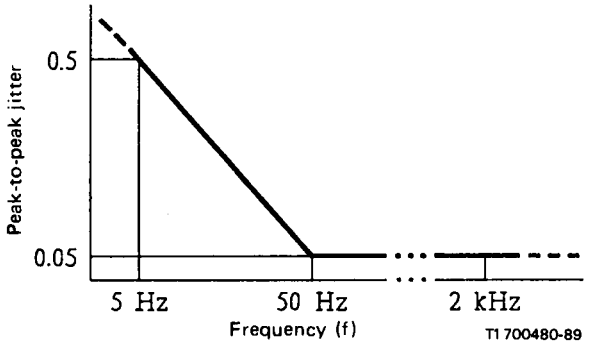


FIGURE 9/V.230

Lower limit of maximum tolerable jitter at slave mode equipment input (log-log scale)

8.3 *Master mode equipment jittter characteristics*

The maximum jitter (peak-to-peak) in the output sequence of a master mode equipment shall be 5% of a bit period when measured using a high pass filter having a cut-off frequency (3 dB point) of 50 Hz and an asymptotic roll off 20 dB per decade. The limitation applies for all data sequences, but for the purpose of demonstrating the compliance of an equipment, it is sufficient to measure jitter with output data sequence consisting of binary ONEs in DV and BV channels and with additional sequence as described in § 8.2.2. c) in DV and BV channels. The limitation applies to the phase of all-zero volt crossings of all adjacent binary ZEROs in the output data sequence.

8.4 *Termination of the line*

The interchange circuit pair termination (resistive) should be 100 ohms ± 5% (see Figure 2/V.230).

8.5 *Transmitter output characteristics*

8.5.1 *Transmitter output impedance*

The following requirements apply at interface point I_A (see Figure 2/V.230 for slave mode equipment) and at interface point I_B for master mode equipment (see §§ 4.5 and 8.9 regarding cordage capacitance).

8.5.1.1 *Master mode equipment transmitter output impedance*

a) When inactive or transmitting a binary ONE, the output impedance, in the frequency range of 2 kHz to 1 MHz, shall exceed the impedance indicated by the template in Figure 10/V.230. The requirement is applicable with an applied sinusoidal voltage of at least 100 mV (r.m.s. value).

Note - In some applications, the terminating resistor can be combined with the master mode equipment (see point B of Figure 2/V.230). The resulting impedance is the impedance needed to exceed the combination of the template and the 100-ohm termination.

b) When terminating a binary ZERO, the output impedance shall be ≥ 20 ohms.

Note - The output impedance limit shall apply for two nominal load impedance (resistive) conditions: 50 ohms and 400 ohms. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value ± 10%. The peak amplitude shall be defined as the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.

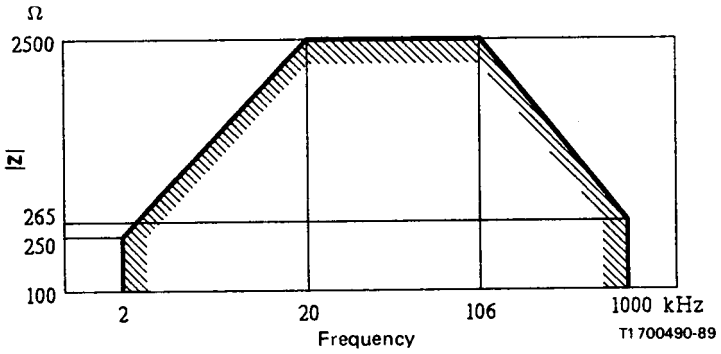


FIGURE 10/V.230

Master mode equipment impedance template (log-log scale)

8.5.1.2 *Slave mode equipment transmitter output impedance*

a) In the inactive and powered down states or when transmitting a binary ONE, the following requirements apply:

i) the output impedance, in the frequency range of 2 kHz to 1 MHz, should exceed the impedance indicated by the template in Figure 11/V.230. This requirement is applicable with an applied sinusoidal voltage of at least 100 mV (r.m.s. value);

ii) at a frequency of 96 kHz, the peak current which results from an applied voltage of up to 1.2 V (peak value) should not exceed 0.6 mA (peak value).

b) When transmitting a binary ZERO, the output impedance shall be ≥ 20 ohms.

Note - The output impedance limit shall apply for two nominal load impedance (resistive) conditions: 50 ohms and 400 ohms. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value ± 10%. The peak amplitude shall be defined as the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.

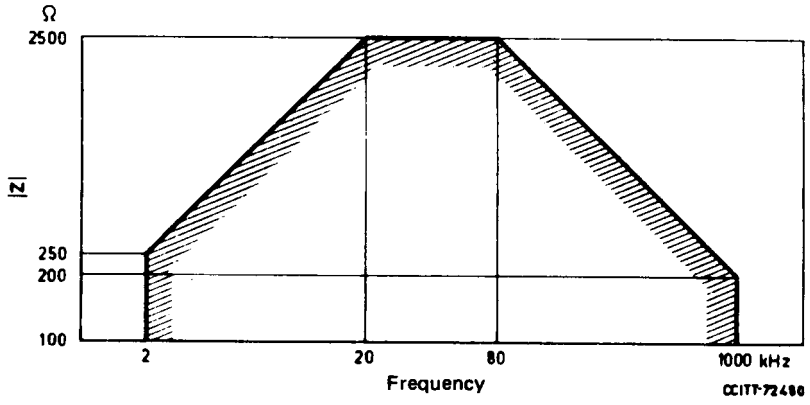


FIGURE 11/V.230

Slave mode equipment impedance template (log-log scale)

8.5.2 *Test load impedance*

The test load impedance shall be 50 ohms (unless otherwise indicated).

8.5.3 *Pulse shape and amplitude (binary ZERO)*

8.5.3.1 *Pulse shape*

Except for overshoot, limited as follows, pulses shall be within the mask of Figure 12/V.230. Overshoot, at the leading edge of pulses, of up to 5% of the pulse amplitude at the middle of a signal element, is permitted, provided that such overshoot has, at 1/2 of its amplitude, a duration of less than 0.25 μs.

8.5.3.2 *Nominal pulse amplitude*

The nominal pulse amplitude shall be 750 mV, zero to peak.

A positive pulse (in particular, a framing pulse) at the output port of master mode and slave mode equipment is defined as a positive polarity of the voltage measured between access leads e to f and d to c respectively (see Figure 20/I.430). (See Table 7/V.230 for the relationship to connector pins.)

8.5.4 *Pulse unbalance*

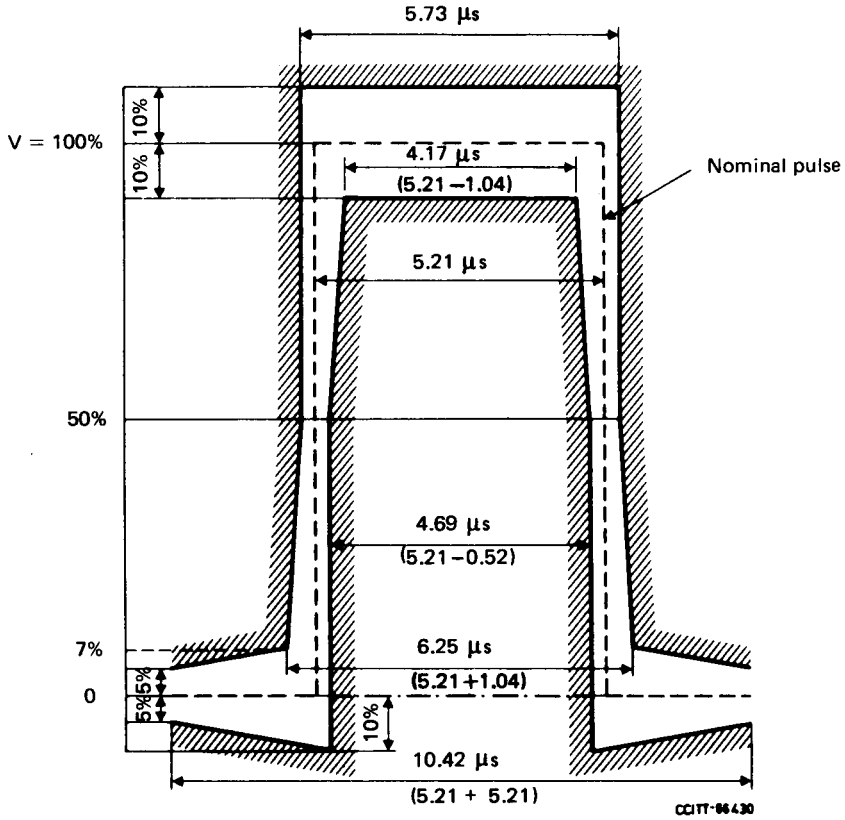
The "pulse unbalance", i.e., the relative difference in $\int U(t)\,dt$ for positive pulses and $\int U(t)\,dt$ for negative pulses shall be $\leq 5\%$.

8.5.5 *Voltage on other test loads (slave mode equipment)*

The following requirements are intended to assure compatibility with the condition where multiple slave mode equipments are simultaneously transmitting pulses on to a passive bus.

8.5.5.1 *400-ohm load*

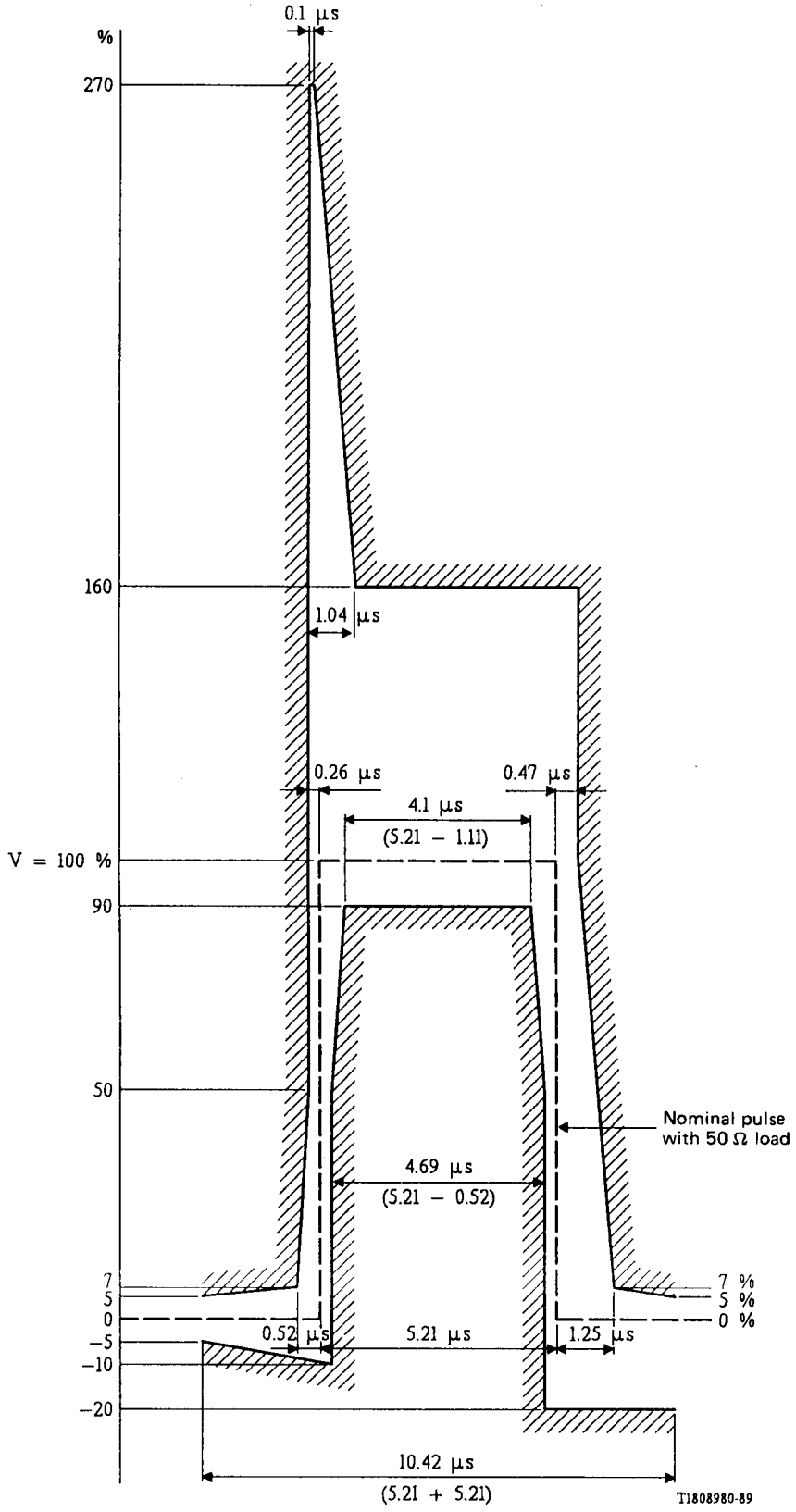
A pulse (binary ZERO) shall conform to the limits of the mask shown in Figure 13/V.230 when the transmitter is terminated in a 400-ohm load.



Note - For clarity of presentation, the above values are based on a pulse width of 5.21 µs. See § 8.1 for a precise specification of the bit rate.

FIGURE 12/V.230

Transmitter output pulse mask



Note - For clarity of presentation, the above values are based on a pulse width of 5.21 µs. See § 8.1 for a precise specification of the bit rate.

FIGURE 13/V.230

Voltage for an isolated pulse with a test load of 400 ohms

8.5.5.2 *5.6-ohm load*

To limit the current flow with two drivers having opposite polarities, the pulse amplitude (peak) with a 5.6-ohm load shall be ≤ 20% of the nominal pulse amplitude.

8.5.6 *Unbalance about earth*

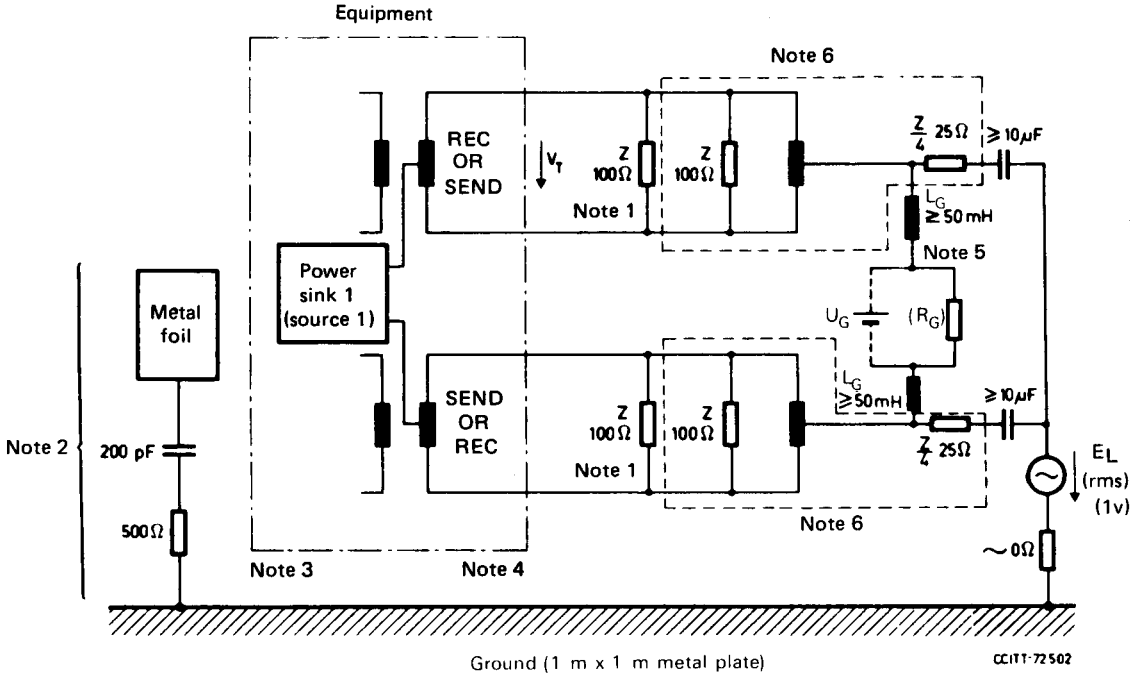
The following requirements apply under all possible power feeding conditions, under all possible connections of the equipment to ground, and with two 100-ohm terminations across the transmit and receive ports.

8.5.6.1 *Longitudinal conversion loss*

Longitudinal conversion loss (LCL), which is measured in accordance with Recommendation G.117, § 4.1.3 (see Figure 14/V.230), shall meet the following requirements:

a) 10 kHz < f ≤ 300 kHz: ≥ 54 dB

b) 300 kHz < f ≤ 1 MHz: minimum value decreasing from 54 dB at 20 dB/decade.



The longitudinal conversion loss: $LCL = 20 \log_{10} \left| \frac{E_L}{V_T} \right|$ dB

The voltages V_T and E_L should be measured within the frequency range from 10 kHz up to 1 MHz using selective test measuring equipment.

The measurement should be carried out in the states:

- deactivated (receive. send).
- power off (receive, send),
- activated (receive).

The interconnecting cord shall lie on the metal plate.

Note 1 - This resistor must be omitted if the termination is already built into the equipment.

Note 2 - Hand imitation is a thin metal foil with approximately the size of a hand.

Note 3 - Equipment with metallic housing shall have a galvanic connection to the metal plate. Other equipment with non-metallic housing shall be placed on the metal plate.

Note 4 - The power cord for mains-powered equipment shall lie on the metal plate and the earth protective wire of the mains shall be connected to the metal plate.

Note 5 - If there is no power source 1 in the master mode equipment, R_G and L_G are not required.

Note 6 - This circuit provides a transverse termination of 100 ohms and a balanced longitudinal termination of 25 ohms. Any equivalent circuit is acceptable. However, for equivalent circuits given in Recommendations G.117 and O.121, powering cannot be provided.

FIGURE 14/V.230

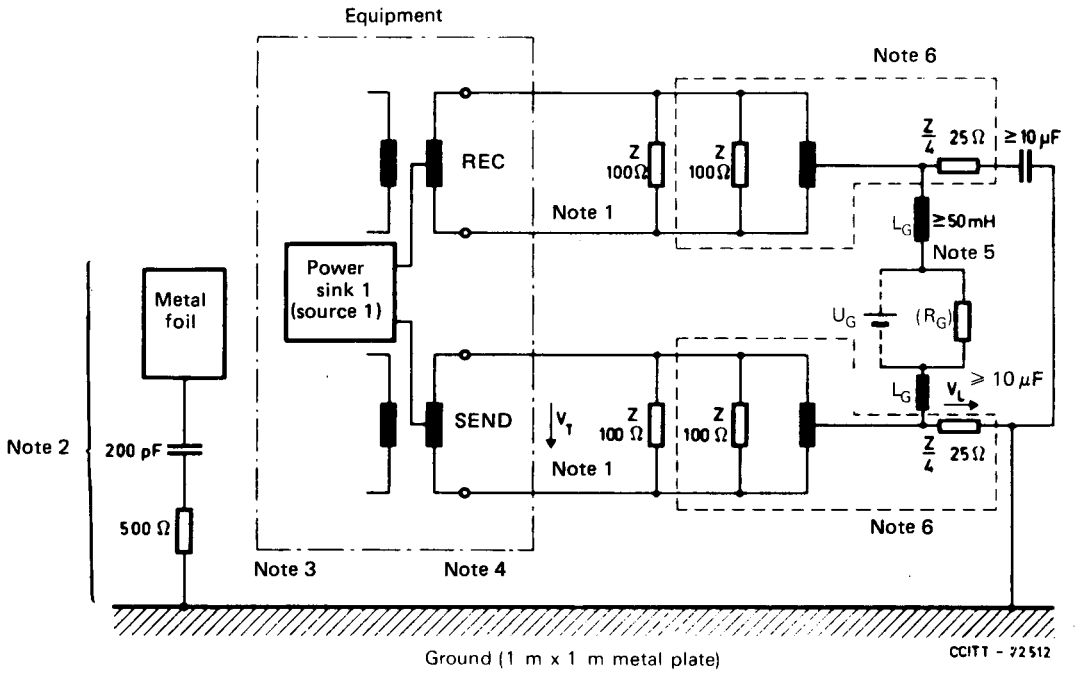
Receiver input or transmitter output unbalance about earth

8.5.6.2 *Output signal balance*

Output signal balance which is measured in accordance with Recommendation G.117, § 4.3.1 (see Figure 15/V.230), shall meet the following requirements:

a) f - 96 kHz: ≥ 54 dB

b) 96 kHz < f ≤ 1 MHz: minimum value decreasing from 54 dB at 20 dB/decade.



$$\text{Output signal balance} = 20 \log_{10} \left| \frac{V_T}{V_L} \right| \text{ dB}$$

The voltage V_T and V_L. should be measured within the frequency range from 10 kHz up to 1 MHz using selective test measuring equipment. The measurement should be carried out in the active state. The pulse patterns should contain all binary ZEROs. However, for the purpose of demonstrating the compliance of an equipment, it is sufficient to measure the output signal unbalance about earth with a pulse pattern of continuous frames with at least the B1 and B2 Channels containing all binary ZEROs.

The interconnecting cord shall lie on the metal plate.

Note - See notes to this figure in Figure 14/V.230.

FIGURE 15/V.230

Transmitter output unbalance about earth

8.6 *Receiver input characteristics*

8.6.1 *Receiver input imbalance*

8.6.1.1 *Slave mode equipment receiver input impedance*

Slave mode equipment shall meet the same input impedance requirements as specified in § 8.5.1.2 a) for the output impedance.

8.6.1.2 *Master mode equipment receiver input impedance*

In the inactive and powered-down states, the following requirements apply:

i) The input impedance in the frequency range of 2 kHz to 1 MHz, should exceed the impedance indicated by the template in Figure 11/V.230. This requirement is applicable with an applied sinusoidal voltage of at least 100 mV (r.m.s. value).

ii) At a frequency of 96 kHz, the peak current which results from an applied voltage of up to 1.2 V (peak value) should not exceed 0.5 mA (peak value).

Note - In some applications, the 100-ohm terminating resistor can be combined with the master mode equipment (see point B of Figure 2/V.230). The resulting impedance is the impedance needed to exceed the combination of the template and the 100-ohm termination.

8.6.2 *Receiver sensitivity - noise and distortion immunity*

Requirements applicable to the equipments for three different interface wiring configurations are given in the following sub-paragraphs. Equipment shall receive, without errors (for a period of at least one minute), an input with a pseudo-random sequence (word length ≥ 511 bits) in all information channels (combination of BV channel, DV channel and, if applicable, the DV-echo channel).

The receiver shall operate, with any input sequence, over the full range indicated by the waveform mask.

8.6.2.1 *Slave mode equipment*

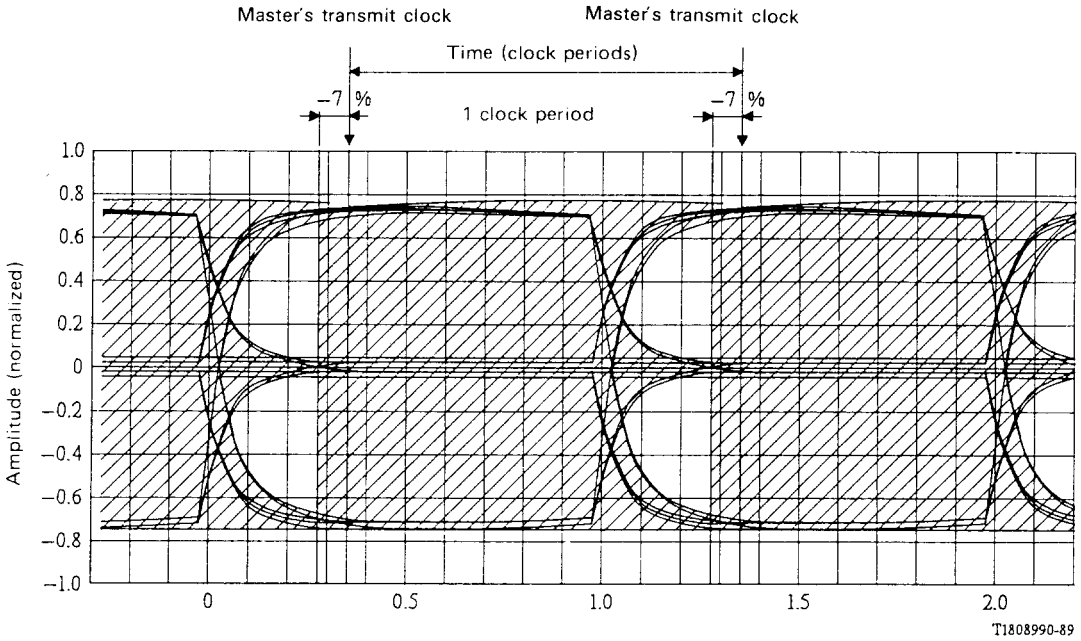
Slave mode equipment shall operate with the input signals conforming to the waveforms specified in § 8.2.1. For the waveforms in Figures 6/V.230 to 8/V.230, slave mode equipment shall operate with the input signals having any amplitude in the range of + 1.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. For signals conforming to the waveform in Figure 5/V.230, operation shall be accomplished for signals having any amplitude in the range of + 1.5 to - 7.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. Additionally, the slave mode equipment shall operate with sinusoidal signals having an amplitude of 100 mV (peak-to-peak value) at frequencies of 200 kHz and 2 MHz superimposed individually on the input signals having the waveform shown in Figure 5/V.230.

8.6.2.2 *Master mode equipment for short passive bus (fixed timing)*

Master mode equipment designed to operate with only short passive bus wiring configurations shall operate when receiving input signals indicated by the waveform shown in Figure 16/V.230. Master mode equipment shall operate, with the input signals having any amplitude in the range of + 1.5 dB to - 3.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2.

8.6.2.3 *Master mode equipment for both point-to-point and short passive bus configurations (adaptive timing)*

Master mode equipment designed to operate with either point-to-point or short passive bus wiring configurations shall operate when receiving input signals indicated by the waveform mask shown in Figure 17/V.230. These master mode equipments shall operate with the input signals having any amplitude in the range of + 1.5 dB to - 3.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. These master mode equipments shall also operate when receiving signals conforming to the waveform in Figure 5/V.230. For signals conforming to this waveform, operation shall be accomplished for signals having any amplitude in the range of + 1.5 to - 7.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. Additionally, these master mode equipments shall operate with the sinusoidal signals, as specified in § 8.6.2.1, superimposed on the input signals having the waveform in Figure 5/V.230.

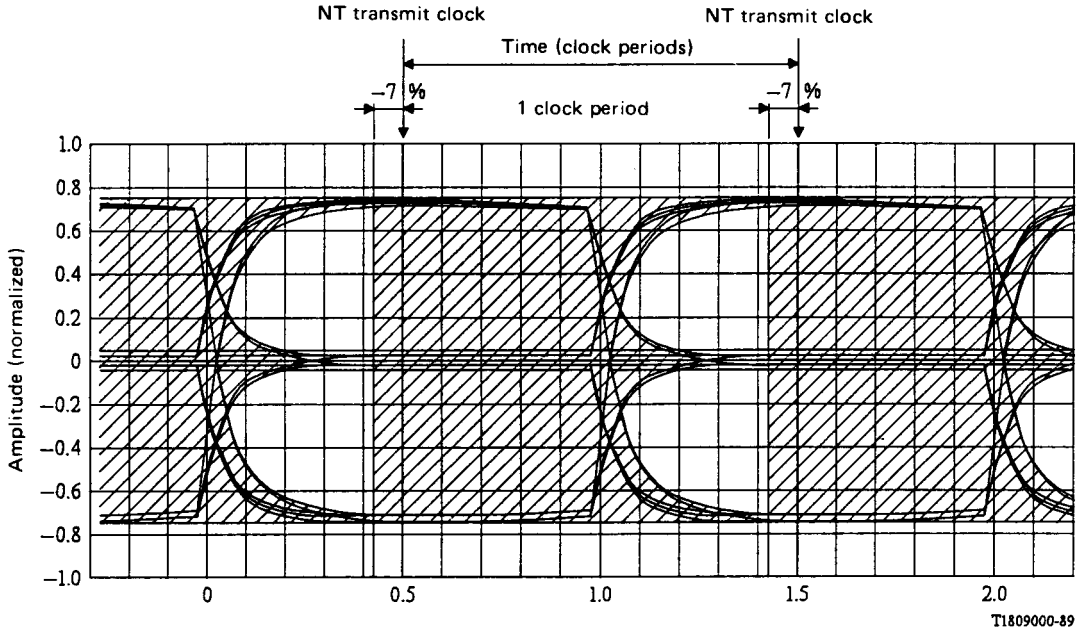


Note 1 - Shaded area is the region in which pulse transitions may occur.

Note 2 - The waveform mask is based on the "worst case" configuration shown in Annex C, Figure C-1/V.230 and waveforms ii) and iii) in § 8.2.1. The shaded area of -7% of one clock period accounts for the situation of a single slave mode equipment connected directly to the master mode equipment with a zero length passive bus. However, the waveform mask does not show the higher possible amplitude of framing and DV-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

FIGURE 16/V.230

Short passive bus receive pulse waveform mask



Note 1 - Shaded area is the region in which pulse transitions may occur.

Note 2 - The waveform mask is based on the same "worst case" passive bus configuration as the waveform mask in Figure 16/V.230 except that the permitted round trip delay of the cable is reduced. The shaded area of - 7 % of one clock period accounts for the situation of a single slave mode equipment connected directly to the master mode equipment with a zero length passive bus. However, the waveform mask does not show the higher possible amplitude of framing and DV-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

FIGURE 17/V.230

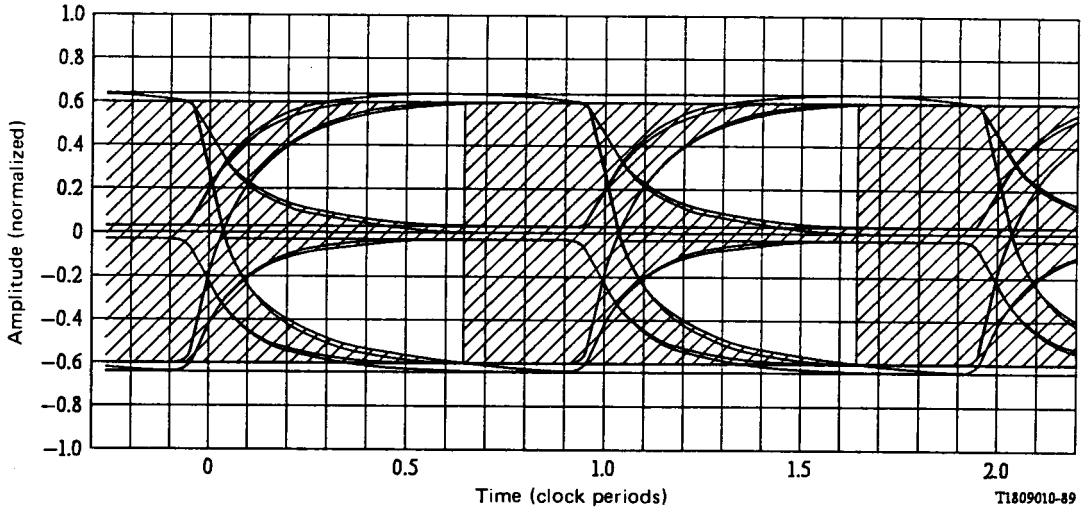
Passive bus receive pulse waveform mask
(Master mode equipment designed to operate with either point-to-point
or short passive bus wiring configurations)

8.6.2.4 *Master mode equipment for extended passive bus wiring configurations*

Master mode equipment designed to operate with extended passive bus wiring configurations shall operate when receiving input signals indicated by the waveform mask shown in Figure 18/V.230. These master mode equipments shall operate with the input signals having any amplitude in the range of + 1.5 dB to - 5.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. Additionally, these master mode equipments shall operate with the sinusoidal signals, as specified in § 8.6.2.1, superimposed on the input signals having the waveform shown in Figure 18/V.230. (The above values assume a maximum cable loss of 3.8 dB. Master mode equipment may be implemented to accommodate higher cable loss.)

8.6.2.5 *Master mode equipment for point-to-point configurations only*

Master mode equipment designed to operate with only point-to-point wiring configurations shall operate when receiving input signals having the waveform shown in Figure 5/V.230. These master mode equipments shall operate with the input signals having any amplitude in the range of +1.5 to -7.5 dB relative to the nominal amplitude of the transmitted signal as specified in § 8.5.3.2. Additionally, these master mode equipments shall operate with the sinusoidal signals, as specified in § 8.6.2.1, superimposed on the input signals having the waveform shown in Figure 5/V.230.



Note 1 - Shaded area is the region in which pulse transitions may occur.

Note 2 - The waveform mask is based on the worst case extended passive bus wiring configuration. It consists of a cable having a characteristic impedance of 75 ohms, a capacitance of 120 nF/km, a lose of 3.8 dB at 96 kHz, four slave mode equipments connected such that the differential delay is at the maximum permitted by § 8.6.3.3. The waveform mask does not show the higher possible amplitude of framing and DV-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

FIGURE 18/V.230

Extended passive bus receive pulse waveform mask

8.6.3 *Master mode equipment receiver input delay characteristics*

Note - Round trip delay is always measured between the zero-volt crossings of the framing pulse and its associated balance bit pulse at the transmit and receive sides of the master mode equipment (see also Annex A).

8.6.3.1 *Master mode equipment for short passive bus*

Master mode equipment shall accommodate round trip delays of the complete installation, including slave mode equipment, in the range 10 to 14 μs.

8.6.3.2 *Master mode equipment for both point-to-point and passive bus*

Master mode equipment shall accommodate round trip delays (for passive bus configurations) in the range 10 to 13 μs.

Master mode equipment shall accommodate round trip delays (for point-to-point configurations) in the range 10 to 42 μs.

8.6.3.3 *Master mode equipment for extended passive bus*

Master mode equipment shall accommodate round trip delays in the range 10 to 42 μs, provided that the differential delay of signals from different slave mode equipments is in the range 0 to 2 μs.

8.6.3.4 *Master mode equipment for point-to-point only*

Master mode equipment shall accommodate round trip delays specified in § 8.6.3.2 for point-to-point configurations.

8.6.4 *Unbalance about earth*

Longitudinal conversion loss (LCL) of receiver inputs, measured in accordance with Recommendation G.117, § 4.1.3, by considering the power feeding and two 100-ohm terminations at each port, shall meet the following requirements (see Figure 14/V.230):

a) 10 kHz ≤ f ≤ 300 kHz: ≥ 54 dB

b) 300 kHz < f ≤ 1 MHz: minimum value decreasing from 54 dB with 20 dB/decade.

8.7 *Isolation from external voltages*

The electrical environment of interface cable pairs is not specified in this Recommendation.

IEC Publication 479-1, Second Issue 1984, specifies current limitations dealing with human safety. According to that publication, the value of a touchable leakage alternating current measured through a resistor of 2 kOhms is to be limited to 9 mA. The application of this requirement to the user-network interface is not a subject of this Recommendation.

It may be necessary to apportion this value between the number of mains powered equipments connected to the passive bus. A possible maximum value of (touchable) leakage alternating current for each mains powered equipment could be 1 mA. However, it should be noted that leakage current of a fraction of this magnitude may interfere with the satisfactory operation of the equipments.

8.8 *Interconnecting media characteristics*

Longitudinal conversion loss of pairs at 96 kHz shall be ≥ 43 dB.

8.9 *Standard GDCI access cord*

A connecting cord designed to connect equipment to a jack on a passive bus cable must meet the requirements specified in Recommendation I.430 for the "standard ISDN basic access TE cord".

9 Power feeding

Power feeding across the General Data Communication Interface is not required by this Recommendation. All equipment should be capable of operating if power is present in accordance with Recommendation I.430, § 9. In the case of a GDCI application which uses power feed across the interface, power source 2 defined in Recommendation I.430 should be the first choice, followed by either power source 1 or power source 3. Any considerations for operation under restricted power conditions are at the discretion of the application.

10 Interface connector and contact assignments

The interface connector and contact assignments are the subject of an ISO standard. Table 7/V.230 is reproduced from the Draft International Standard, DIS 8877, dated November 1985. For the transmit and receive leads, pole numbers 3 through 6, the polarity indicated is for the polarity of the framing pulses. For the power leads, pole numbers 1, 2, 7 and 8, the polarity indicated is for the polarity of the d.c. voltages. See Figure 20/I.430 for the polarity of power provided in the phantom mode. In that figure, the leads that are lettered a, b, c, d, e, f, g and h correspond with pole numbers 1, 2, 3, 6, 5, 4, 7 and 8, respectively.

TABLE 7/V.230

Pole (contact) assignment for 8-pole connections (plugs and jacks)

Pole number	Function		Polarity
	Slave mode equipment	Master mode equipment	
1	Power source 3	Power sink 3	+
2	Power source 3	Power sink 3	-
3	Transmit	Receive	+
4	Receive	Transmit	+
5	Receive	Transmit	-
6	Transmit	Receive	-
7	Power sink 2	Power source 2	-
8	Power sink 2	Power source 2	+

Note - This reference is only provisional.

ANNEX A

(to Recommendation V.230)

Wiring configurations and round trip delay considerations used as a basis for electrical characteristics

A.1 *Introduction*

A.1.1 In § 4 of this Recommendation, two major wiring arrangements are identified. These are point-to-point configuration and a point-to-multipoint configuration using a passive bus.

While these configurations may be considered to be the limiting cases for the definition of the interfaces and the design of the associated equipments, other significant arrangements should be considered.

A.1.2 The values of overall length, in terms of cable loss and delay assumed for each of the possible arrangements, are indicated below.

A.1.3 Figure 2/V.230 is a composite of the individual configurations. These individual configurations are shown in this Annex.

A.2 *Wiring configurations*

A.2.1 *Point-to-multipoint*

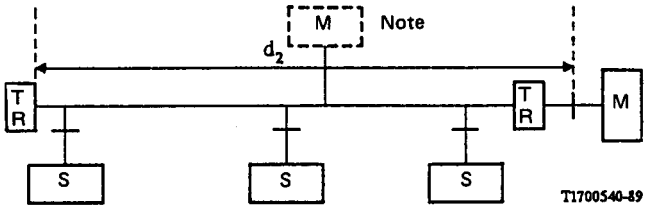
A.2.1.1 The point-to-multipoint wiring configuration identified in § 4.2 of this Recommendation may be provided by the "short passive bus" or other configurations such as "extended passive bus".

A.2.1.2 *Short passive bus* (Figure A-1/V.230)

An essential configuration to be considered is a passive bus in which the slave mode devices may be connected at random points along the full length of the cable. This means that the master mode equipment receiver must cater for pulses arriving with different delays from various terminals. For this reason, the length limit for this configuration is a function of the maximum round trip delay and not of the attenuation.

A master mode equipment receiver with fixed timing can be used if the round trip delay is between 10 to 14 us. This relates to a maximum operational distance from the master mode equipment in the order of 100-200 m (d_2 in Figure A-1/V.230) [200 m in the case of a high impedance cable (Z_c = 150 ohms) and 100 m in the case of a low impedance cable (Z_c = 75 ohms)]. It should be noted that the slave master equipment connections acts as stubs on the cable, thus reducing the master mode equipment receiver margin over that of a point-to-point configuration. A maximum number of 8 slave mode equipments with connections of 10 m in length are to be accommodated.

The range of 10 to 14 μs for the round trip delay is composed as follows. The lower value of 10 μs is composed of two bits offset delay (see Figure 3/V.230) and the negative phase deviation of -7% (see § 8.2.3). In this case the slave mode equipment is located directly at the master mode equipment. The higher value of 14 μs is calculated assuming the slave mode equipment is located at the far end of a passive bus. This value is composed of the offset delay between frames of two bits (10.4 μs), the round trip delay of the unloaded bus installation (2 μs), the additional delay due to load of the slave mode equipment (i.e., 0.7 μs) and the maximum delay of the slave mode equipment transmitter according to § 8.2.3 (15% = 0.8 μs).



TR Terminating resistor

M Master

S Slave

Note - In principle, the master mode equipment may be located at any point along the passive bus. The electrical characteristics in this Recommendation, however, are based on the master mode equipment located at one end. The conditions related to other locations require confirmation.

FIGURE A-1/V.230

Short passive bus

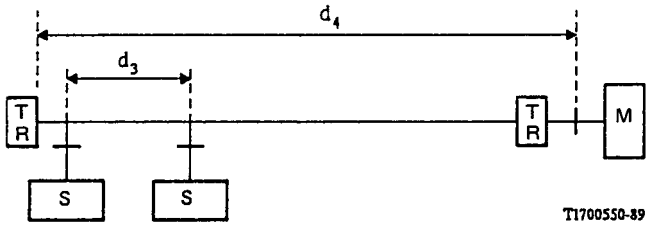
A.2.1.3 *Extended passive bus* (Figure A-2/V.230)

A configuration which may be used at an intermediate distance in the order of 100 m and 1000 m is known as an extended passive bus. This configuration takes advantage of the fact that terminal connection points are restricted to a grouping at the far end of the cable from the master mode equipment. This places a restriction on the differential distance between slave mode equipments. The differential round trip delay is defined as that between zero-volt crossings of signals from different slave mode equipments and is restricted to 2 μs.

This differential round trip delay is composed of a slave mode equipment differential delay of 22% or 1.15 μs according to § 8.2.3, the round trip delay of the unloaded bus installation of 0.5 μs (line length: 25 to 50 m) and an additional delay due to the load of 4 slave mode equipments (0.35 μs).

d_3 depends on the characteristics of the cable to be used.

The objective for this extended passive bus configuration is a total length of at least 500 m (d_4 in Figure A-2/V.230) and a differential distance between slave mode equipment connection points of 25 to 50 m (d_3 in Figure A-2/V.230). However, an appropriate combination of the total length, the differential distance between slave mode equipments connected to the cable, may be determined by individual Administrations.



TR Terminating resistor

M Master

S Slave

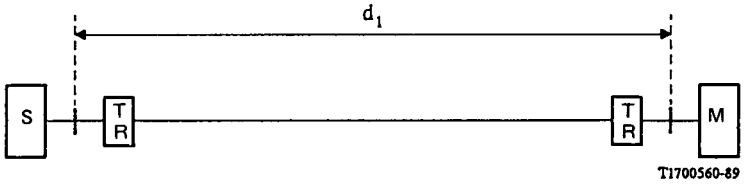
FIGURE A-2/V.230

Extended passive bus

A.2.2 *Point-to-point* (Figure A-3/V.230)

This configuration provides for one transmitter/receiver only at each end of the cable (see Figure A-3/V.230). It is, therefore, necessary to determine the maximum permissible attenuation between the ends of the cable to establish the transmitter output level and the range of receiver input levels. In addition, it is necessary to establish the maximum round trip delay for any signal which must be returned from one end to the other within a specified time period (limited by DV-echo bits).

A general objective for the operational distance between equipment units is 1.0 km (d_1 in Figure A-3/V.230). It is agreed to satisfy this general objective with a maximum cable attenuation of 6 dB at 96 kHz. The round trip delay is between 10 to 42 μs.



TR Terminating resistor

M Master

S Slave

FIGURE A-3/V.320

Point-to-point

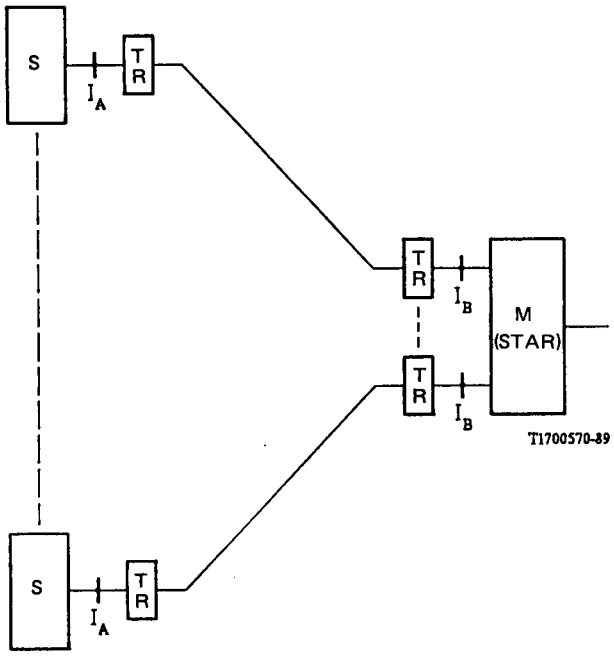
The lower value of 10 μs is derived in the same way as for the passive bus configuration. The upper value is composed of the following elements:

- 2 bits due to frame offset (2×5.2 μs = 10.4 μs, see § 5.4.2.3);
- maximum 6 bits delay permitted due to the distance between master and slave devices and the required processing time (6×5.2 μs = 31.2 μs);
- the fraction (+ 15%) of a bit period due to phase deviation between slave mode equipment input and output (see § 8.2.3, 0.15×5.2 μs = 0.8 μs).

It should be noted that an adaptive timing device at the receiver is required at the master mode equipment to meet these limits.

For the master mode equipment used for point-to-point and passive bus configurations (see § 8.6.3.2), the tolerable round trip delay in passive bus wiring configurations is reduced to 13 us due to the extra tolerance required for the adaptive timing. Using this type of wiring configuration, it is also possible to provide point-to-multipoint mode of operation at layer 1.

Note - Point-to-multipoint operation can be accommodated using only point-to-point wiring. One suitable arrangement is STAR illustrated in Figure A-4/V.230. In such an implementation, bit streams from slave mode equipments must be buffered to provide for operation of the DV-echo channel(s) to provide for contention resolution, but only layer 1 functionality is required. It is also possible to support passive bus wiring configurations on the ports of STARs.



TR Terminating resistor

M Master

S Slave

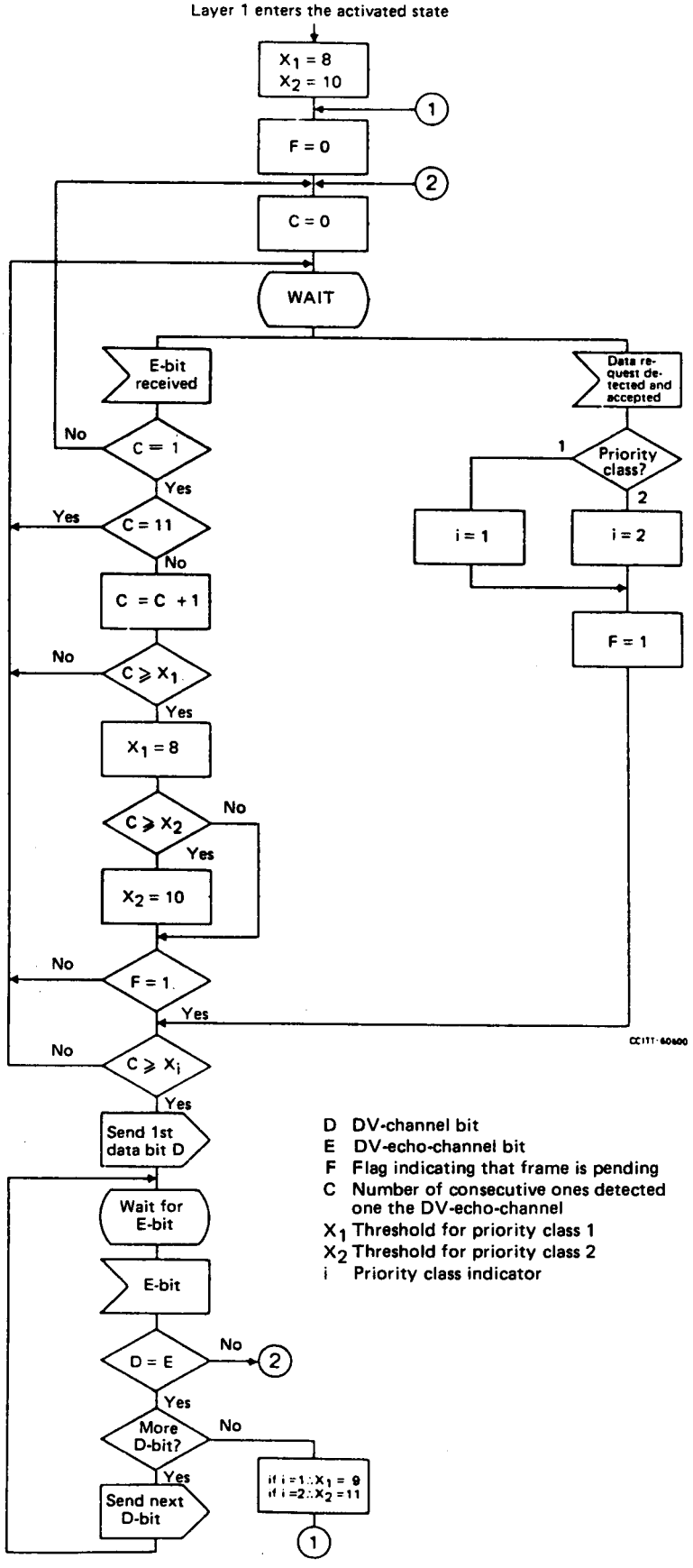
FIGURE A-4/V.230

Star

ANNEX B

(to Recommendation V.230)

SDL representation of a possible implementation of the DV-channel access



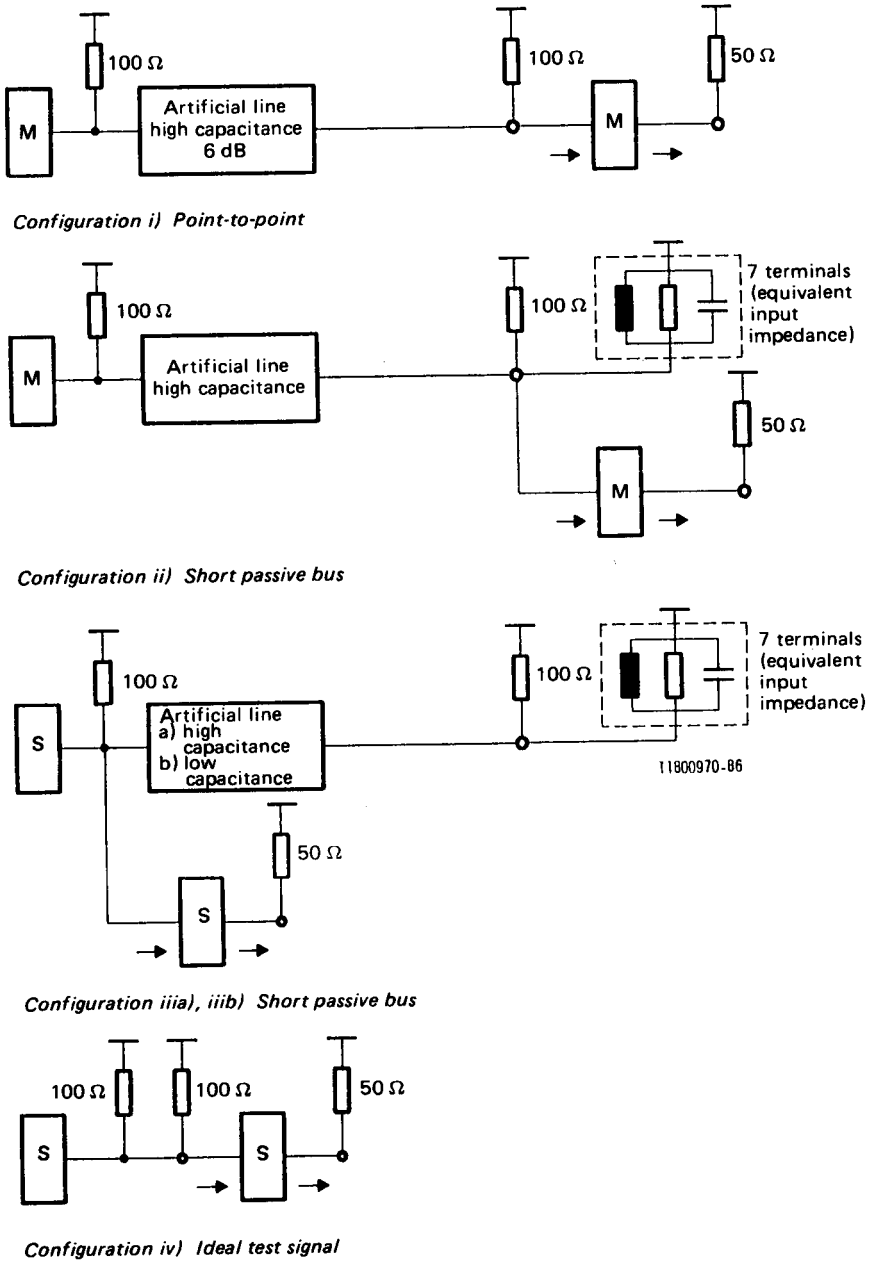
ANNEX C

(to Recommendation V.230)

Test configurations

In § 8 of this Recommendation, waveforms are shown for testing master and slave mode equipment. This Annex describes configurations, for testing slave mode equipment, which can be used to generate these waveforms (see Figure C-1/V.230). Similar configurations can be used to test master mode equipment.

Table C-1/V.230 gives the parameters for the artificial lines reproduced in Figure C-1/V.230. The artificial lines are used to derive the waveforms. For test configurations ii) and iii), the cable length used corresponds to a signal delay of 1 μs.



M Master

S Slave

FIGURE C-1/V.230

Test configurations

TABLE C-1/V.230

Parameters for the artificial lines

Parameters	High capacitance cable	Low capacitance cable
R (96 kHz)	160 ohms/km	160 ohms/km
C (1 kHz)	120 nF/km	30 nF/km
Zo (96 kHz)	75 ohms	150 ohms
Wire diameter	0.6 mm	0.6 mm