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SERIES J: CABLE NETWORKS AND TRANSMISSION OF TELEVISION, SOUND PROGRAMME AND OTHER MULTIMEDIA SIGNALS

Interactive systems for digital television distribution

Timing interface for cable modem termination systems

ITU-T Recommendation J.211

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Timing interface for cable modem termination systems

Summary

The timing interface for cable modem termination systems (DTI) defined in ITU-T Recommendation J.211, supports the accurate and robust transport of the DTI server 10.24-MHz master clock, 32-bit cable modem termination timestamp, and time of day, to the DTI client within the modular cable modem termination system (M-CMTS) cable network. The DTI protocol is structured to minimize the complexity and cost of the DTI client clocks, and the per-port cost of the shared server function while supporting all S-CDMA and TDMA timing requirements.

Source

ITU-T Recommendation J.211 was approved on 29 November 2006 by ITU-T Study Group 9 (2005-2008) under the ITU-T Recommendation A.8 procedure.

FOREWORD

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Timing interface for cable modem termination systems

1 Scope

The requirements for timing and synchronization of the DOCSIS system come from the following areas.

- existing DOCSIS specification and testability requirements;
- remote PHY system requirements;
- implementation requirements;
- services like T1 or E1 and wireless.

These requirements place definitions and constraints on the use of the DOCSIS master clock and the DOCSIS timestamp, which is delivered in the SYNC message. The DOCSIS specification originally envisioned the M-CMTS-CORE, EQAMs, and upstream receive functions on one assembly, fed with a common clock. The timestamp counter resides in the M-CMTS-CORE function.

The M-CMTS™ Remote PHY architecture may result in three components: the M-CMTS-CORE, the upstream receiver, and the EQAM being located in a different chassis, and potentially at different physical locations. As a system, the three components comply with the DOCSIS specification and any existing CMTS equipment.

The DOCSIS timing protocol (DTI) defined in this Recommendation, supports the accurate and robust transport of the DTI server 10.24-MHz master clock, 32-bit DOCSIS timestamp, and time of day, to the DTI client within the DOCSIS M-CMTS cable network. The DTI protocol is structured to minimize the complexity and cost of the DTI client clocks, and the per-port cost of the shared server function while supporting all S-CDMA and TDMA timing requirements.

To support regional differences in master clock frequency, two DTI client options are defined, one producing a 10.24-MHz master clock output, and another producing a 9.216-MHz master clock output. A single DTI server master clock frequency of 10.24 MHz supports DTI clients of both types.

1.1 System requirements

The DTI system requirements refer to the DOCSIS timing requirements as outlined in the DOCSIS specification. These requirements are presented independent of the CMTS architecture.

The clauses of the DOCSIS specification [ITU-T J.122] that are of interest are:

– 6.2.11.2 Mini-slot numbering
– 6.2.21.8.2 Chip timing jitter for synchronous operation
– 6.3.7 CMTS timestamp jitter
– 6.3.8 CMTS clock generation
– 6.3.9 CMTS downstream symbol clock jitter for synchronous operation
– 6.3.10 CMTS downstream symbol clock drift for synchronous operation
– 9.3 Timing and synchronization

1.2 TDM services consideration

To maintain compatibility with the TDM service synchronization hierarchy, the DTI server clock operates with the specifications detailed in clause 8.1 which integrate both the DOCSIS timing system requirements and the existing legacy synchronization network clock consistent with [ITU-T G.812] and [T1.101]. This is done to ensure that the CM supporting TDM services can derive its clocking and meet [ITU-T G.823] or [ITU-T G.824] jitter and wander requirements for both traffic-bearing and synchronization-bearing transport clock sources.

Support of TDM services will require that the master clock and the downstream symbol clock be locked and upstream and downstream clocks be coherent.

1.3 Modular implementation requirements

The M-CMTS-CORE element:

- uses the DTI server master clock for creating a timestamp;
- uses the timestamp for MAP generation.

The Edge QAM element:

- uses the DTI server master clock for symbol rate generation;
- uses the timestamp for inserting and/or correcting SYNC messages.

The Upstream receive element:

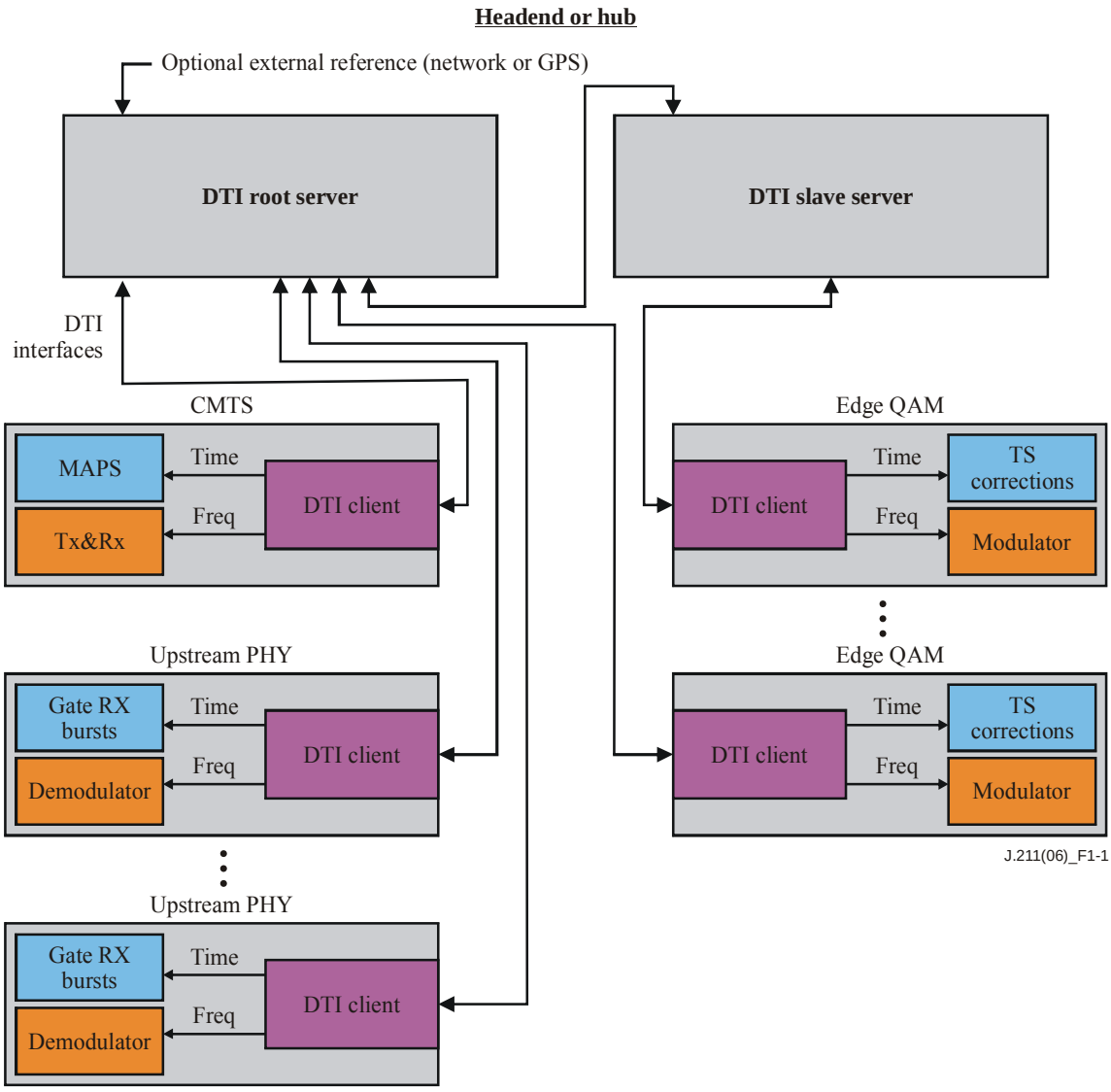
- uses the timestamp and/or S-CDMA frame and the MAP for determining when to look for the start of a receive burst;
- uses a clock locked to the master clock for reception of symbols in S-CDMA mode.

1.4 Architecture

Figure 1-1 shows frequency and timing distribution examples for both headend and hub. The DTI server establishes the reference for the timing distribution network and synchronizes all connected DTI clients via point-to-point connections between the server and each client. A single protocol initiated by the DTI server permits the client to perform frequency and time synchronization. As shown, upstream receive, Edge QAMs, and the M-CMTS-CORE may have different uses for the synchronized frequency and time, but utilize a common client function.

The DTI protocol and server-client interactions are described in detail in clauses 7 and 8. The essential characteristics are:

- The DTI server initiates the protocol, which the DTI client uses to establish its time and frequency synchronization.
- Using a ping-pong scheme, the client always immediately replies to the DTI server when it receives a transmission from the DTI server. The server uses this response to auto-compensate any delays with the effect that the client becomes precisely synchronized to the server.
- The server-to-client-to-server handshake continually repeats, assuring that a tight synchronization can be maintained.



NOTE – CMTS Core, Upstream PHYs and Edge QAMs can be configured for redundancy.
DTI Servers can be configured redundantly and a slave server can be connected to a master server up to a depth of 1 from the master.
All DTI links from a DTI Root Server and connected DTI Slave Servers will be synchronous as if they came from the same server.

Figure 1-1 – Timing architecture

The DTI protocol and components support accurate and robust transport of the server 10.24-MHz master clock and 32-bit DOCSIS timestamp to the client within a node or building. The protocol is structured to minimize the complexity and cost of the client clocks and the per-port cost of the shared server function while supporting all the DOCSIS S-CDMA, TDMA and future TDM services timing requirements in a modular system.

The high accuracy (<5 ns) and high stability (<1-ns timing jitter budget) is achieved by using a simple ping-pong layer-2 timing protocol over a single twisted pair connection using common passive PHY components in both directions. This structure provides delay reciprocity so that all cable delay processing can be performed in the server. The client's role in delay correction is to provide a fixed delay response to the server frame and to use the cable advance supplied by the server to advance the local 10-kHz DTI frame clock to correct for cable delay.

To ensure reliable transport and client clock operation, the client clock is required to report the current phase error of its local clock (frame clock) with respect to the delay-corrected server frame clock. This measurement is reported to the server at the 10-kHz frame rate. The server's role is to process this measurement data and verify the client's timing operation. This protocol supports real-time detection and mitigation of client clock faults.

The DTI client can be realized with a single digital component, a simple PHY and a low-cost local oscillator, as holdover and filtering are supported in the shared server. A common definition of the DTI high-speed clock is necessary to ensure compatibility between all DOCSIS DTI client components.

1.5 Synchronization needed for TDM services deployment

The deployment of TDM services compliant with the existing telecommunications TDM standards (e.g., T1 or E1) will require both synchronization and traceability to a common external clock source. In this case, if a cable modem supporting TDM services is connected to an M-CMTS EQAM, the cable modem will need to be synchronized with the DTI server operating with an external TDM service reference.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.812] ITU-T Recommendation G.812 (2004), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks*.

[ITU-T G.823] ITU-T Recommendation G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

[ITU-T G.824] ITU-T Recommendation G.824 (2000), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy*.

[ITU-T J.122] ITU-T Recommendation J.122 (2002), *Second-generation transmission systems for interactive cable television services – IP cable modems*.

[ISO/IEC 8802-3] ISO/IEC 8802-3:2000, *Information technology – Telecommunications and information exchange between systems – Local and metropolitan area networks – Specific requirements – Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications*.

[T1.101][*)] ANSI T1.101 (1999), *Synchronization Interface Standard*.

2.1 Reference acquisition

– American Institute of Electrical Engineers, Internet: http://www.ieee.org/portal/site

– American National Standards Institute, Internet: http://webstore.ansi.org

*) T1 standards are maintained since November 2003 by ATIS.

3 Terms and definitions

This Recommendation defines the following terms:

3.1 bridging mode: A short-term operating condition of the DTI clock where the DTI client has recently lost its controlling input and is using stored data, acquired while in normal or fast mode operation, to control its output. While in bridging, the degree of deviation of the output is deemed to be such that DTI client clock is still performing within normal or acceptable limits. If an outage period persists, the DTI client clock will transition to the holdover mode indicating that the DTI client clock output may be degraded.

3.2 DTI minimum clock oscillator: An oscillator that supports all the client clock performance requirements with holdover limited to the minimum bridging time. A non-ovenized oscillator can be used to support this oscillator category.

3.3 fast mode: An operating condition of a clock in which it is locked to an external reference and is using time constants, which are reduced to quickly bring the local oscillator's frequency into approximate agreement with the synchronization reference frequency.

3.4 free-run mode: An operating condition of a DTI clock whose output signals are internally controlled by the DTI server. The clock has never had, or has lost, external reference input and has no access to stored data that was acquired from a previously connected external reference during the time after the last power cycle. Free-run ends when the clock output is influenced by an external reference or the process to achieve lock to an external reference. Free-run may provide needed stability when external reference has been lost or not equipped.

3.5 gpssec: The gpssec is a 32-bit timestamp counter that is incremented every second. GPS system time began on January 6, 1980. The gpssec value was set to zero at the January 6, 1980 start epoch.

3.6 holdover mode: An operating condition of a DTI clock that has lost its controlling input and is using stored data, acquired while in normal or fast mode operation, to control its output. The stored data is filtered to minimize the effects of short-term variations and to establish a predictor of oscillator behaviour during the reference outage. This permits the output deviation from normal operation to be minimized.

3.7 maximum time interval error (MTIE): For a sequence of time delay samples x_i, MTIE at observation time (S) is:

$$\text{MTIE measurement: } MTIE(S) = \max_{j=1}^{N-n+1} \left[\max_{i=j}^{n+j-1}(x_i) - \min_{i=j}^{n+j-1}(x_i) \right]$$

where:

τ_o = sample period

N = number of samples in the sequence

n = $[S/\tau_o] + 1$

S = observation time

x_i = time delay sample

3.8 normal mode: An operating condition of a clock in which the output signals are controlled by an external input reference. The expected mode and state permits each clock within a distribution to have the same long-term average frequency and time. Clocks in this mode are referred to as locked meaning that they are in tight relationship with the DTI root clock. A DTI server clock in a fault-free free-run mode will be considered in normal mode.

3.9 root DTI server: The DTI server that is the source of traceable time and frequency for all subtending DTI servers and clients in a building.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

CM	Cable Modem
CMTS	Cable Modem Termination System
CRC	Cyclic Redundancy Check
DEPI	Downstream External PHY Interface
DOCSIS	Data-Over-Cable Service Interface Specification
DS	Downstream
DTI	DOCSIS Timing Interface
DTS	32-bit DOCSIS Time Stamp
EQAM	Edge QAM (A network element which receives MPEG-TS frames over a network interface such as Ethernet, and modulates them onto QAM carriers for use on a HFC plant)
ERMI	Edge Resource Manager Interface
GE	Gigabit Ethernet (1 Gbit/s)
GPS	Global Positioning System
IE	Information Element (An element of a MAP message)
IP	Internet Protocol
M-CMTS	Modular CMTS
MAC	Media Access Control (Used to refer to the layer-2 element of the system, which would include DOCSIS framing and signalling)
MPEG	Motion Picture Experts Group
MPEG-TS	Motion Picture Experts Group Transport Stream
MTIE	Maximum Time Interval Error
NCO	Network Controlled Oscillator
PCR	Program Clock Reference
PHY	Physical Layer (Used to refer to the downstream QAM transmitters and the upstream burst demodulators (receiver))
PID	Packet Identifier used in MPEG-TS
PLL	Phase-Locked Loop
PUSI	Payload Unit Start Indicator
QAM	Quadrature Amplitude Modulation
S-CDMA	Synchronous Code Division Multiple Access
TDM	Time Division Multiplexing
TDMA	Time Division Multiple Access
TDM Services	Legacy T1/E1 or T3/E3 voice and/or data transport
UDP	User Datagram Protocol
US	Upstream

UTC Coordinated Universal Time (Also known as Greenwich Mean Time (GMT) or Zulu time)

5 Conventions

Throughout this Recommendation, the words that are used to define the significance of particular requirements are capitalized. These words are:

"MUST" This word or the adjective "REQUIRED" means that the item is an absolute requirement of this Recommendation.

"MUST NOT" This phrase means that the item is an absolute prohibition of this Recommendation.

"SHOULD" This word or the adjective "RECOMMENDED" means that there may exist valid reasons in particular circumstances to ignore this item, but the full implications should be understood and the case carefully weighed before choosing a different course.

"SHOULD NOT" This phrase means that there may exist valid reasons in particular circumstances when the listed behaviour is acceptable or even useful, but the full implications should be understood and the case carefully weighed before implementing any behaviour described with this label.

"MAY" This word or the adjective "OPTIONAL" means that this item is truly optional. One vendor may choose to include the item because a particular marketplace requires it or because it enhances the product, for example; another vendor may omit the same item. Optional features implemented, MUST meet the defined requirements.

6 Physical layer requirements

This clause specifies the physical layer requirements of the DTI protocol.

6.1 Introduction

The DTI link comprises the connection between a DTI server and various other elements, such as M-CMTS-CORE, EQAM and US receivers collocated in the node that derive their clocking (time and frequency) from the DTI server. Since the link resembles an Ethernet (802.3) 10BaseT link, it is advantageous to leverage the availability and cost effectiveness of this standard. This Recommendation defines the differences between the DOCSIS timing interface and a conventional 802.3-10BaseT interface. Table 6-1 indicates the similarity between the two links.

Table 6-1 – Physical layer comparisons

Characteristics	Ethernet 802.3-10BaseT	DOCSIS timing interface
Data rate (Mbit/s)	10	5.12
Accuracy	Free-running; 100 ppm	Traceable to Master Clock
Transmission mode(s)	Full/half duplex (Note 1)	Ping-Pong (Note 1)
Topology	Star (Note 2)	Star (Note 2)
Maximum segment length	100 m	200 m
Media	UTP	UTP
Signalling method	Baseband	Baseband
Modulation	Manchester	Manchester

Table 6-1 – Physical layer comparisons

NOTE 1 – Conventional Ethernet 802.3 transceivers use separate wire pairs for transmission in the two directions. The DTI uses a ping-pong scheme whereby the same pair is used for transmission in both directions. This ensures the maximal reciprocity, minimizing the asymmetry in transmission delay between the two directions and minimizes crosstalk.

NOTE 2 – Conventional Ethernet installations utilize a star-wiring configuration where the "common" point is a switch or hub. In the DTI scenario, the common point is the DTI server.

The governing standard for Ethernet (physical layer) is [ISO/IEC 8802-3]. The physical layer specifications (primarily section 14 of the standard) are applicable here.

6.2 Physical connector description

The DTI server, as well as the DTI client, MUST have an RJ45 (female) connector for each DTI link. This permits conventional Ethernet cabling techniques to be applied. See [ISO/IEC 8802-3], section 14.5.1. One distinction is that the DTI utilizes a single pair for transmission in both directions. Therefore, a crossover function is not required. Contacts 1 and 2, labelled "SIG+" and "SIG–" will be used for the ping-pong transmission.

The cable interconnect MUST be as defined in Table 6-2.

Table 6-2 – DTI RJ45 interconnect

RJ45 pin number	Signal	Comment
1	SIG+	10BaseT compliant
2	SIG–	10BaseT compliant
3	NC	
4	NC	
5	NC	
6	NC	
7	NC	
8	NC	

6.3 Cable requirements

The DTI MUST operate normally over a maximum of 200 metres of UTP cable rated at category 5E or better.

6.4 Electrical description

6.4.1 Impedance

The termination impedance MUST be 100 ohms. The differential output impedance as measured on the TD circuit MUST be compliant with section 14.3.1.2.2 of [ISO/IEC 8802-3]. The transmitter impedance balance, or the ratio of common-mode to differential-mode impedance balance of the TD circuit MUST exceed $29 - 17 \log_{10}(f/10)$ dB, where f is the frequency in MHz, over the frequency range 1.0 MHz to 20 MHz (see section 14.3.1.2.4 of [ISO/IEC 8802-3]).

6.4.2 Isolation

There MUST be isolation between the physical layer circuits, including frame ground, and all leads including those not used by the DTI link. The isolation requirement follows [ISO/IEC 8802-3], section 14.3.1.

6.4.3 EMI considerations

The DTI link will comply with applicable local and national codes for limitation of electromagnetic interference.

6.4.4 Signal strength (voltage)

The per-symbol peak differential voltage on the SIG± signals at the DTI server, when terminated in a 100-Ω resistive load MUST be between 2.2 V and 2.8 V for all data sequences. For an all-ones Manchester-encoded pattern, any even harmonic measured on the TD circuit MUST be at least 27 dB below the fundamental. The magnitude of the total common-mode output voltage MUST be less than 50 mV peak.

6.4.5 Common-mode rejection

Given application of common-mode voltage of 15 V peak ~10 MHz sine wave (see section 14.3.1.2.6 of [ISO/IEC 8802-3]) the differential-mode voltage MUST NOT change by more than 100 mV for all data sequences. The edge jitter introduced MUST be less than 3 ns.

6.4.6 Signal description

The transmission between the DTI server and the DTI client MUST be ping-pong in nature, using the same pair of wires for transmission in both directions. The data pattern MUST be Manchester encoded with an underlying bit rate of 5.12 Mbit/s, locked to the DTI master clock.

7 DOCSIS timing protocol

See clause 1.1 for an informational description of the DTI protocol.

7.1 DTI timing entities

The DTI protocol is supported by two terminated entities:

1) DTI server;

2) DTI client.

DTI server and client functional entities are part of the M-CMTS architecture. The DOCSIS client function is structured to permit a low-cost client clock function within all EQAMs, upstream receivers, and M-CMTS-CORE entities.

The DTI server SHOULD support multiple client functions to support scalable growth of DTI port capacity within a node or building.

The DTI server MUST support a SNMP management interface, IP addressing and use RJ45 connectors.

A DTI server in a single building MAY consist of active and backup servers components in a common shelf and/or DTI servers in subtending shelves.

A DTI server MAY support at least one of the following two capabilities:

1) operation as a subtending server;

2) provide DTI outputs capable of supporting DTI subtending servers.

The following accuracy requirements may be confirmed with a delay-calibrated client. A delay-calibrated client provides sufficient measurement points to determine current calibrated delay bias.

All DTI root server outputs MUST meet a 1.25-ns accuracy requirement when tested with a delay-calibrated client with respect to the DTI root server master clock test port with correction for test port group delay.

All DTI subtending server outputs MUST meet a 2.5-ns accuracy requirement when tested with a delay-calibrated client with respect to the DTI root server master clock test port with correction for test port group delay.

A DTI output that can support a subtending DTI server MUST meet a 1.25-ns accuracy requirement when tested with delay-calibrated client under normal operating conditions. An M-CMTS EQAM, M-CMTS-CORE or a separate upstream receiver MUST support at least one DTI client interface.

A DTI server in slave mode is intended to only accept a DTI input from a root server.

An M-CMTS device MAY support multiple DTI clients if protection for a DTI interconnect cable loss is desired.

If an M-CMTS device has more than one DTI client, it MUST not switch to a protection client as a result of a loss of DTI input until a minimum timeout of 500 ms.

7.2 DTI timing structure

Figure 7-1 defines the structure of the DOCSIS timing protocol as:

a) sent by the server;

b) received by the client after the cable delay; and

c) output at the Client Test Port after the cable advance correction.

The highest-level structure is the DTI timeslot. A DTI timeslot occupies 1024-master clock (10.24 MHz) periods spanning 1/10 kHz = 100 µs. A bit period consists of two consecutive master clock counts starting with an even count, resulting in 512-bit periods in a DTI timeslot. The timeslot is synchronized to the DOCSIS 32-bit timestamp (DTS), such that the current bit period of a timeslot is the integer, as follows:

current_bit_count = floor[(DTS mod 1024)/2]

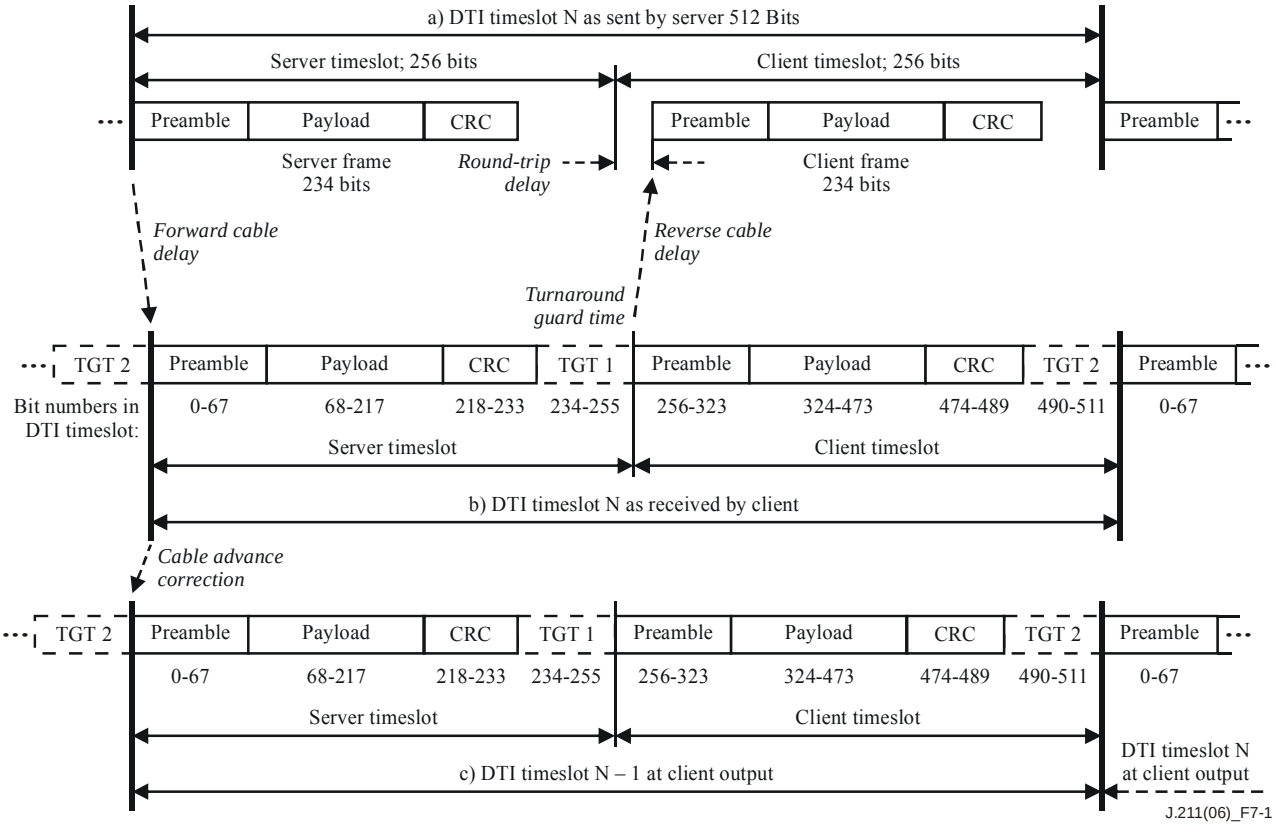


Figure 7-1 – DTI protocol timing structure

The client's received DTI timeslot timing is offset from the server's DTI timeslot timing by the cable propagation delay (plus any group and logic delays). Since the client when in steady state tracks the server, the client counts off a continuous succession of bit slots timed on its own 5.12 MHz-bit clock, repeating DTI timeslots seamlessly modulo 512 bits. The client always receives the first preamble bit from the server in bit slot 0. When it transmits, the client MUST transmit the first bit of its preamble in bit slot 256.

The DTI protocol is ping-pong in nature. The server and client share the line using time division duplexing (TDD), one transmitting while the other receives. The DTI timeslot is divided into two equal intervals: the server timeslot and client timeslot. Layer 2 communication protocol data units (PDUs) are termed "Frames". Both server and client frames are 234 bits in length, and each is followed by a 22-bit turnaround guard time (TGT). The purpose of TGT1, located after the server frame, is to allow time for the client to complete its CRC processing and perform receive/transmit switching on the line after receipt of the server frame. The purpose of TGT2, located after the client frame, is to provide for the round-trip delay of the cable, ensuring that the client frame has been received by the server before the server begins transmitting the next server frame, including time for the server to perform receive/transmit switching on the line after receipt of the client frame. Each TGT provides approximately 4.3 μs of guard time, which well exceeds the maximum round-trip delay for 200 m cable of approximately 2 μs.

At the client output, the DTI frame timing is adjusted earlier in time by the cable advance correction sent by the server, in order to align the client output frame timing closely with the server frame timing. To allow for causality, the data received during the previous frame is buffered and output by the client after the CRC check has completed.

7.3 Traceability of DOCSIS timestamp

Time of coincidence (TOC) is an important concept to understand the relationship of any DTI timestamp (DTS) 32-bit counter to GPS system time. GPS system time began on January 6, 1980. GPS receivers will provide a 32-bit gpssec timestamp that was zero at the January 6 start epoch. The gpssec is a 32-bit timestamp counter that is incremented every second. The DTS is also a 32-bit timestamp counter that is incremented every 10.24-MHz master clock. The objective is to map the current GPS system time to the current DOCSIS timestamp in a coherent manner.

By definition, the DTS can be assigned the value of zero at the same January 6, 1980 start epoch. At the next second, the DOCSIS timestamp will advance 10'000 timeslots with 1024-MHz master clocks per timeslot, so the DTS should be 10'240'000.

The TOC is the next integer gpssec when the DTS will be exactly zero. This will occur every 262'144 seconds (~ every 3 days)[1]. If a reset to zero process were used to synchronize every DTS counter in a server, then it would require up to three days to align a server at start-up. The approach is to generate an initial value for DTS by a mapping function so that the alignment can occur on any one-second boundary.

The mapping function from gpssec to DTS in the DTI server MUST be:

$$DTS = 2 \wedge 10 * [(10'000 * (gpssec \bmod 262144)) \bmod 2 \wedge 22]$$

A client that implements the 10.24-MHz master clock option will use the server DTS directly. A client that implements the 9.216-MHz master clock option will map gpssec to a 9.216-MHz DTI client DTS according to the formula provided in 8.2.

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[1] The gpssec time-scale will roll over every 136 years. Since there are exactly 16'384 TOC events between roll overs, there is no disruption of the DTS.

The four time-of-day setting modes are:

1) GPS;

2) User time set;

3) Default time set;

4) Network timing protocol (NTP) version 4 or greater.

The GPS traceability mode provides the most precise time setting capability. Regardless of the time of day mode, the DTI server MUST convert time of day information to the equivalent gpssec value.

The user time set permits a user to enter an approximate time of day setting through either a local or remote user interface. The default time set operation, if selected, will establish a coarse time of day setting after a reset or power cycle. The time of day is based on the current value of the real time clock in the server.

The NTP time set mode if supported will allow the DTI server to establish a time setting via the NTP protocol as currently configured in the DTI server. If NTP time mode is supported, the DTI server MUST support NTP version 3 or higher.

The DTI server MUST support a means to configure the time of day setting modes of user time set, default time set, NTP or GPS.

7.3.1 GPS frequency mode

In order to provide continuity in the DTI timebase when transitioning from free-run mode or network mode to GPS mode, an intermediate state, "GPS frequency mode", is defined. When the DTI server transitions from free-run or network mode to GPS frequency mode, the DTI server's 10.24-MHz output frequency is adjusted smoothly so as to track the GPS system frequency, while maintaining continuity of the DTI time counters. The system may remain in GPS frequency mode for an extended period of time. If and when the DTI server transitions from GPS frequency mode to GPS mode, the DTI time counters are realigned to GPS time; this may be done in a discontinuous manner during a scheduled maintenance period.

When transitioning from free-run or network mode to GPS mode, the DTI server MUST enter the GPS frequency mode first.

In GPS frequency mode, the DTI server MUST maintain the existing time setting mode and validity state unless changed as a result of user time setting input.

The DTI server MUST support a user input to schedule a transition time from GPS frequency mode to GPS mode.

The DTI server operating in normal lock in GPS frequency mode MUST meet the same MTIE requirements as in GPS mode.

During the transition from free-run to GPS frequency mode normal lock, all DTI server free-run requirements MUST be met.

During the transition from normal lock network to GPS frequency mode normal lock, all DTI server normal lock network MTIE requirements MUST be met.

Under extended GPS holdover conditions, it is possible to enter the degraded MTIE region of performance. The DTI server needs to support a graceful recovery from this state if it should arise. The following requirement applies:

> When recovery from a GPS degraded condition, the DTI server MUST support the ability to slew the frequency to accommodate at least 1 ms of offset over a recovery period of less than 24 hours without exceeding the free-run performance limits.

In user mode and default mode, there are no requirements to adjust the DTI time-scale and ToD output after the initial time setting. The DTI time services are for local use only and not traceable to GPS system time.

If the DTI server supports frequency adjustment of the time-scale in NTP mode, the vendor SHOULD specify the time accuracy performance under vendor-defined NTP configuration(s).

If the DTI server supports frequency adjustment of the time-scale in NTP mode, the DTI server output performance requirements MUST meet the performance requirement of the system operation mode (free-run or network).

If frequency adjustment of the time-scale in NTP mode needs to be suspended to prevent degradation of output, the DTI server MUST report this condition.

If the user requests a transition from user or default time setting to NTP after warm-up, the DTI server MAY reject the request if the transition would degrade the output performance.

7.4 DTI frame structure requirements

The DTI frame structure MUST consist of a preamble followed by the payload and finally by a 16-bit CRC as shown in Figure 7-2. The length of the DTI frame, including the preamble and the CRC MUST be 234 bits. The CRC MUST be calculated only on the payload bits. The rising edge of the 10-kHz DTI frame clock MUST be aligned with the leading edge of the first bit of the preamble of the DTI server. The client digital clock recovery circuit MUST be tolerant to missing clocks since any bit error in the frame will prevent the CRC OK flag in the client CRC checker from being asserted.

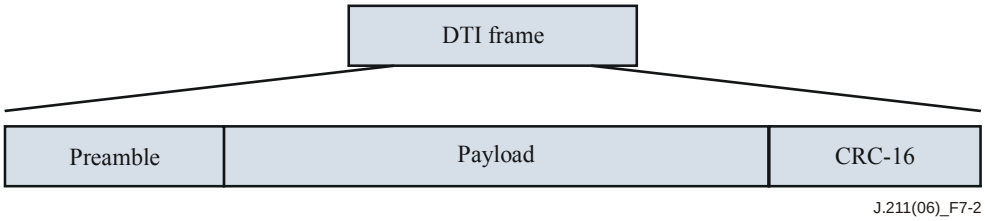


Figure 7-2 – DTI frame structure

7.4.1 Conventions for this Recommendation

In this Recommendation, the following convention applies any time a bit field is displayed in a figure. The bit field should be interpreted by reading the figure from left to right, then from top to bottom, with the MSB being the first bit so read and the LSB being the last bit so read. The DTI frames are transmitted most significant element first. Within bit fields, the most significant bit MUST always be transmitted on the wire first. There are nine bit fields that constitute a frame in each direction. Fields MUST transmit in numerical order from lower to highest value (see Tables 7-1 and 7-2 for field order).

7.4.2 Server to client

The frame structure in the server-to-client direction MUST operate as shown below in Table 7-1.

Table 7-1 – DTI server frame structure

Field	Name	Size (Bits)	Description
1	Preamble	68	Preamble of 0xAAAA AAAA AAAA AAAA 9 prior to Manchester encoding
2	Device type	8	Byte describing type of server
3	Server status flags	8	8 flag bits identifying server status
4	DOCSIS upper timestamp	22	22 most significant bits of the DTS
5	Time of day	10	Field supports serial ToD message over multiple frames
6	Cable advance	24	Integer and fractional cable advance
7	Path traceability field	10	Field supports serial Path Traceability Message over multiple frames
8	Reserved	68	All bits set to "1"
9	CRC-16	16	16-bit CRC which covers all bits except preamble
	Total payload bits	234	

In the server-to-client direction, the DTI frame structure details are as follows.

7.4.2.1 Preamble

The 68-bit preamble is used to align the digital clock recovery circuit on the client and to locate the bit transitions in the Manchester coding that contain information. The pattern "1001" (0x9) at the end of the preamble locates the beginning of the payload.

7.4.2.2 Device type

The 8-bit device type field is used to identify the type of server and its timing source. The bits in this field MUST be assigned as shown below:

Bit 7:5 ***External timing source (for root server)***

000: Server has no external timing source

001: Server is receiving external timing from GPS

010: Server is receiving timing from a network

011-111: Reserved

Bit 4:3 ***Server hop count***

00: Server is the root DTI server for the office distribution

01: Server is directly connected to root DTI server

10-11: Reserved

Bit 2:0 Root server clock type

000: Server clock is ITU type I

001: Server clock is ITU type II

010: Server clock is ITU type III

011: Server clock is ANSI T1.101 ST3 (back-up operation only)

100-111: Reserved

7.4.2.3 Server status flags

This 8-bit field is used to send the server status to a client. The information in this field relates to the DTI server transmitting the DTI protocol. The bits MUST be assigned as shown below:

Bit 7: Reserved

Bit 6: Client performance stable

This bit, when set to "1", indicates that the server verifies the client phase error measurement is within acceptable operating performance.

Bit 5: Cable advance

This bit, when set to "1", indicates that the cable delay has been calculated and that the value in the cable advance field is valid.

Bit 4: Holdover mode

This bit, when set to "1", indicates that the server has lost its timing reference and is in holdover.

Bit 3: Normal mode

This bit, when set to "1", indicates that the clock is stable, has locked on to the timing reference, and is compliant with the appropriate clock standard.

Bit 2: Fast mode

This bit, when set to "1", indicates that the clock is using a short time constant. A shorter time constant is used in the clock circuit to shorten the initial lock time when the server first powers up or receives a reference for the first time.

Bit 1: Free-run mode

This bit, when set to "1", indicates that the server is operating with output frequency that has not been influenced by local external reference signals.

Bit 0: Warm-up

This bit is set to "1" to indicate that the reference oscillator has not stabilized yet.

7.4.2.4 DOCSIS upper timestamp

These 22 bits MUST contain the most significant portion of the DOCSIS 32-bit timestamp, which is the portion of the timestamp that remains constant for an entire DTI frame period (1/10 kHz = 100 μs). These bits are used to load and/or monitor the upper 22 bits of the 32-bit DOCSIS timestamp counter in the client. The 10 least significant bits of the DOCSIS timestamp counter in the client represent the number of 10.24-MHz clocks since the beginning of the DTI frame. Together, these two fields create the entire 32-bit DOCSIS timestamp.

7.4.2.5 Time of day

The time of day (ToD) message provides time in binary format and optionally in ASCII format, each with 1-second resolution. The gpssec time and leap second are sent in binary format. When in verbose mode, calendar time in ASCII format is also sent, including a modified Julian date and

local date/time information. The ToD message is transmitted at a rate of 10 bits (one byte of payload and two control bits) per DTI frame, and is subcommutated to span multiple DTI frames. The first control bit indicates that the location of the pulse per second will be coincident with the beginning of the next frame. The second control bit is a data valid flag which applies to the payload byte. The data valid flag may be used to stop and start the subcommutated byte stream. When the data valid flag is 0, the payload byte MUST contain all ones. When the data valid flag, is 1, the payload byte MUST contain the next serial byte in the ToD message. The ToD message corresponding to a given pulse-per-second (PPS) count MUST start transmission one or more frames after the frame where the PPS flag bit has been set, and complete transmission within 100 ms. The bit assignments for the 10-bit ToD message field in each DTI frame MUST be as follows:

Bit 9: PPS flag

This bit MUST be set to '1' when the beginning of the next frame is coincident with the DTI server pulse per second[2]. The asserted "1" indicates that the next DTI server frame PPS flag position bit is the on-time mark for PPS information just transferred during the last one-second period. This on-time frame MUST contain byte one of the ToD message. The PPS flag bit is asserted in every 10'000th frame.

Bit 8: Data valid bit

This bit is set to '1' to indicate that the data in the payload byte (following eight bits) contains valid data.

Bit 7-0:

This field contains the subcommutated ToD payload byte, which MUST be in accordance with Table 7-2.

Table 7-2 – ToD subcommutated message format

Byte number	Length	Type	Format	Name	Description
1	1	Binary	See ToD status field description in 7.4.2.6	ToD status	
2-5	4	Binary		gpssec	32-bit gpssec timestamp
6	1	Binary		Leap seconds	Cumulative leap seconds between gpssec and UTC
7	1	7-bit ASCII	ASCII "*" (0x2A) denotes Valid ToD Calendar Time ASCII "!" (0x21) denotes Invalid ToD Calendar Time	ToD calendar time valid	
8-12	5	7-bit ASCII	MMMMM Where M is [0-9] ASCII	MJD	Modified Julian date (number of days since November 17, 1958)
13	1	7-bit ASCII	ASCII decimal point "." (0x2E)		

[2] The Pulse Per Second is free-running except in GPS mode where it is aligned to the GPS 1PPS.

Table 7-2 – ToD subcommutated message format

Byte number	Length	Type	Format	Name	Description
14-23	10	7-bit ASCII	Year/Month/Day Year: [0000-9999] Month: [1-12] Day: [1-31]	Date	Local date
24	1	7-bit ASCII	ASCII decimal point "." (0x2E)		
25-32	8	7-bit ASCII	Hour: Min:Sec Hour: [00-23] Min: [00-59] Sec: [00-60][a)]	Time	Local time
33	1	7-bit ASCII	ASCII decimal point "." (0x2E)		
34:38	5	7-bit ASCII	SHH.F S: sign [+, –] H: offset in hours F: [0] or ([5] for 30-minute offsets)	Time zone offset	Local time zone offset
39	1	7-bit ASCII	ASCII decimal point "." (0x2E)		
40	1	7-bit ASCII	ASCII "D" (0x43)	Leap second indicator	
41	1	7-bit ASCII	ASCII carriage return (0x0D)		
[a)] 60-second indicator may be used to indicate a leap second.					

7.4.2.6 ToD status field

This 8-bit field is used to report the status of the Time Of Day Message. The bits in the ToD status field MUST be assigned as shown below:

Bit 7:4: ***Time setting mode***

0000: Default Time Setting Mode

0001: User Time Setting Mode

0010: NTP Time Setting Mode

0011: GPS Time Setting Mode

0100-1111: Reserved

Bit 3:2: ***ToD state***

00: ToD is currently not valid

01: ToD is valid

10-11: Reserved

Bit 1:0: ToD message mode

00: Short Message Mode. Message bytes 0-5 (binary only)

01: Verbose Message Mode: Message includes all fields in Table 7-2

10-11: Reserved

The DTI server MUST support the Short Message Mode for ToD delivery.

The Verbose Message Mode SHOULD be supported by the DTI server.

If more than one ToD message mode is supported, the default MUST be the Short Message Mode.

If more than one ToD message mode is supported, the mode SHOULD be configurable on a port basis.

7.4.2.7 Cable advance

Cable advance is described in 8.1.2. The cable advance information MUST be contained in this 24-bit field. The 16 most significant bits of the cable advance MUST contain the integer portion of the cable advance value that is in 149.8-MHz[3] sample clock cycles. The remaining 8 bits, the least significant byte of the cable advance, MUST be the fractional portion of the cable advance and is in 1/256 of a 149.8-MHz clock cycle.

7.4.2.8 Path traceability field

The path traceability field is a 10-bit field that MUST be used to send byte-oriented data to the client. The path traceability field MUST be filled as follows:

Bit 9: Start of message

The path traceability field start of message bit MUST be set high for one frame to indicate the beginning of a status message.

Bit 8: Data valid bit

The path traceability field data valid bit MUST be set to '1' to indicate that the next eight data bits contain valid data. When the path traceability field data valid bit is '0', the client MUST ignore the contents of the eight data bits that follow.

Bit 7:0: Data byte

This data byte MUST contain the serial message data bytes.

Table 7-3 – Path traceability message format

Name	Type (1 byte)	Length (1 byte)	Value (variable length)
Root DTI server IPv4 address	1	4	IP address of root DTI server (highest level in tree)
Root DTI server output port #	2	1	Root server output port number for this DTI interface. Output port number counting starts at 0 and goes through 255.
DTI server IPv4 address (if not root server)	3	4	IP address of DTI server source DTI interface (if not root server)
DTI server output port #	4	1	Server output port number for this DTI interface. Ports start counting at 0 and continue to 255.
Root DTI server IPv6 address	5	16	IP address of root DTI server (highest level in tree)

[3] The 149.8-MHz high-speed clock is more precisely 10.24 MHz * 512/35.

Table 7-3 – Path traceability message format

Name	Type (1 byte)	Length (1 byte)	Value (variable length)
DTI server IPv6 address (if not root server)	6	16	IP address of root DTI server (highest level in tree)
Root DTI server DTI version (Note)	7	1	DTI version number running on root server
DTI server DTI version	8	1	DTI version number running on DTI server (if not root server)
EOT	9	1	0x00 The EOT identifies the end of the path traceability field.
NOTE – For DTI servers compliant with the first release of this Recommendation, this value shall be zero.			

If there is a subtending DTI server, the root DTI server address MUST be passed through the subtending DTI server to DTI clients. In other words, a DTI client connected to a root server through an intermediate server will have both a Root Server IP address and a Server IP address in the path traceability field. The root server MUST not transmit the non-root IP information. The path traceability field MUST follow the Type, Length, and Value sequence, as shown below, and follows the bit/byte ordering already defined.

Type	Length	Value	Type	Length	Value

7.4.2.9 Reserved

The remaining 68 bits MUST be reserved for future use. They will be filled with '1's until defined otherwise.

7.4.2.10 CRC-16

The CRC-16 field MUST contain the 16-bit CRC-16 cyclic redundancy check. The CRC-16 generator MUST be initialized with '1's during the preamble bits. After the last bit of the preamble, the payload data MUST be shifted through the CRC-16 code generator. Following the last bit of the payload, the serial output MUST be switched from the transmit shift register to the output of the CRC-16 generator and 16 more '1's MUST be shifted through the generator to shift out the 16-bit CRC. The generator polynomial MUST be x^16 + x^12 + x^5 + 1, which is the ITU-T CRC-16 generator polynomial.

The leading edge of the first bit location following the CRC MUST coincide with the rising edge of the 10-kHz receive frame clock.

7.4.3 Client to server

The frame structure for the client-to-server direction MUST operate as shown below in Table 7-4.

Table 7-4 – DTI client frame structure

Field	Name	Size	Description
1	Preamble	68	Preamble of 0xAAAA AAAA AAAA AAAA 6 prior to Manchester encoding
2	Device type	8	Byte describing type of client
3	Client status flags	8	8 flag bits identifying client status
4	Reserved	22	Not used set to one
5	Reserved	10	Not used set to one
6	Client clock integrated phase	24	16-bit 2-complement value of the local frame clock
7	Client DTI Version	10	Client DTI version number
8	Reserved	68	All bits set to one
9	CRC-16	16	16-bit CRC which covers all bits except preamble
	Total payload bits	234	

In the client to server direction the DTI frame structure details are shown below:

7.4.3.1 Preamble

The 68-bit preamble is used to align the clock recovery circuit on the server and to locate the bit transitions in the Manchester coding that contain information. The pattern "0110" (0x6) at the end of the preamble locates the beginning of the payload.

7.4.3.2 Device type

The 8-bit device type field is used to identify the type of client and its timing source. The bits in the device type MUST be defined as follows:

Bit 7:4: Timing source

Timing source does not have to be reported to the server.

These bits are reserved and will be filled with '1's.

Bit 3:0: Client clock type

0000: Client oscillator is an ITU type 1

0001: Client oscillator is an ITU type 2

0010: Client oscillator is an ITU type 3

0011: Client oscillator is an ITU Stratum 3

0100: Client oscillator is a DTI Minimum Clock oscillator

0101-1111: Reserved

7.4.3.3 Client status flags

This 8-bit field is used to send the client status to a server. The client status flag bits MUST be defined as follows:

Bits 6 & 7: Reserved for future use

Bit 5: Bridging mode

This bit, when set to '1', indicates that the client has lost its timing reference and is maintaining acceptable performance.

Bit 4: Holdover mode

This bit, when set to '1', indicates that the client has lost its timing reference and is in holdover.

Bit 3: Normal mode

This bit, when set to '1', indicates that the clock is stable, has locked on to the timing reference, and is compliant with the appropriate clock standard.

Bit 2: Fast mode

This bit, when set to '1', indicates that the clock is using a short time constant. A shorter time constant can be used in the clock circuit to reduce the initial lock time when the client first powers up or receives a reference for the first time.

Bit 1: Free-run mode

This bit, when set to '1', indicates that the client is operating with output frequency that has not been influenced by a client or DTI server.

Bit 0: Warm-up

This bit when set to '1' indicates that the client oscillator has not stabilized yet.

7.4.3.4 Client clock integer phase error

This 24-bit field MUST return a snapshot of the client phase error. The value will be in units of 149.8-MHz sample clock cycles and will reside in the 16 most significant bits. The lower eight bits of the 24-bit field MUST be padded with zeros and MUST NOT be used by the DTI server. The value MUST be a signed 2's complement number. If the DTI client supports more bits of resolution, the DTI client MUST round the reported value to the nearest integer sample clock cycle.

7.4.3.5 Client DTI version

This 10-bit field MUST report the current DTI protocol version supported by the client expressed as an unsigned integer. For the first release, this value MUST be zero.

7.4.3.6 Reserved

The remaining 68 bits MUST be reserved for future use. They will be filled with '1's until defined otherwise.

7.4.3.7 CRC-16

This 16-bit field MUST contain the CRC-16 cyclic redundancy check. The CRC-16 generator MUST be initialized with '1's during the preamble bits. After the last bit of the preamble, the payload data MUST be shifted through the CRC-16 code generator. Following the last bit of the payload, the serial output MUST be switched from the transmit shift register to the output of the CRC-16 generator and 16 more '1s' MUST be shifted through the generator to shift out the 16-bit CRC. The generator polynomial MUST be x^16 + x^12 + x^5 + 1.

7.5 DTI server-client protocol interaction

The following protocol exchange diagram (Figure 7-3) will be used to illustrate the protocol rule set. Specific requirements relative to server and client operation supporting the protocol are delineated in clause 8.

The exchange starts with both the server and client inactive (powered down). The first step is server warm-up. The principal sub-system requiring warm-up in a DTI server is the local oscillator. During warm-up, a server is transmitting DTI messages, with the warm-up state indicated. The server will stay in the warm-up state until the oscillator is stable and a stable time-of-day setting is acquired. The server transitions to the free-run state and will persist in this state until locked to an external reference. Figure 7-3 illustrates the client power-up occurring during timeslot M. The client will not transmit until loss of receive frame condition has cleared (see 8.2.3). During timeslot M, the DTI server enters the normal condition as shown. The next server frame indicates this normal condition in the service status flags. Note that the client can begin locking, using valid server frames as soon as the server is out of warm-up, establish a time-of-day setting, and is actively transmitting. Assuming that the client has established receive framing and it receives the current frame with a valid CRC, it responds with a client frame in timeslot M+1. The client clock is assumed to be in warm-up at this time, as reflected in the client status flag lock, set to invalid. At timeslot M+2, the server can begin to process the client frame by measuring round-trip delay, as well as collect the client clock phase error measurement data returned in the client frame.

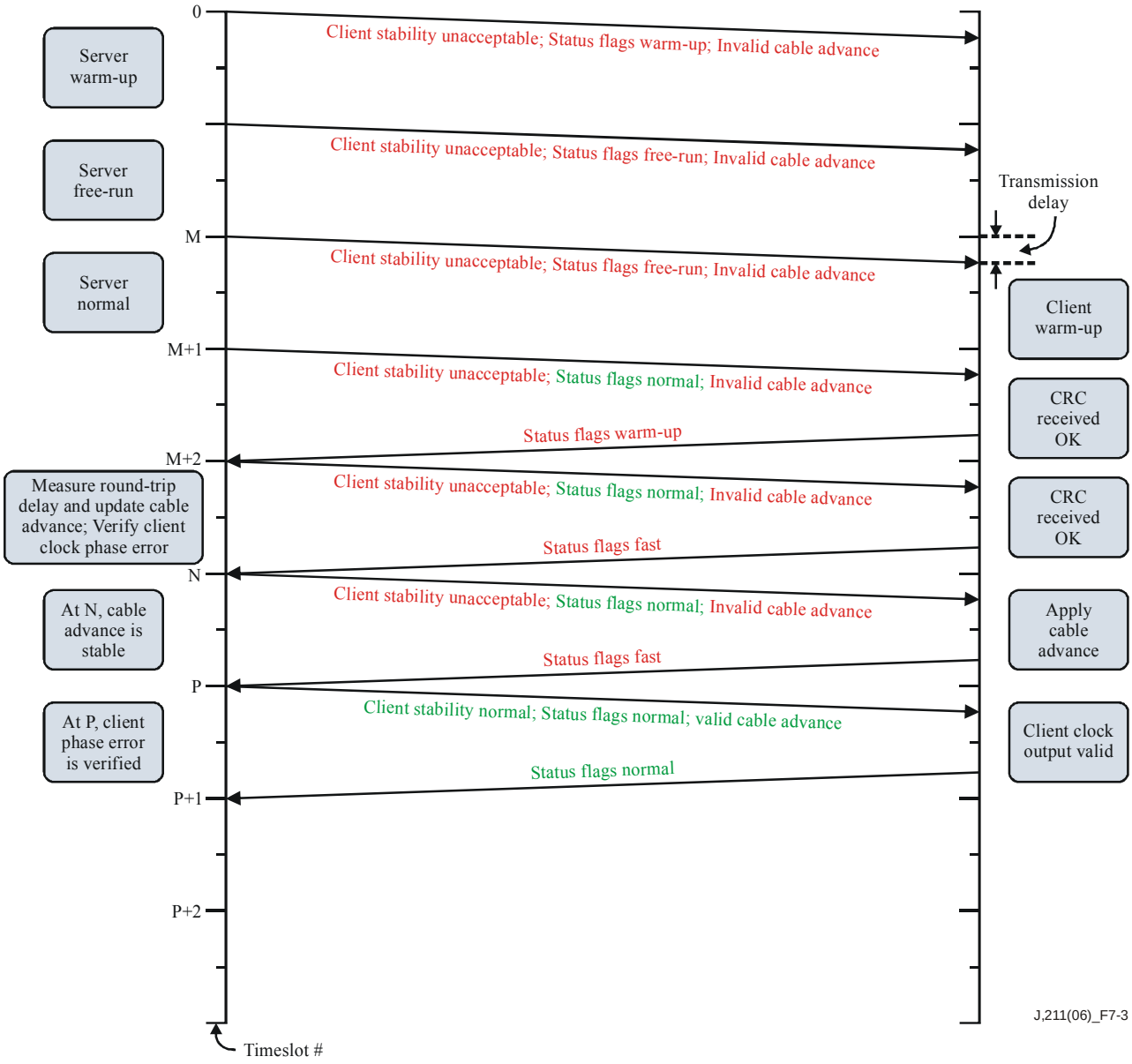


Figure 7-3 – Example of DTI server-client protocol

The server filters the round-trip measurement data to establish a stable cable advance correction that will not degrade the timing performance of the client clock. Figure 7-3 illustrates the server achieving stable cable advance just prior to timeslot P. At timeslot P the server transmit frame indicates this by setting the cable advance flag to valid. During the same timeslot, the client clock is assumed to achieve a local phase lock and the client message indicates fast mode. Finally, just prior to timeslot P+1 the server has verified, using the client clock phase error data since timeslot M+1, that the client is in proper phase lock with respect to master clock and reports this at P+1 by setting the client stability condition flag to "valid".

8 DTI client and server operation

See clause 1.1 for an informational description of the DTI protocol.

8.1 DTI server modes

The DTI server can support three modes of operation:

1) Free-running master: No external source is provided to control frequency or timestamp accuracy.
2) GPS traceable: Source of timestamp and frequency traceability is GPS.
3) Network traceable: A standard network PDH, SONET or SDH interface is used to provide traceability to a Stratum 1 frequency reference.

In M-CMTS, deployment where all the elements are collocated GPS traceability is not required.

The DTI server MUST support the free-running master clock mode. In this mode, no external sources of traceability are required.

The DTI server MAY support the GPS-traceable mode of operation.

The DTI server MAY support the network-traceable mode of operation.

8.1.1 Free-running master mode

The free-running master clock requirements are related closely to the existing DOCSIS clocking requirements, with additional margin included to ensure the DTI client master clock output performance meets all requirements.

To support common tracking of all downstream elements including DTI clients, the free-running master mode MUST limit output frequency slew rate to less than 10^{-9} over a ten-second period.

The free-running master mode output frequency accuracy MUST be better than 1 ppm over a temperature range of 0° to 40°C for up to 10 years from the date of manufacturer.

The DTI server high-frequency jitter (above 10 Hz) in free-running master mode MUST be less than 50 ps RMS.

The DTI server ranging wander when observed through the ranging wander qualification filter[4] MUST be less than 250 ps RMS.

DTI server port-to-port performance applies to ports on a single root server or ports between a root server and a subtending server. The DTI server port-to-port ranging wander when observed through the ranging wander qualification filter MUST be less than 125 ps RMS.

8.1.2 External reference modes

8.1.2.1 Common synchronization performance requirements

NOTE – The requirements in this clause do not apply in free-run master mode.

8.1.2.1.1 DTI server holdover performance

To maintain compatibility with the TDM service synchronization hierarchy, the DTI server clock MUST operate with holdover performance in one of the categories specified in Table 8-1. These categories are consistent with controlling standards for existing TDM services [ITU-T G.812] and [T1.101].

[4] The ranging wander measurement filter is described in Appendix IV.

Table 8-1 – DTI server holdover requirements

ITU-T G.812 type	ANSI T1.101-1999 stratum level	Holdover aging allowance (ppb per day) (Note 1)	Holdover temperature allowance ppb (Note 2)	24-hour holdover total allocation (aging and temperature) ppb
Type I	NA	0.2	2.0	2.2
Type II	Stratum 2	NA	NA	0.1
Type III	Stratum 3E	1.0	10.0	11.0
NOTE 1 – Represents the average frequency drift caused by aging. This value is derived from typical aging characteristics after 60 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate. NOTE 2 – Operating temperature conditions are in the range of 0° to 40°C ambient at a maximum rate of 10°C per hour.				

8.1.2.1.2 DTI server slew rate performance

The DTI server needs to constrain the phase slew rate during the 35 seconds of the DOCSIS maximum ranging interval. The DTI Server MUST maintain a phase slew rate of 5 ns over a ten-second period during normal and acceptable operation.

8.1.2.1.3 DTI server timing jitter performance

The DTI server ranging timing wander over a 35-second period with the mean subtracted needs to be allocated as part of the 1-ns RMS requirement for chip timing jitter for synchronous operation as discussed in Appendix III. Two collocated servers supporting two clients and the associated PHY components need to be considered in the overall budget. The following requirements support a 400-ps RMS allocation of the 1-ns RMS requirement to the DTI components.

- The DTI server high frequency jitter (above 10 Hz) in free-running master mode MUST be less than 50 ps RMS.
- The DTI server ranging wander when observed through the ranging wander bandpass filter MUST be less than 250 ps RMS.
- DTI server port-to-port performance applies to ports on a single root server or ports between a root server and a subtending server. The DTI server port-to-port ranging wander when observed through the ranging wander qualification filter MUST be less than 125 ps RMS.

8.1.2.2 GPS traceable

The DTI server is required to support both DOCSIS system timing requirements as well as the synchronization timing requirements of the TDM services that may need to be supported. With the modular CMTS architecture, DTI elements such as upstream receivers, EQAMs, and M-CMTS-cores may be in different nodes or buildings. The DTI servers in different buildings MUST operate with sufficient coherence to support all time- and frequency-dependent functions particularly ranging, latency management and TDM service synchronization when operating in GPS mode.

The DTI server MUST operate within the maximum time interval requirements specified in Figure 8-1 in GPS-traceable mode. Figure 8-1 defines three levels of server operation:

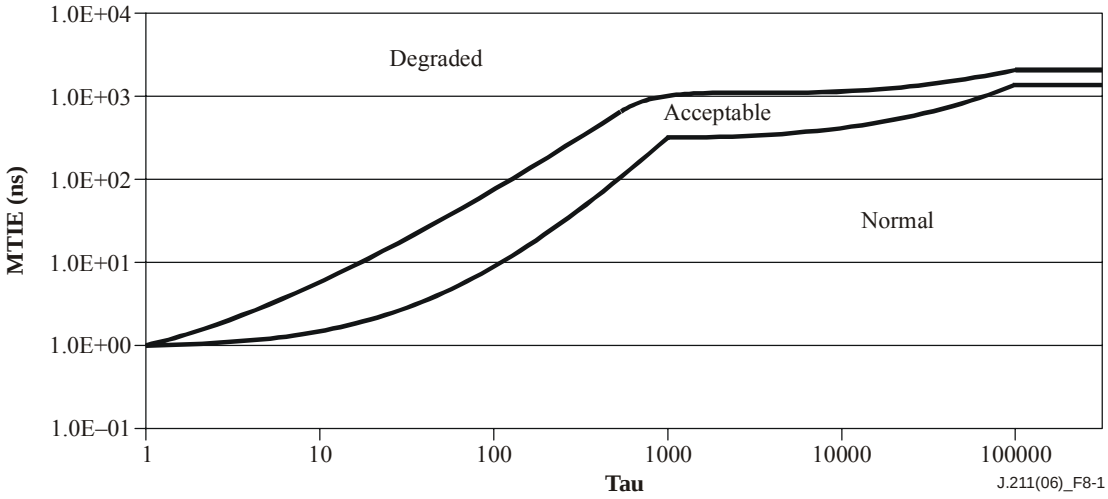
1) Normal – This is the performance level anticipated under the normal operating environment. While the server should operate over the full environmental requirements specified by the MSO, it is recommended that the vendor document the environmental limits such as limited temperature slew associated with normal operation. Normal operation does not include loss of all external references.

2) Acceptable – This is the performance level the server MUST meet over the full environmental requirements specified by the MSO. The server MUST meet this level of MTIE over limited outage periods of the input references. It is recommended that the vendor document the outage periods that can be supported.

3) Degraded – The server MUST NOT enter the degraded level of operation unless there is an extended duration outage beyond the vendor-specified limit or the environmental limits are exceeded.

Additionally, the following operating conditions apply for normal and acceptable service levels:

- The maximum ambient temperature slew rate is less than 10°C per hour.
- If there is more than one valid input, a reference switch from one valid input to another is considered normal and acceptable.
- The DTI server is not operating in warm-up or free-run.
- The DTI server has been continuously powered for at least one hour.



MTIE acceptable operating limits

Observation time, τ (seconds)	MTIE (nanoseconds)
$0.1 \le \tau < 1000$	$.5 + .5 * \tau + .00201 * \tau^2 – 1.51e\text{-}6 * \tau^3$
$280 \le \tau < 100{,}000$	$0.01 * \tau + 1000$
$100{,}000 \le \tau < 500{,}000$	2000

MTIE normal operating limits

Observation time, τ (seconds)	MTIE (nanoseconds)
$0.1 \le \tau < 1000$	$.95 + .05 * \tau + .00026 * \tau^2$
$1000 \le \tau < 100{,}000$	$0.01 * \tau + 300$
$100{,}000 \le \tau < 500{,}000$	1290

Figure 8-1 – GPS-traceable mode MTIE requirements

When the GPS-traceable DTI server is required to operate with a second GPS-traceable server in a different location, the time error of the DTI server master clock with respect to UTC frequency reference[5] over a 35-second time window with the mean subtracted MUST be less than 300 ps RMS under normal operating conditions.

8.1.2.3 Network-traceable mode

The network mode of operation utilizes synchronization embedded on PDH, SONET, and SDH physical layer and framing to provide frequency traceability to a Stratum 1 network clock. Synchronization traceability can potentially be delivered by:

- a plesiochronous digital network (PDH) DS1 signal that is a traffic-bearing signal: A traffic-bearing signal is either traceability to a Stratum 1 clock within the transport network or stratum-traceable source from the remote terminating equipment. The wander and jitter requirements are less stringent than the synchronization-bearing mode described in the next paragraph. In addition, a traffic-bearing interface may incur transients associated with SONET or SDH pointer adjustment events;
- a PDH signal that is a synchronization-bearing signal: A synchronization-bearing signal is traceable to a Stratum 1 clock within a transport network and is required to meet tighter wander and jitter bounds;
- a SONET/SDH signal from a traceable network element: SONET/SDH networks are required to be synchronous and supplied the traceable synchronization from a synchronization port on the terminating equipment. The derived synchronization interface port can support synchronization status message to provide a level of verification.

The network mode of operation SHOULD NOT utilize references operating at the traffic-bearing performance limits as specified in [ITU-T G.824]. Vendors MAY support filtering of traffic-bearing signals but this operation is beyond the scope of this Recommendation.

The network mode provides precise frequency (rate) synchronization but not precise time synchronization. When the signal is used with a properly designed filter clock in a DTI sever, the output DTI timing signals will support all M-CMTS requirements when all the DOCSIS elements are collocated. The network mode (as well as the GPS mode) will also enable delivery of synchronization required for commercial T1 services.

The DTI server MUST meet the output MTIE and common synchronization requirements under both normal and acceptable input conditions (see 8.1.2.3.1).

8.1.2.3.1 Normal and acceptable input conditions

Normal and acceptable input conditions are defined as follows:

- The maximum input jitter is less than 3.24 microseconds peak-to-peak from 10 Hz to 40 kHz.
- The maximum input wander is limited to the MTIE mask in Figure 8-2.
- The maximum ambient temperature slew rate is less than 10°C per hour.
- If there is more than one valid input, a reference switch from one valid input to another is considered normal and acceptable.
- The DTI server is not operating in warm-up or free-run.
- The DTI server has been continuously powered for at least one hour.

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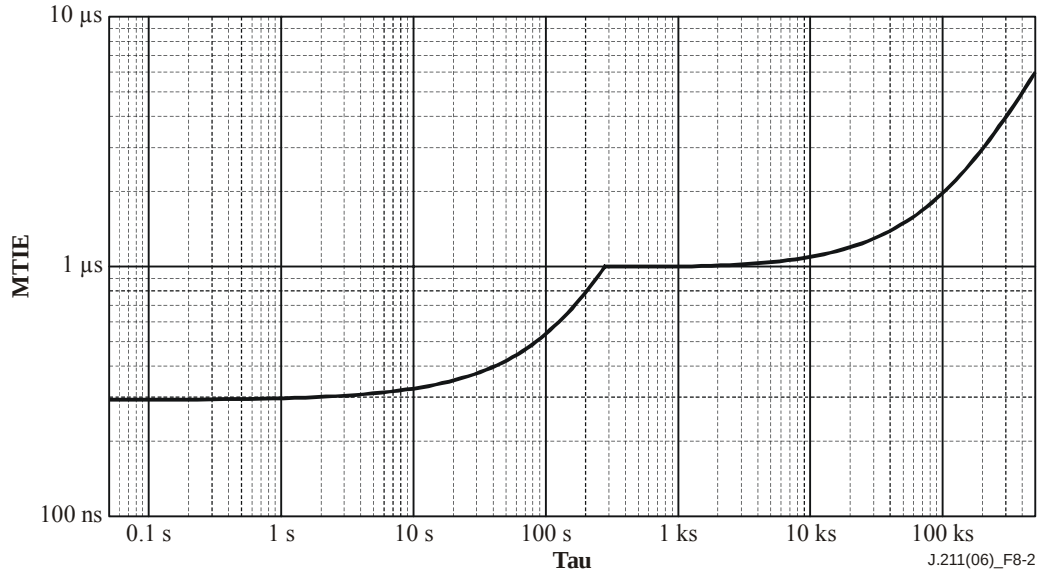
[5] In practice, a cesium reference clock or equivalent may be used to approximate a UTC frequency reference.

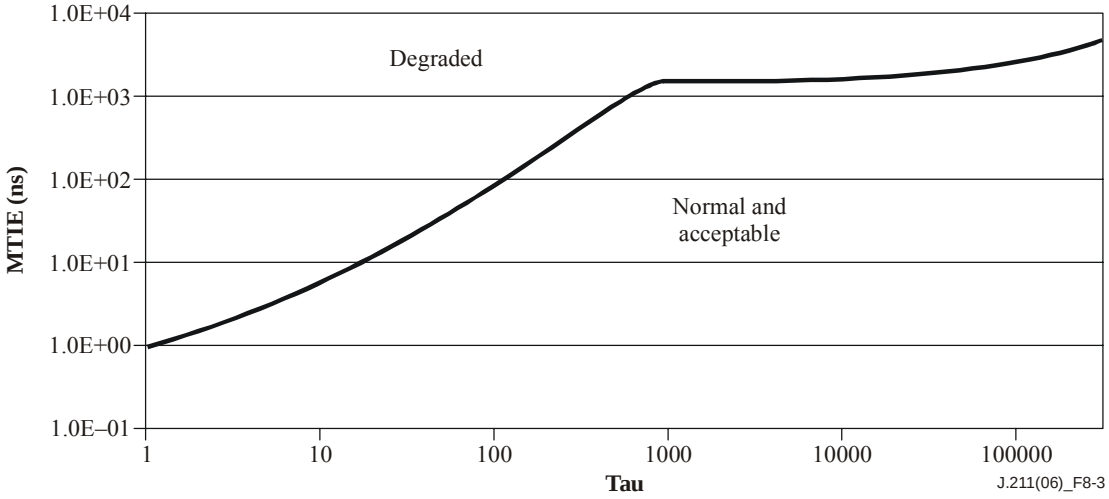


MTIE synchronization-bearing input reference	
Observation time, τ (seconds)	MTIE (nanoseconds)
$0.1 \leq \tau < 280$	$2.5 * \tau + 300$
$280 \leq \tau$	$0.01 * \tau + 997$

Figure 8-2 – Network input MTIE requirements

8.1.2.3.2 Network-traceable MTIE performance requirements

The DTI server MUST meet the normal and acceptable MTIE performance requirements in Figure 8-3 under the input conditions stipulated in clause 8.1.2.3.1.



MTIE network traceable performance requirements	
Observation time, τ (seconds)	MTIE (nanoseconds)
$0.05 \leq \tau < 1000$	$.5 + .5 * \tau + .00335 * \tau^2 - 2.35e\text{-}6 * \tau^3$
$1000 \leq \tau$	$0.01 * \tau + 1490$

Figure 8-3 – Network-traceable mode MTIE requirements

8.1.3 DTI server functional requirements

The server clock MUST support the clock fast mode, clock free-run mode, clock holdover mode and clock normal mode, as defined in [T1.101].

During warm-up, a server MUST transmit DTI messages with the client performance stable flag and the cable advance flag set to "false".

The DTI server MUST NOT exit warm-up until it has established an initial time-of-day setting.

Until a stable cable advance correction is established, the server MUST indicate an invalid cable advance in the server status flags.

Under normal operating conditions with a properly functioning client clock and a normal transport bit error rate (BER) ($<10^{-8}$), the server MUST establish a stable cable advance within 20 seconds from the first valid client response.

The DTI server MUST support both manual and automatic modes for cable advance.

The DTI server cable advance mode MUST be settable on a per port basis.

Regardless of the cable advance mode, the DTI server MUST minimize changes in the cable advance value once the stable cable advance flag is asserted to ensure that all DTI server performance requirements are met.

In manual cable advance mode, the cable advance correction value MUST be unchanged unless an update is requested by the user. Transitioning from automatic mode to manual mode MUST freeze the current cable advance value. Transitioning from manual mode to automatic mode MUST resume automatic adjustment starting from the current cable advance value.

In automatic cable advance mode, the DTI server MUST automatically adjust the cable advance to slow changes in the cable delay associated with normal environmental conditions.

In automatic cable advance mode under stable cable advance operation (server status cable advance flag = 1), the rate of change of the cable advance MUST be no more than one LSB of the fractional cable advance word (26 ps) per second.

The DTI server MAY provide an option to set the cable advance to a user selectable value under manual cable advance mode.

When switching from a working DTI server to a protection DTI server in a common shelf, the DTI output signal MUST be active within 500 ms.

Under normal operating conditions with a properly functioning client clock, a normal transport BER ($<10^{-8}$), a protection DTI server that has just become active MUST establish a stable cable advance within 1000 ms from the first valid client response.

8.1.4 DTI server test signal mode

The DTI server MUST support a test mode for each output port of the server. The test signal MUST be a continuous stream of all "ones" prior to Manchester encoding. The measurement of phase bias requires accounting for the group delay in any common path elements between the output port connector and the point where the transmit and receive paths split within the server. The delay bias measurement should be referenced to this transmit receive split point.

The DTI server MUST support a 10.24-MHz master clock test port. This port MUST be phase accurate with less than 2500-ps bias when compared to normal DTI server ports. The master clock test port output jitter MUST be less than 25 ps RMS.

The DTI server MUST support a 10-kHz master frame clock test port. This port MUST be phase accurate with less than 2500-ps bias when compared to normal DTI server ports. The master frame clock test port output jitter MUST be less than 50 ps RMS.

8.2 DTI client operation

The DTI client is located within a host M-CMTS device, such as an EQAM, US receiver or M-CMTS-Core (see Figure 8-4). The function of the DTI client is to interface with the DTI server using the DTI protocol, and to provide time, frequency and management interfaces to the M-CMTS device.

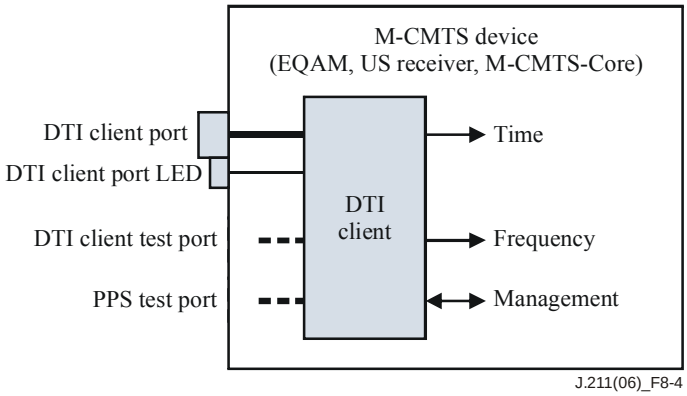


Figure 8-4 – DTI client system interface

Since the DTI client is likely to be integrated into the M-CMTS device, the internal time, frequency and management interfaces may be proprietary, and as such are not defined by this Recommendation. The test port requirements specified herein are intended to verify the performance of the corresponding operational signals.

At an M-CMTS entity (e.g., M-CMTS-Core or EQAM), the difference between the time communicated via the DTI client test port output and the time reference used by an M-CMTS entity is to be minimized and is to be no greater than 1 µs. For example, the timestamps within SYNC messages transmitted by an EQAM should reflect a timebase that differs from the time communicated via the DTI client test port output by no more than 1 µs. As another example, the upstream receiver within the CMTS-Core should perform ranging based on a time reference that also differs from the time communicated via the DTI Client Test Port output by no more than 1 µs.

DTI clients residing in EQAM, US Receiver and M-CMTS-CORE M-CMTS devices:

- MUST provide a DTI client port;
- MUST provide a DTI status LED;
- MUST employ a one-sided 3-dB loop filter bandwidth in the range of 1-10 Hz to track the DTI server timing;
- MUST support a pull-in range capable of locking to a properly functioning server over normal operating conditions, as specified in clause 8.2.1, for a period of 10 years from date of manufacturer.

DTI clients residing in US receiver and M-CMTS-CORE M-CMTS devices MUST provide a DTI client test port.

DTI clients residing in EQAM M-CMTS Devices MAY provide a DTI client test port.

DTI clients residing in M-CMTS EQAM devices that do not provide a DTI client test port MUST provide a PPS test port and support verification of DTI client operation as per clause 6.

Since the DTI client test port, and the EQAM DTI test port, are not required for normal operation, it may be necessary to remove panels or covers on the M-CMTS device in order to access these ports.

To support regional differences in DOCSIS master clock frequency, this Recommendation includes two DTI client master clock output options. The DTI client MUST support one of the following master clock output options:

1) 10.24 MHz;

2) 9.216 MHz.

A clock interworking function is responsible for generating the client output signals, and allows DTI clients supporting either master clock frequency option to operate with a common DTI server and DTI layer 1 and layer 2 protocols.

For the 10.24-MHz option, the clock interworking function produces a master clock and DTS that are a replica of the DTI server master clock and DTS. The clock interworking function requires no translation of the master clock frequency and DTS.

For the 9.216-MHz option, the clock interworking function produces a master clock and DTS that are a translation of the DTI server master clock and gpssec. When the 9.216-MHz master clock frequency option is used, the client MUST generate a 32-bit counter based on the 9.216-MHz clock and the following relationship with the current gpssec.

9.216 DTI client DTS = 2^13*[(1125*(gpssec mod 2^19)) mod 2^19]

An example of both the 10.24-MHz and 9.216-MHz clients is provided in Appendix II.

8.2.1 DTI normal operating conditions

The DTI client MUST meet all specifications when under normal operating conditions defined as:

- the ambient temperature range is between 0 to 40° C;
- the maximum ambient temperature slew rate is less than 10°C per hour;
- the DTI transport BER is less than 10^{-8};
- the cable length is between zero and 200 metres and is operating in compliance with clause 6.

8.2.2 DTI client operational modes

The DTI client MUST support and report the operational modes described in Table 8-2.

Table 8-2 – Client operating states

Mode	Description
Warm-up	Oscillator has not yet stabilized.
Free-run	Client has not had a valid timing source since reset, or has had to abort acquisition.
Fast	Client is using a short acquisition time constant so as to reduce the initial lock time.
Normal	Clock is stable, has locked on to the timing reference, and is fully compliant.
Bridging	Client has lost its timing reference but is maintaining acceptable performance.
Holdover	Client has lost its timing reference but is attempting to maintain last valid frequency.

8.2.3 DTI client mode transition diagram

The DTI client MUST implement mode transition similar to those described in Table 8-3 and shown in Figure 8-5.

Table 8-3 – Client mode transitions

Transition	From	To	Condition for transition	Comment
T1	Warm-up	Free-run	Vendor-specific timeout. (Timeout less than 20 ms)	Allows sufficient time for oscillator to stabilize.
T2	Free-run	Fast	FER ≤ 0.02 over 50 ms	Sufficient number of valid frames from server
T3	Fast	Free-run	FER ≥ 0.05 over 50 ms	Acquisition aborted
T4	Fast	Normal	'FER ≤ 0.02 over 50 ms' & 'Client Performance Stable' & 'Cable Advance' = TRUE	Acquisition complete
T5	Normal	Bridging	FER ≥ 0.5 over 50 ms	Insufficient number of valid frames from server
T6	Bridging	Normal	'FER ≤ 0.02 over 50 ms' & 'Client Performance Stable' & 'Cable Advance' = TRUE	
T7	Bridging	Holdover	2-second timeout	
T8	Holdover	Fast	FER ≤ 0.02 over 50 ms	Sufficient number of valid frames from server

With a valid server connected, and under normal operating conditions, the DTI client MUST transition from free-run to normal within a period of 20 seconds.

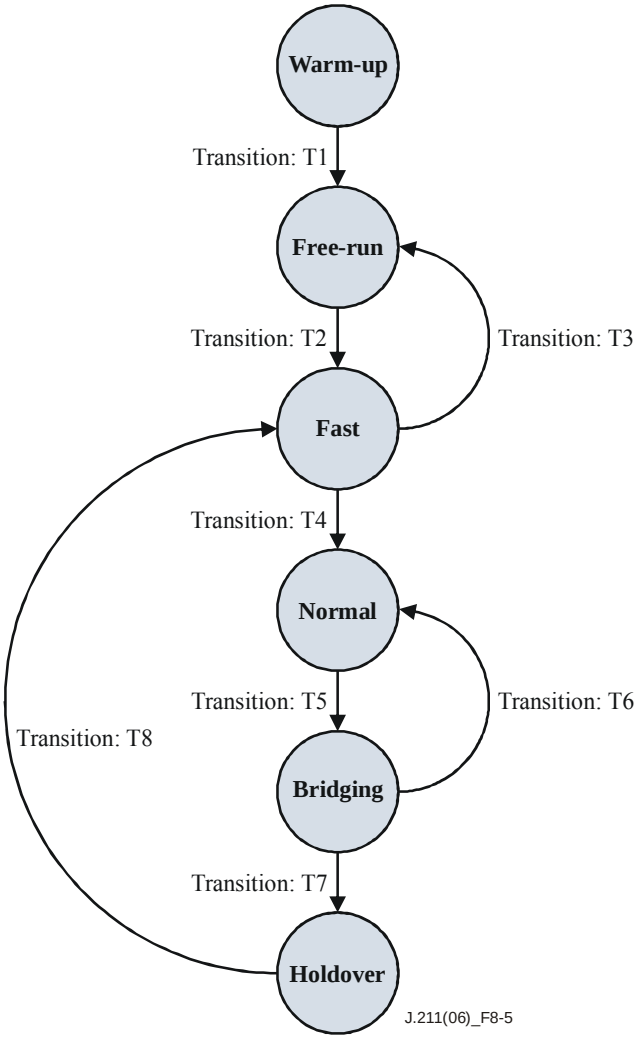


Figure 8-5 – Client mode transition diagram

8.2.4 Functional requirements

The client MUST NOT transmit while in the warm-up, free-run or holdover modes. The client MUST NOT transmit unless the most recent CRC-16 received from the server is valid. This guarantees that transmission does not occur during periods of high frame error rates.

In order to support the cable advance ranging measurement, the client frame MUST have less than 15 ns peak-to-peak jitter when in normal DTI client mode.

8.2.5 DTI client port

The DTI client port MUST be an RJ45 female connector, with the pinout as described in Table 8-4.

8.2.6 DTI client test port

The DTI client test port MUST provide the following signals:

- 10.24-MHz clock (100-ohm differential LVDS);
- 10-kHz frame clock (50-ohm LVTTL);
- DTI frame serialized data (50-ohm LVTTL).

The DTI client test port MUST use a standard seven-pin Serial-ATA header such as the Molex SD-67800-005 with the following pin assignments.

Table 8-4 – DTI client test port

Pin	Signal
1	GND
2	10.24 MHz +
3	10.24 MHz –
4	GND
5	10-kHz frame clock
6	Serialized data (client only)
7	GND

The 10.24-MHz clock will be a duplicate version of the master clock provided by the DTI client. Great care should be taken to minimize its delay and maximize its fidelity. This clock will be used for jitter, phase alignment and wander measurements.

8.2.7 DTI client test port clock

The DTI client test port clock MUST meet the double sideband phase noise requirements shown in Table 8-5 over the specified frequency ranges[6]. The DTI client clock MAY provide enhanced phase noise performance as described in Annex A.

Table 8-5 – Client phase noise

	Double sideband phase noise requirements	Jitter
10 Hz to 100 Hz	< –53 dBc	<0.035 ns RMS
100 Hz to 1 kHz	< –61 dBc	<0.014 ns RMS
1 kHz to 10 kHz	< –53 dBc	<0.035 ns RMS
10 kHz to 5.12 MHz	< –53 dBc	<0.035 ns RMS

If the DTI client is in the NORMAL or BRIDGING mode, the DTI client test port clock MUST exhibit wander below 10 Hz with a standard deviation of less than 270 ps relative to a properly functioning root DTI server 10.24-MHz test port clock.

If the DTI client is in the NORMAL mode, then the DTI client test port clock MUST maintain absolute phase alignment of ±5 ns with a fixed offset less than ±50 ns specified by the vendor. The measurement is made with respect to a properly functioning root DTI server 10.24-MHz test port clock over the full 0 to 200 metre cable length.

8.2.7.1 DTI client test port data

The DTI client test port data is a delayed version of the 5.12 Mbit/s DTI frame data. The data present on the line during the previous frame N – 1 is buffered and output by the client during frame N after the client checks the CRC received from the server in frame N – 1. If the CRC check on frame N – 1 passes, the entire 512-bit DTI frame N – 1 (server preamble, server payload, server CRC, TGT1, client preamble, client payload, client CRC, and TGT2, as illustrated in Figure 7-1 c) and detailed in clause 7.4) MUST be output serially on the client test port during frame N. Also, when the CRC check passes, the client test port MUST output 22 zeros during each turnaround guard time TGT1 and TGT2. If the check on the CRC received from the server in frame N – 1 fails,

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[6] These jitter values are 3 dB tighter than the corresponding DOCSIS 2.0 values, in order to allow for independent jitter contributions from two DTI clients respectively driving the EQAM and upstream receiver.

the client test port MUST output a dummy frame consisting of 512 ones during frame N. In any case, the client test port data output is always a continuous stream of data at a 5.12-Mbit/s rate. The data MUST be clocked out off a half rate of the 10.24-MHz clock where each bit corresponds to two 10.24-MHz clock cycles and the test port frame clock identifies both the start of the frame data, and the data bit alignment with respect to the 10.24-MHz clock. The alignment of the frame clock and test data is described in greater detail in the next clause.

8.2.7.2 DTI test port frame clock

The 10-kHz frame clock is used to frame both the serialized data and the 10.24-MHz clock edge for phase alignment measurements. Its rising edge serves a dual purpose: it identifies the first bit of the server-to-client frame preamble, and it identifies the 10.24-MHz ATP clock cycle edge that is phase-aligned to the DTI server ATP output. The frame clock falling edge identifies the first bit of the client-to-server frame preamble.

Both the frame clock and serialized data MUST maintain a minimum of 20 ns set-up time and a minimum of 0 ns hold time with respect to the 10.24-MHz clock.

A timing diagram of the frame clock and its relation to the 10.24-MHz clock and the serialized data is shown in Figure 8-6.

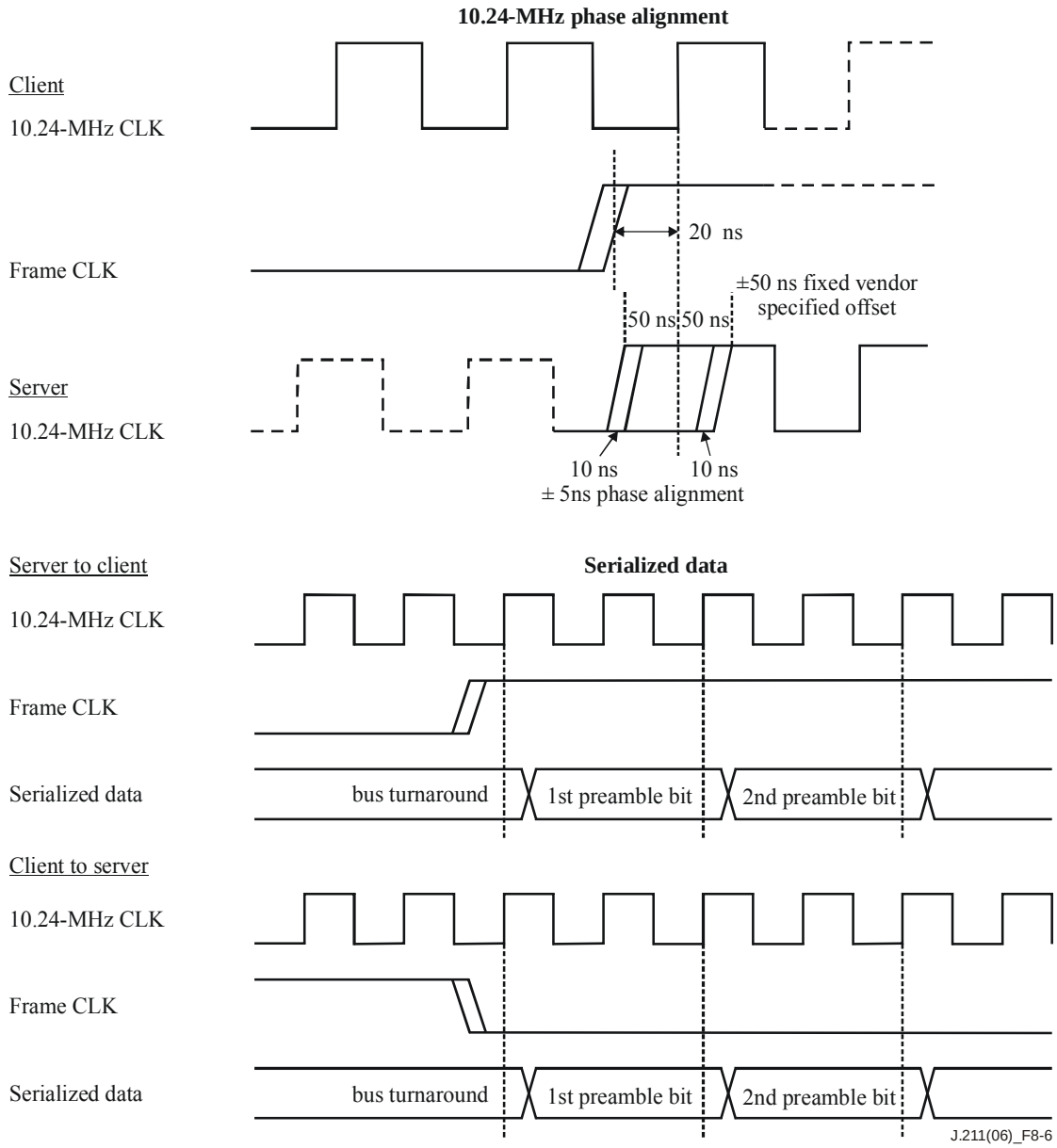


Figure 8-6 – Test port timing diagram

8.2.8 Alternative EQAM DTI testing

EQAMs MAY use their RF port in conjunction with a PPS test port instead of their DTI client test port for DTI ATP testing. The downstream symbol clock integrated phase noise measurements are measured directly on the RF port in lieu of DTI master clock jitter measurements. The SYNC messages are observed on the RF port to check DTS synchronization. A PPS test port connector MUST be available for compliance test purposes.

The PPS test port connector MAY be normally externally accessible. In this case the PPS test port connector MUST be a female BNC 50-ohm-type connector.

The PPS test port connector MAY not be normally externally accessible and will only be provided for compliance test purposes. In this case the PPS test port connector MUST be a cable-mounted male BNC 50-ohm-type connector and the cable which connects the PPS test port connector to the DTI client MUST be less than one metre in length. The method of coupling this cable to the DTI client is left to the discretion of the vendor.

Figure 8-7 shows this alternative test arrangement.

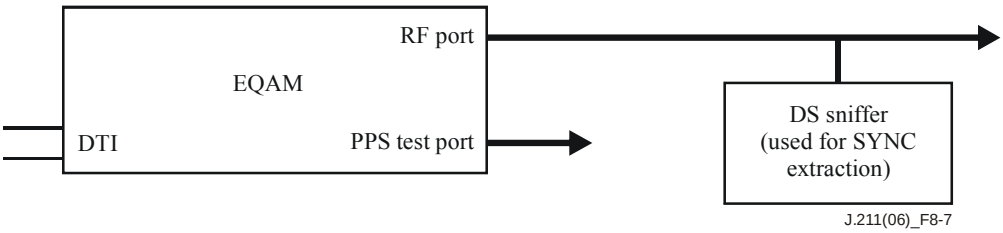


Figure 8-7 – Edge QAM test port option

The PPS test port servers a dual purpose: it identifies the gpssec time mark, and provides a phase timing reference to facilitate the measurement of two-way DTI ranging phase alignment with respect to a DTI server. If the DTI client is in the Normal mode, then the active edge of the PPS MUST maintain absolute phase alignment with respect to the server master clock test port output of ±5-ns peak, with a vendor-specified fixed offset of up to ±50 ns.

8.2.9 DTI status LEDs

The DTI status LEDs MUST be either a single green/yellow bi-colour LED or a set of two LEDs, one green and one Yellow.

The DTI status LEDs MUST be externally viewable and be integrated into, or in close proximity to, the DTI client port connector.

The DTI status LEDs MUST reflect the status of the DTI client as described in Table 8-6.

Table 8-6 – DTI status LEDs

DTI status LEDs	DTI client mode
Off	Warm-up, free-run or holdover
Yellow	Fast
Green	Normal or bridging

8.3 DTI distribution fallback strategies

Figure 8-8 shows several levels of protection that can be provisioned to establish various degrees of operational confidence in the timing distribution network.

The DTI server provides the point-to-point connections to the DTI clients. Each DTI link (a connection from server to client) is sourced from the server via a passive backplane where the physical connections are made. The server can be provisioned to provide backup for each of these connections via server-based protection cards. The protection is shown on Shelf A, but not on Shelf B. With protection cards, should an active card fail, the associated protection card provides seamless continuous function.

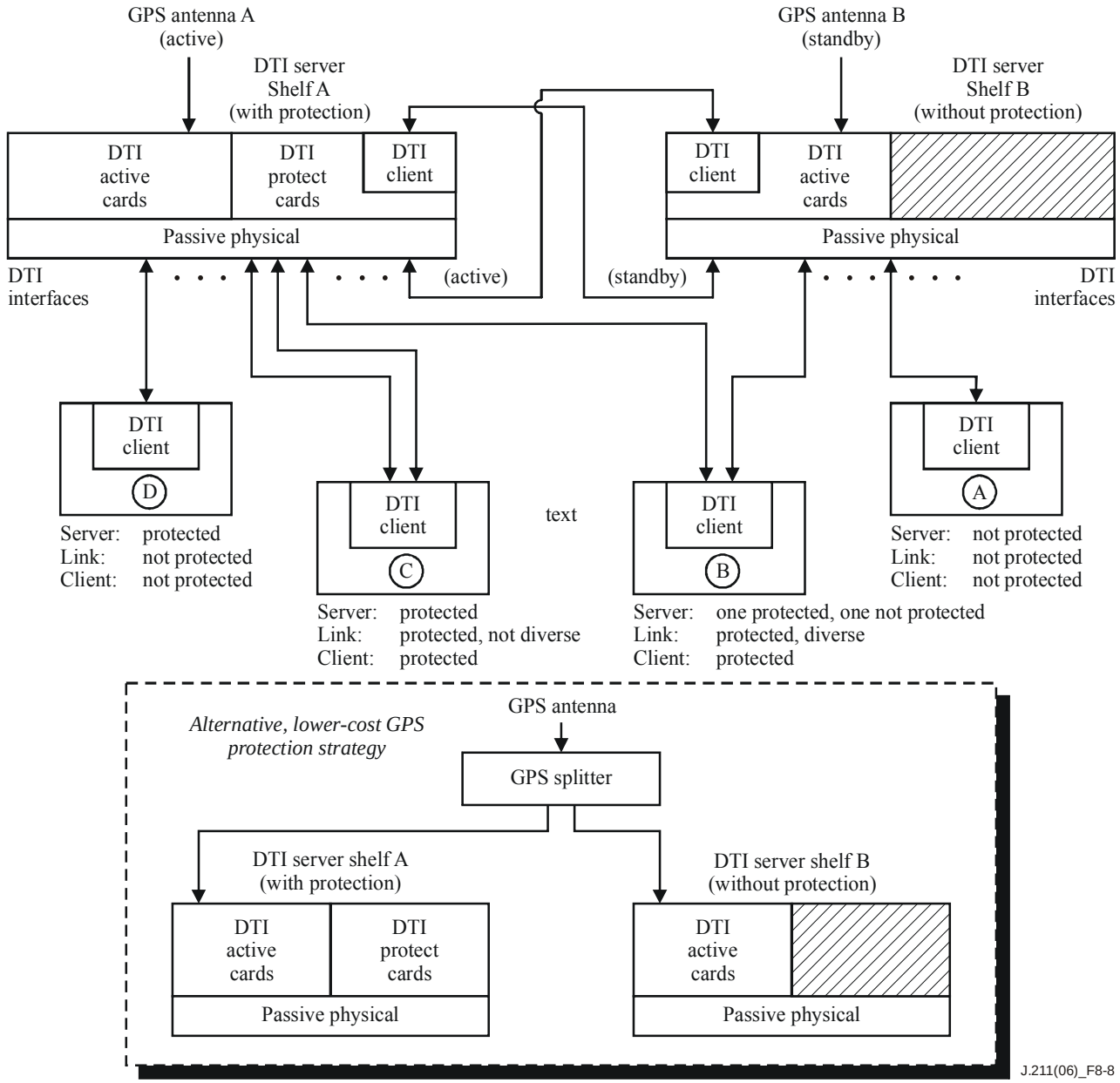


Figure 8-8 – DTI distribution fallback strategies

Figure 8-8 also shows several levels of fallback provisioning at the DTI client:

- DTI client A illustrates minimal fallback. A non-protected server has a single connection to a client.
- DTI client D illustrates a more robust fallback implementation. As with client A, client D accepts a single DTI connection, but in this case a protected server is providing it.
- DTI client C illustrates a more robust fallback implementation. Here the client accepts two DTI connections, allowing for normal operation in the event of a failure on either link.
- DTI client B illustrates a more robust fallback implementation. Client B has the same two DTI connections as client C, but in this implementation the links themselves are from diverse servers, which reduces the likelihood of both links failing (from the server side).

Multiple DTI server interconnections are also shown in Figure 8-8. To ensure best coherence (overall alignment of all timing within the timing distribution network), the preferred method is to have a single reference driving the network[7]. This reference is shown in the figure as GPS antenna A, which is actively being used by DTI server shelf A. Note that a DTI link is shown as active between server shelf A and server shelf B. Server shelf B uses a standard DTI client interface as its reference (much like any client would).

In normal operation, server shelf B is essentially "slaved" to server shelf A. In the event of a fallback on server shelf A, such as a loss of GPS via antenna A, server shelf B can become the driving shelf, using GPS antenna B (which would now become active). Server shelves A and B would reverse roles so that A would now be driven from B via the DTI link from shelf B (labelled "standby") to the DTI client shown in server shelf A.

Regarding GPS fallback in general, Figure 8-8 shows each of the server shelves connected to GPS from a different antenna, which provides fallback protection in the event of an individual antenna (or its cabling) becoming defective. The bottom of Figure 8-8 shows an alternative, lower-cost approach where a single GPS antenna is shared by the server shelves via a splitter. Of course, the antenna and cable redundancy is lost, but this method still provides GPS-quality reference availability to the timing network in the event of a single DTI server shelf failure.

[7] Alternatively, when there is no need for external traceability, the root DTI server can be free-running with no external references.

Annex A

Ranging wander qualification filter

(This annex forms an integral part of this Recommendation)

This annex specifies an ATP test fixture or method that permits the measurement of server performance as it affects the wander between two DTI clients, due to the clients' tracking of the server. Unlike a CMTS where the upstream receiver and downstream EQAM share a common chassis and implicitly negligible wander associated with the master clock, a modular system introduces distributed components and requires an allocation of ranging wander to address practical limits. The controlling specification from [ITU-T J.122] is cited for reference:

A.1 Chip timing jitter for synchronous operation

For S-CDMA mode, upstream chip clock timing error (with the mean error subtracted out) relative to the CMTS master clock MUST be less than 0.005 RMS of the chip period over a 35-second measurement interval.

Note that 0.005 chip/5.12 Mcps = 1.0 ns RMS. Figures A.1 and A.2 illustrate this DOCSIS system timing specification.

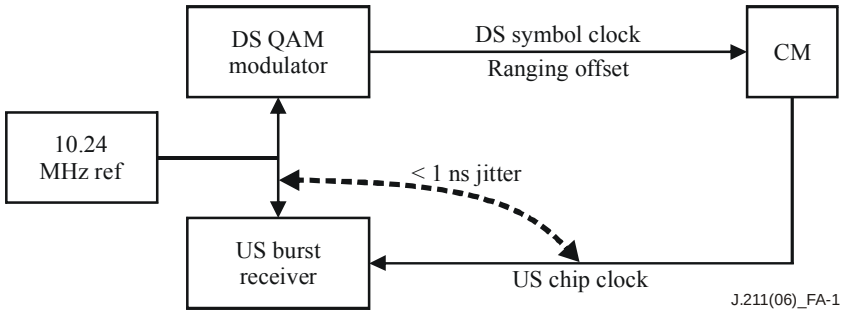


Figure A.1 – Current non-modular CMTS implementation

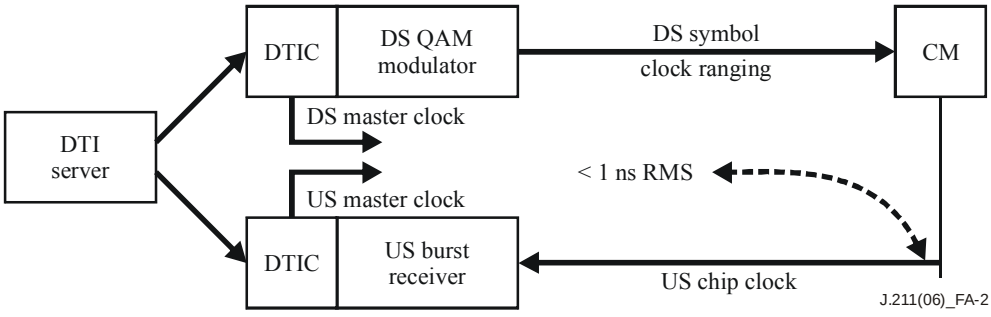


Figure A.2 – New modular CMTS implementation

As can be seen in Figure A.2, delay variation between the DS QAM version of the master clock and the US burst receiver version of the master clock will contribute to the 1-ns RMS overall system requirement. The proposed new budget is based on minimizing this effect while maintaining practical cost constraints. The 1-ns RMS budget is partitioned into a 916-ps RMS component allocated to the existing CM ranging process and a 400-ps RMS allocation to the DTI-related effects. The DTI allocation is further budgeted as shown:

1) DTI server port: 250 ps RMS ranging wander;

2) Subtending server port additional wander: 125 ps RMS;

3) Client clock local oscillator: 100 ps RMS additional wander.

Although a part of the wander will be common-mode between the two clients, the worst-case boundary is to assume that each client clock will have sufficient variation in loop parameters (bandwidth and damping factor) so that wander is uncorrelated between the two clients. Vendor implementation and aging of components (varactor gain) may contribute to this effect.

To determine the level of ranging wander noise introduced by a DTI server, the critical issue is the degree to which a client clock can track the server. The model of the client tracking suggests a bandpass filter:

1) A low-pass measurement filter to capture the capability of the client to filter high-frequency server noise.

2) A high-pass error signal filter to capture the client ability to track the server low-frequency delay variations.

The overall ranging filter is a composite of these two sections generating a bandpass filter.

The jitter filter is bounded by the minimal jitter filtering capability of a client. The maximum bandwidth is 10 Hz and the assumed filter is single pole (20 dB/decade).

The tracking filter is bounded by the minimum 1-Hz bandwidth allowance and assumes a damping factor of 3 and a type II PLL. This high-pass filter will attenuate low-frequency components with a 40-dB/decade roll-off. The combination of these two filters performance can be seen in Figure A.3:

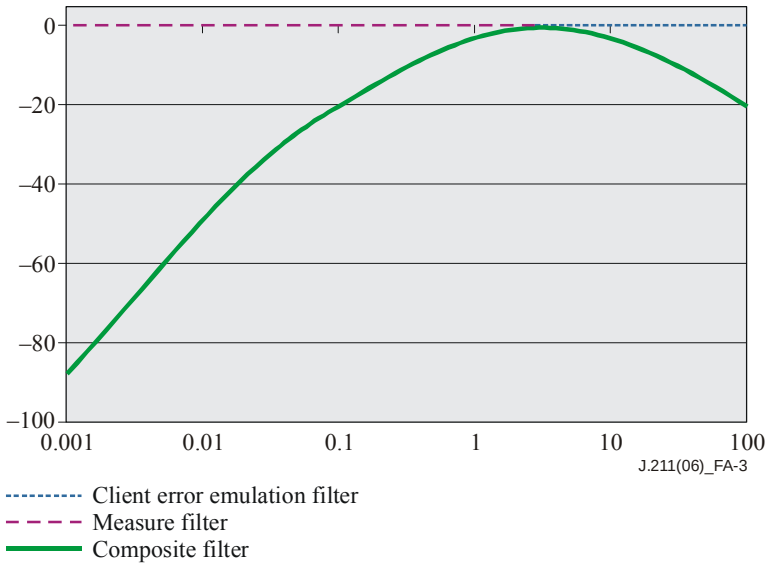


Figure A.3 – Ranging wander test filter

The ranging wander qualification filter R(S) is defined to be:

$$R(S) = E(S)M(S)$$

Where E(S) is the high-pass tracking filter and M(S) is the low-pass jitter filter.

$$E(S) = S^2/(S^2 + 5.934\ S + 0.9784)$$

$$M(S) = 1/[1 + (1/(2\pi * 10\ \text{Hz})S]$$

In the special case where the DOCSIS EQAM and upstream receivers are not collocated, there is an additional allocation of 300 ps RMS for each root server to address the phase variation over a 35-second maximum ranging interval. Stated another way, each root server is allowed a 300 ps RMS wander with respect to UTC frequency (with the mean removed). The DTI servers will be required to be traceable to GPS in both locations to obtain this level of phase coherency.

Appendix I

DTI server functional description

(This appendix does not form an integral part of this Recommendation)

This appendix provides supporting information to assist development of compliant DTI servers.

Figure I.1 illustrates a reference diagram showing the server processing function relating to external references. Vendors are free to implement alternate internal architecture as long as all DTI server requirements are met. The relationship between the gpssec time-scale and the DTI timestamp is discussed in detail in clause 7.2. This appendix discusses one method to support these requirements.

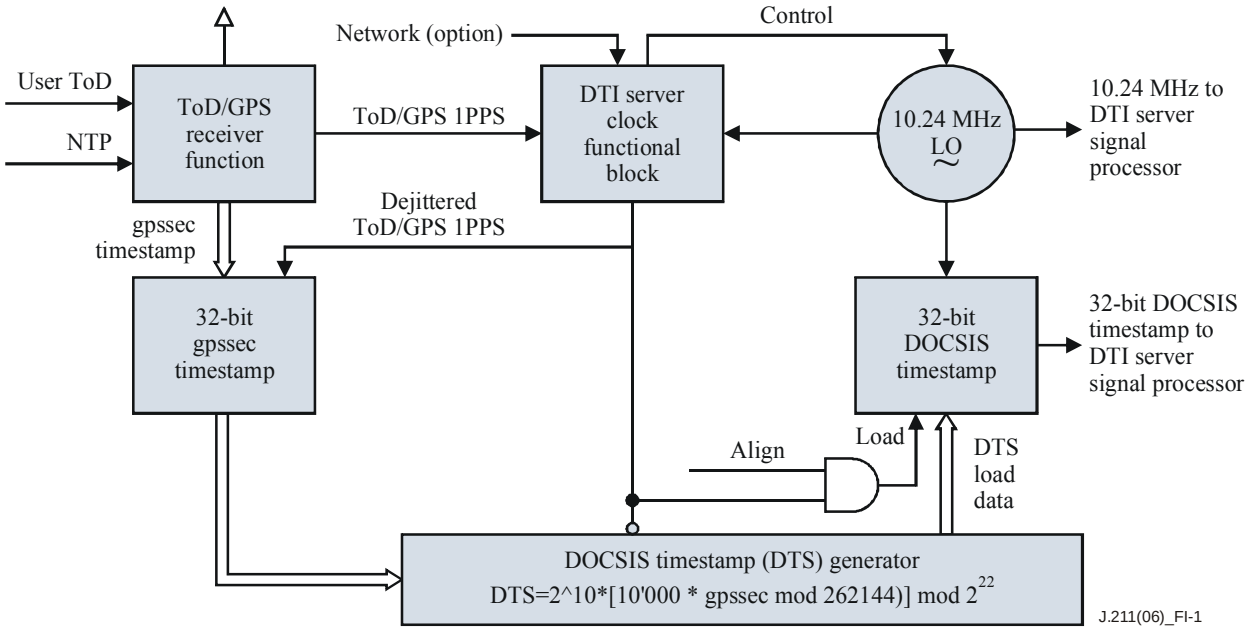


Figure I.1 – Server ToD/GPS/Network signal processing reference block diagram

The core functional block in a server is the DTI server clock. The server clock principle function is to control the 10.24-MHz master clock and a precise timing tick (shown as the dejittered 1PPS in the diagram) based on error measurement with respect to the external input. The external input may be either GPS or a network reference. The server supports a function to align the DOSCIS timestamp to the GPS time-scale (or externally supplied estimate of GPS time). The DOCSIS timestamp generator functional block illustrates this operation. The generator calculates the next DOCSIS timestamp based on the current gpssec value. This value is loaded synchronously with the dejittered ToD/GPS 1PPS signal if the alignment control is asserted. The dejittered ToD/GPS 1PPS output is maintained in tight coherency with the 10.24-MHz clock to permit a synchronous alignment of the DOCSIS timestamp within one master-clock period.

I.1 Server DTI signal processing

A block diagram of the DTI server signal processor is shown below in Figure I.2.

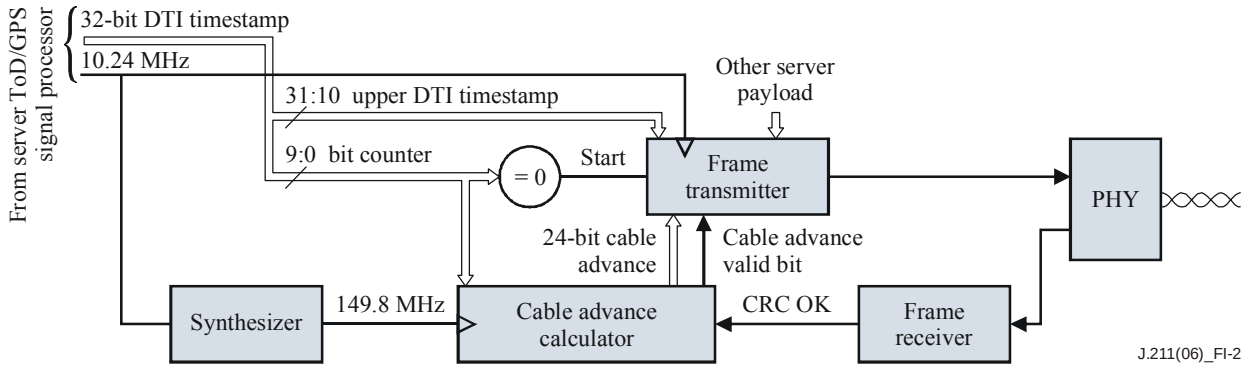


Figure I.2 – DTI server reference signal processing block diagram

The DTI server signal processor generates the DTI timing signal, receives the reply from the client, calculates the round-trip cable delay, and relays it back to the client as a cable advance value. The DTI server signal processor receives (from the ToD/GPS/External reference signal processor) a 10.24-MHz clock, and the 32-bit DOCSIS timestamp. The lower 10 bits of the DOCSIS timestamp are the actual bit counter for the DTI frame. The lower 10 bits of the DOCSIS timestamp will be referred to as "bit counter" for the rest of this explanation. The DTI frame is launched when the bit counter is zero. The DTI timing signal is clocked out using the 10.24-MHz clock (2 clocks per Manchester symbol). The DTI Frame transmitter will append the 68-bit preamble to the beginning of the frame and a 16-bit CRC to the end.

The client will receive the DTI timing signal and respond when its frame counter is at 512. The server DTI frame receiver will receive the response from the client and will issue its CRC_OK after the 16th CRC bit has been received.

A cable delay measurement circuit measures the delay of the received CRC_OK flag from where it would appear if the delay were zero. The measurement process may be started when the 10.24-MHz DTI counter is at 746[8] modulo 1024. Conceptually, if there is zero round-trip cable delay, the last bit of the CRC returning from client will arrive at the 746 server counter value. The received CRC_OK flag terminates the measurement process. This produces a raw cable delay value that is updated at a 10-kHz rate. The raw cable delay value has a resolution of one 149.8 MHz clock cycle.

A cable delay filter then processes the output of the measurement circuit. The filtering process will remove any transient values and will average the delay value. The averaging process will also produce the fractional delay value.

The 24-bit cable advance value is derived by dividing the cable delay by 2.

[8] 746 = 512 + 234.

Appendix II

DTI client functional description

(This appendix does not form an integral part of this Recommendation)

This appendix provides supporting information to assist development of compliant DTI clients.

II.1 DTI client block diagram

The block diagram shown below in Figure II.1 shows the data flow of the DTI client signal processing.

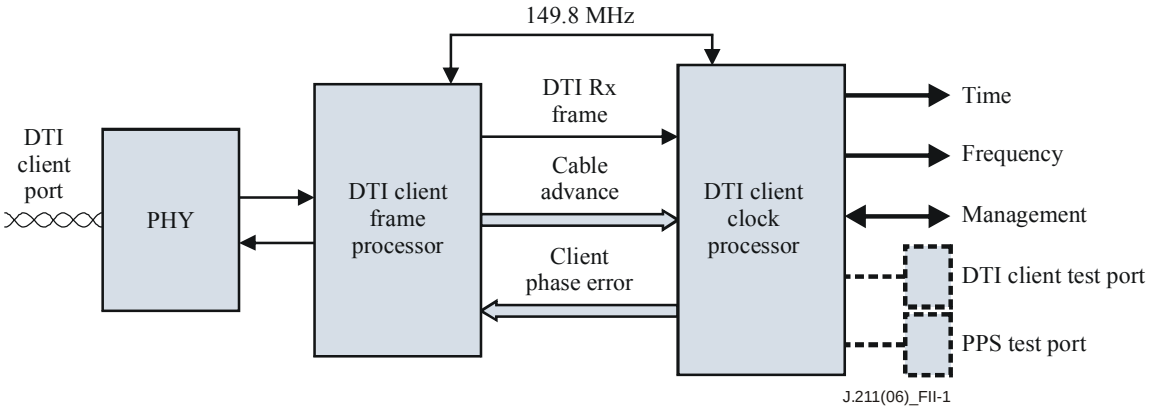
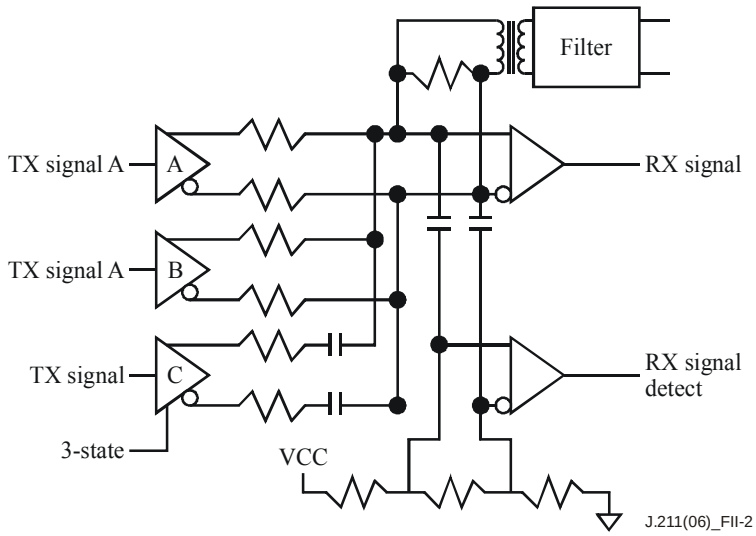


Figure II.1 – DTI client block diagram

II.2 DTI client PHY

The ping-pong DTI timing signal is passed through an EMI filter to ensure EMI compliance and minimize susceptibility. The signal then flows through a transformer to block common mode noise on the DTI timing signal. When receiving the DTI signal, driver A is fixed at '1', driver B is fixed at '0', and driver C is set to high impedance which provides a 100-ohm termination that is biased at the midpoint. The receive signal is sliced at the zero crossing to recover the data. A receive signal less than a nominal level (400 mV) is not interpreted as data. This can be accomplished by sending the receive signal through a digital comparator with a bias on the inputs as shown in Figure II.2.



MOD	Driver A	Driver B	Driver C
Transmit	DTI signal	DTI signal	DTI signal
Receive	'1'	'0'	High impedance

Figure II.2 – Example DTI PHY interface circuit

The output of the burst detector is filtered so that it will provide a steady active state while data is present. The burst detect signal is used to qualify the RX_SIG.

In the transmit direction, the drivers A, B and C are active and in phase. Drivers A and B generate the NRZ Manchester symbols simultaneously. Driver C provides pre-emphasis for the transmitted DTI signal.

II.3 DTI client frame processor

Figure II.3 shows an example of a DTI frame processor. The input to the DTI frame processor block is an NRZ Manchester-encoded digital signal from the PHY. The burst detect signal is also provided by the PHY (if available). The output from the DTI frame transmitter to the DTI PHY is a tri-state differential digital signal (DTI_TX).

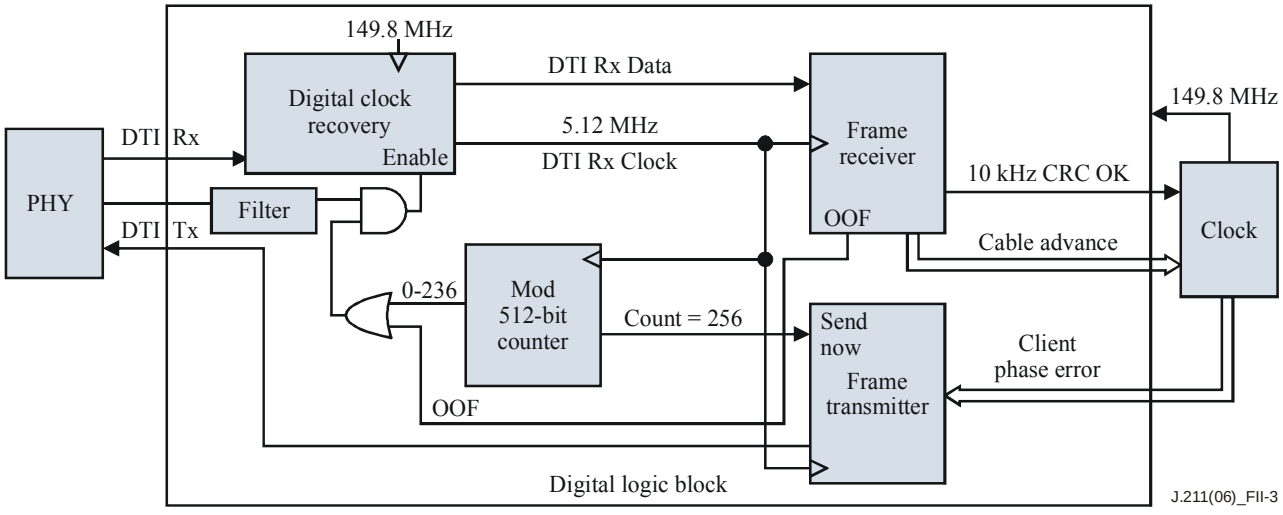


Figure II.3 – DTI client frame processor

The digital clock recovery utilizes a 149.8-MHz sample clock. This sample clock is derived from 10.24 MHz using a 512/35 multiplier. The digital clock recovery circuit operates in two states: Tracking and Flywheel. The clock recovery tracks the input signal only while the receive signal is present, and does not track the transmit signal that will be present at the input when the transmitter is enabled.

While the receive signal is not being used, the clock recovery is in the flywheel state and uses the 149.8-MHz sample clock, which is tuned to the correct frequency by the clock, to generate the carrier frequency.

Initially, the clock recovery may be gated by the filtered burst detect signal from the DTI PHY until framing is established. The client will not be transmitting until framing is established. Once framing is established, the mod 512-bit counter is aligned. Then, the bit counter is decoded and utilized to enable the clock recovery only when the client transmitted burst is completed and the burst detect is triggered.

The entire DTI client frame processor operates from the recovered 10.24-MHz server clock (and the associated 5.12-MHz Manchester bit clock) since the round-trip measurement process in the DTI server requires a fixed 256-bit 5.12-MHz symbol clock delay.

The frame receiver block detects the preamble, receives the DTI payload, checks the data integrity and generates a 10-kHz CRC OK signal that is used to steer the clock. The device type, server status flags, and server cable advance, which are part of the DTI payload, are not updated if the frame has a CRC error.

The mod 512-bit counter is decoded to locate the beginning of the transmit slot. The frame transmitter generates the preamble, serializes the payload, appends a CRC-16 cyclic redundancy checksum and sends the serial bit stream to the DTI PHY. The transmitter also reports the current client clock phase error measurement. The control signal for the transmit portion of the DTI PHY needs to be decoded from the mod 512-bit counter, and is only asserted if the receiver has properly framed.

The receive signal from the PHY will be processed by the DTI frame processor. The DTI frame processor decodes the Manchester signal, locates the end of the preamble, and then extracts the payload data. A CRC-16 check is done on the receive data, and is used to validate the payload data and generate the DTI RX frame signal. The cable advance from the payload data and the DTI RX frame signal are used to synchronize the client clock.

After the DTI frame processor has synchronized to the incoming DTI timing signal, and if the received frame is error-free, the client response is launched when the bit counter in the DTI frame processor reaches 256.

II.4 DTI client clock processor

The DTI client clock processor supports either 10.24-MHz master clock-based DOCSIS systems or 9.216-MHz-based DOCSIS systems. Reference architectures for both interworking functions are presented here for completeness.

II.4.1 10.24-MHz master clock interworking function

The client clock is built around a type II digital phase-locked loop as shown in Figure II.4. Its frequency is steered to achieve phase alignment of its local 10-kHz frame clock with respect to the 10-kHz CRC OK signal from the DTI client frame processor. The phase alignment is advanced by the cable advance value. The phase-locked loop needs to be tolerant of missing clocks since any data error will prevent the 10-kHz CRC OK from being asserted in the DTI frame processor.

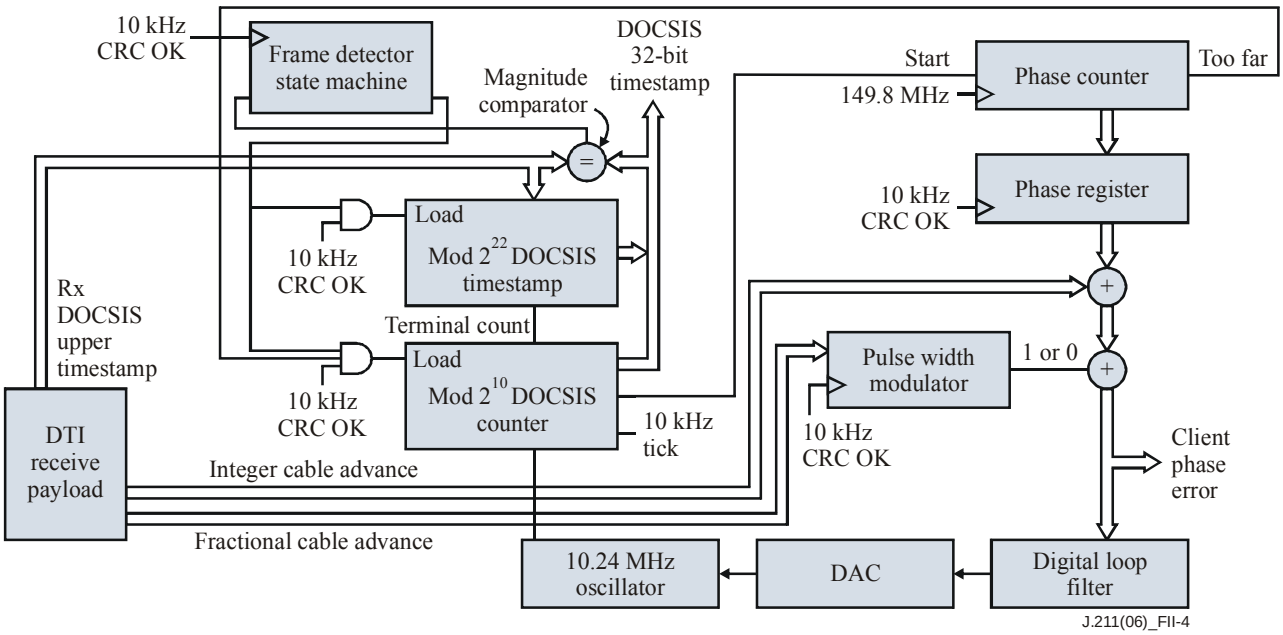


Figure II.4 – DTI clock processor (10.24-MHz)

The client clock should use a local mod 1024 DOCSIS counter to produce the lower part of the DOCSIS timestamp (the local 10-kHz frame clock), to create a DTI clock-based 10 kHz to run the DPLL phase comparator. This counter utilizes the 10.24-MHz local oscillator and the phase of the counter is controlled by the clock loop. The count value of this mod 1024 counter can be loaded if excessive phase errors exist in the clock loop to accelerate the initial lock time of the loop.

The phase counter generates the digital phase word that controls the loop. The phase can be a signed straight binary counter that is loaded with a negative value by a decoded value off of the mod 1024 counter. The preload value should be such that the phase counter passes through 0 when mod 1024 counter rolls over to 0. If the phase counter saturates, it generates the "too far" signal that is used to adjust the mod 1024 counter.

The 10-kHz CRC OK signal from the DTI frame processor is used to strobe the phase counter value into the phase register. This will cause the phase register to hold the uncorrected phase error in the loop. To correct for the cable delay the integer portion of the server cable advance, received from the payload in the frame receiver, is added to the phase counter register to create a corrected phase error value. This will cause the DPLL to lock with a phase register value that is the negative cable advance value and thus will advance the clock by that amount.

The fractional cable advance, which is a fraction of one of the 149.8-MHz clock cycles, is achieved by pulse-width modulating a 1-bit value that is added to the phase register. The pulse-width modulator creates a pulse-width that is the fractional cable advance/256 duty-cycle. The pulse-width modulator is clocked at 10 kHz since this is the phase update rate of the DPLL.

The corrected phase error is filtered by the digital loop filter and sent to an A to D converter to steer the voltage-controlled 10.24-MHz oscillator. The corrected phase error is also sent to the DTI client frame processor block to be added to the payload to be sent back to the server.

The upper 22-bit DOCSIS timestamp value, received in the DTI server payload, is compared against the mod 2^{22} DOCSIS timestamp counter and is checked at the 10-kHz CRC OK rate. A frame detector state machine checks this to determine if the two are in agreement, and if not, the local DOCSIS timestamp counter will be synchronized to the value received from the DTI server. The mod 2^{22} DOCSIS timestamp counter is only loaded if the frame detector state machine indicates

an out-of-frame condition. The upper 2^{22} DOCSIS timestamp is concatenated with the mod 1024 counter to produce the complete 2^{32} DOCSIS timestamp.

II.4.2 9.216 MHz master clock interworking function

The client clock is built around a type II digital phase-locked loop as shown in Figure II.5. Its frequency is steered to achieve phase alignment of its local 10.24-kHz pseudo-frame clock with respect to the 10.24-kHz pseudo-frame rate clock obtained from the DTI client frame processor. The 10.24-kHz pseudo-frame rate clock is obtained using the receive 5.12-MHz receive bit clock. The 5.12-MHz signal clocks the modulo 500 counter that is maintained in alignment with the receive 1 PPS. The alignment to 1 PPS ensures that the all 9.216-MHz clients operate with the same phase relationship as discussed shortly.

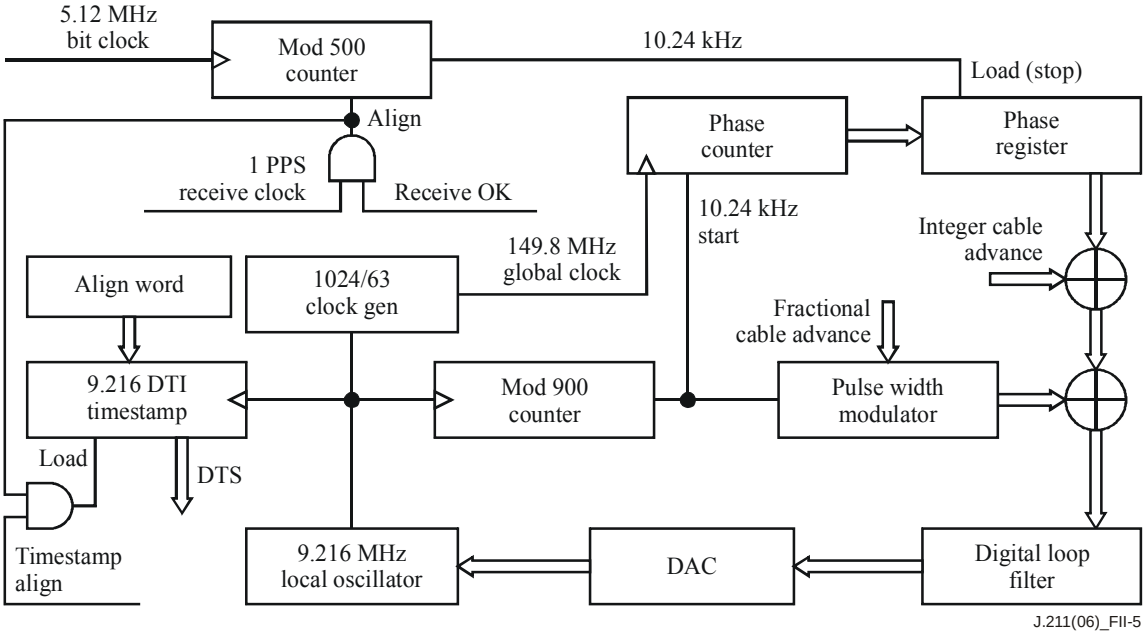


Figure II.5 – DTI clock processor (9.216 MHz)

The local and received 10.24-kHz clocks are compared to each other using a start stop counter arrangement. The clock error is measured using the 149.8-MHz global clock synthesized from the 9.216-MHz local oscillator. An M over N clock generator function with M = 1024 and N = 63 is used to obtain the global clock. The start stop counter is arranged so that zero represents alignment of the two 10.24-kHz clock sources.

If the 24-bit cable advance is zero, then the phase measurement would directly control the digital loop filter and in steady state the phase error would be zero with respect to the received pseudo-frame rate clock. Since the receive clock is delayed by the cable advance, the cable advance is injected into the loop as an additive offset forcing the local 10.24 kHz and master clock to lock early with respect to the receive clock. The advance is the correct amount to compensate for the cable delay.

One last function is the generation of the local 9.216-MHz DTI timestamp count. For clarity, the 9.216-MHz timestamp count is referred to as 9.216 DTI client DTS. The 9.216 DTI client DTS range is 2^32 counts which is the same as the DTI server DTS.

By definition, the 9.216 DTI client DTS can be assigned the value of zero at the same January 6, 1980 start epoch. At the next second the 9.216 DTI client DTS will advance to 9'216'000.

The time of coincidence is the next integer gpssec when the 9.216 DTI client DTS will be exactly zero. This will occur every 2^19 seconds (every 524'288 seconds or ~6 days)[9]. If a reset to zero process were used to synchronize every 9.216 DTI client DTS counter would require up to six days to align. The proposed process is to generate a proper initial alignment value for 9.216 DTI client DTS by the correct mapping function so that the alignment can occur on any one-second boundary.

The mapping function from gpssec to 9.216 DTI client DTS is:

$$\text{9.216 DTI client DTS} = 2^{13} * [(1125 * (\text{gpssec} \bmod 2^{19})) \bmod 2^{19}]$$

Since all the modulo operations are powers of 2, this mapping can be easily supported in the client hardware. The gpssec system time is transferred in the sub-commutated time of day field from the server.

9 The gpssec time-scale will roll over every 136 years. Since there are exactly 8'192 TOC events between roll overs, there is no disruption of the 9.216 DTI client DTS.

Appendix III

DTI jitter budget

(This appendix does not form an integral part of this Recommendation)

Figure III.1 below shows a reference model for the jitter budget analysis:

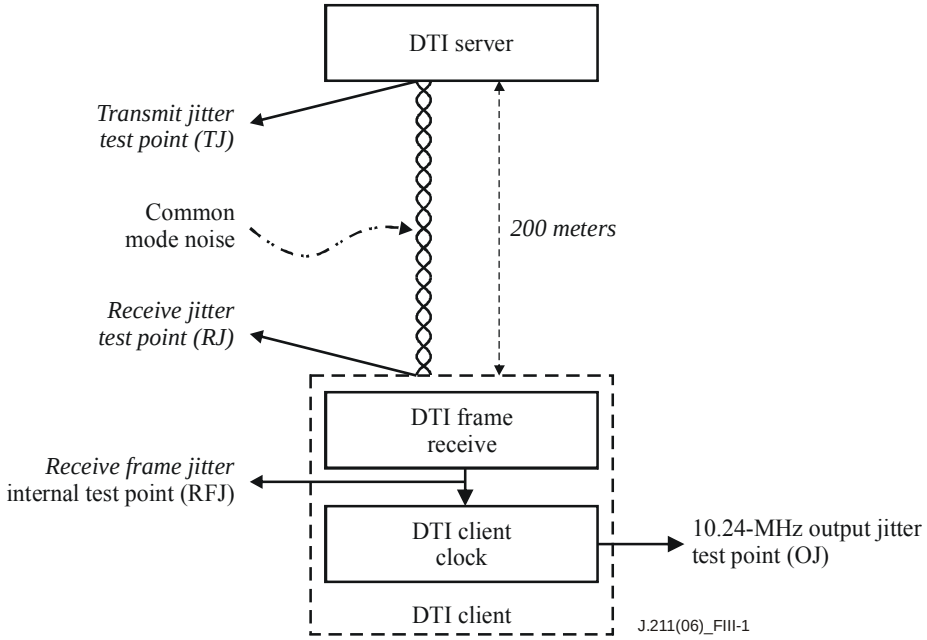


Figure III.1 – DTI jitter budget reference model

III.1 Model description

The model characterizes the accumulated jitter in the forward path (from the DTI server to the DTI client). The reverse path is not included as its impact is limited to establishing cable advance.

The output of the DTI server is a Manchester-encoded frame. The frame includes the preamble, payload and CRC and is transmitted at a 10-kHz rate. The physical layer characteristics are specified in clause 6. The principal specifications are:

- Peak differential symbol voltage: 2.2 to 2.6 V;
- Common mode source noise: <50 mV;
- 100-ohm differential impedance.

This Recommendation supports an all-ones test signal mode at the output. The transmit jitter (TJ) test point is at the DTI server RJ45 connector.

The next component is the transport. Clause 6 stipulates that the transport is UTP category 5E cable (or better) with a maximum distance limit of 200 metres. The DTI transmission is half duplex (ping-pong) and is the only wire pair active in the cable to minimize interference and optimize delay compensation.

Clause 6.4.5 specifies the common-mode rejection requirements. The induced common mode noise level is 15 V (the same as 10BT in 802.3). Both the differential noise level in voltage and edge jitter are specified.

The mapping from common mode noise to edge jitter is modelled in two steps. First the differential noise level is established based on the following:

- The model assumes a white noise common mode source at the 15-V peak level.
- The minimum common mode rejection ratio (CMRR) is specified for both the cable and the terminating transformers (35 dB).

The second step is to map the amplitude noise level to the jitter level based on the minimum slew rate of the receive signal over the cable.

This jitter performance is testable at the input DTI client RJ45 connector. The receive jitter (RJ) is modelled as the power sum of the transmit jitter and common mode induced jitter in the transport.

The DTI frame receive process recovers the receive 10-kHz frame rate from the incoming bursts. The recovery process utilizes the preamble for alignment. The vendor is free to implement the frame recovery process parameters in any method consisting with meeting the output performance objectives. The model assumes a digital PLL based on the high frequency ~149-MHz local clock used for cable advance. The bandwidth of this recovery PLL is assumed to be a maximum of one full frame or less. The receive frame jitter (RFJ) is therefore an internal test point that is included in the model to capture the jitter filtering aspects of the frame recovery process.

Finally, the DTI client clock is modelled in steady state as PLL. The reference input to the PLL is the 10-kHz receive frame process included the 149-MHz digital quantization noise.

The local oscillator is assumed to be the DTI minimum client oscillator. The loop bandwidth is assumed to be 1 Hz for this analysis.

III.2 Analysis

III.2.1 Transmit jitter specification

The high frequency jitter >10 Hz is specified to be less than 50 ps RMS. This jitter allowance accommodates the expected noise in digital drive circuitry required in a DTI server. The transmit jitter is modelled as a white noise source.

III.2.2 Receive jitter analysis

The receive jitter is the power sum of the transmit jitter and the common mode noise-related jitter. It can be viewed in the time domain as the delay variation of the receive eye-pattern. The common mode component is bounded by physical layer requirements.

The common mode induced edge jitter bound over 200 metres of cable is less than 2.005 ns RMS.

The total receive jitter is the power sum which is dominated by the common mode effect (2.01 ns RMS).

III.2.3 Receive frame jitter analysis

The edge jitter on the eye-pattern is filtered in the frame recovery process. Assuming a preamble based filtering approach the effective noise reduction factor prior to aliasing into the 10-kHz frame rate is 11.3[10]. The resulting receive frame jitter is then 177 ps RMS.

[10] Based on a particular implementation of frame clock recovery, other methods may have more or less noise suppression.

III.2.4 10.24-MHz output jitter

The output jitter is the power sum of two components:

– the jitter power of the DTI minimum oscillator in the band of interest;

– the residual jitter power of the quantized 10-kHz frame signal in the band of interest.

The output jitter given a 1-Hz loop filter bandwidth with no enhanced jitter suppression techniques is given in Table III.1.

Table III.1 – DTI 10.24-MHz output jitter performance

HPF jitter cut-off frequency [Hz] (Note 1)	Integrate Jitter in Band ps RMS			
	Residual 10-kHz input jitter (Note 2)	DTI minimum oscillator (Note 3)	DTI 10.24-MHz jitter	DOCSIS 2.0 Spec (Note 4)
10	6.8	4.02	7.9	88
100	3.44	1.55	3.8	73
1000	0.72	0.46	0.86	70

NOTE 1 – High pass from cut-off to ½ master clock rate (5.12 MHz).

NOTE 2 – Assuming worst-case common mode noise over maximum 200 metre cable distance.

NOTE 3 – Typical measured performance of a compliant voltage controlled temperature compensated oscillator (VCTCXO).

NOTE 4 – The numbers derived from the 50 ps, 20 ps, 50 ps, 50 ps integrated phase noise requirements for the master clock in DOCSIS 2.0.

The broadband jitter (10 Hz to ½ master clock) is shown in the first row. The 88-ps RMS budget is calculated from the DOCSIS 2.0 (6.3.8 of ITU-T Rec. J.122) by power summing the individual bands. In contrast, the DTI 10.24-MHz broadband jitter is 7.9 ps RMS. Recall that this jitter is under the conditions of maximum cable distance, maximum common mode noise and minimum DTI client oscillator. There is a better than 20 dB margin compared to the required master clock performance.

If we consider the direct use of the 10.24-MHz DTI signal to support RF carrier operation (with minimal additional jitter filtering), the more important aspect may be the high-frequency jitter, as the carrier recovery will track the lower frequency components.

The third row shows the integrated jitter above 1 kHz. The 10.24-MHz output directly from the client has less than 1 ps (0.86) of jitter in this band. This is better than a 38-dB margin compared to the required master clock performance in this band.

Appendix IV

Symbol clock synchronization

(This appendix does not form an integral part of this Recommendation)

In synchronous (S-CDMA) operation, the downstream symbol clock is locked to the 10.24-MHz master clock using a 16-bit integer M/N ratio.

For the standard DOCSIS and EuroDOCSIS symbol rates, the recommended M/N ratios are shown in Table IV.1.

Table IV.1 – Symbol clock synchronization

Modulation	Symbol rate	M/N
EuroDOCSIS	6.952	869/1280
DOCSIS 64QAM	5.056941	401/812
DOCSIS 256QAM	5.360537	78/149

In an M-CMTS installation, the DTI server-client distributes a phase-aligned master clock across multiple EQAMs. It is also desirable to control the phase of the symbol clocks generated by each EQAM. This can be achieved without additional signalling across the DTI interface.

The DOCSIS timestamp counter is a 32-bit counter clocked by the 10.24-MHz master clock, which rolls over every 4'294'967'296 clock cycles. Unfortunately, none of the required 'n' values divide evenly into this number.

The DTI client also provides a 'gpssec' value. 'gpssec' is a 32-bit timestamp that is incremented every second, or more accurately, every 10'240'000 cycles of the 10.24-MHz master clock.

It is convenient to declare that a positive zero-crossing of all symbol clocks occurred at the master clock edge where the 'gpssec' counter was set to "zero" (January 6, 1980). Given this, it is possible, given the 'gpssec' counter value, to determine how many master clock cycles remain before the next symbol clock positive zero-crossing, as follows:

$$\text{Master clock cycles remaining} = (\text{'gpssec'} \times 10'240'000) \text{ MOD 'N'}$$

For example, if the 'gpssec' value has just updated to 123'456, then the number of master clock cycles remaining before a positive zero-crossing of the DOCSIS 256 QAM symbol clock (M/N=78/149) is given by:

$$\text{Master clock cycles remaining} = (123'456 \times 10'240'000) \% 149 = 135$$

This means that the DOCSIS 256 QAM symbol will experience a positive zero-crossing in exactly 135 master clock cycles. This remainder value (135) can be used to 'count-down' to a reset pulse, or alternatively, can be forced directly into the divisor register of the NCO used to generate the symbol clock.

Given that the set of N values is limited, specific formulas can be used which simplify the math. Specifically, for the three values of N in the table:

N = 1'280 Master clock cycles remaining = 0

N = 812 Master clock cycles remaining = ((gpssec + roll over) MOD 203) * 680) MOD 812

N = 149 Master clock cycles remaining = ((gpssec + roll over) MOD 149) * 124) MOD 149

Note that for N = 1'280 there are exactly 8'000 divide by N cycles in a second so that the cycle remaining is constant and zero.

Since this 'N' value does not divide evenly into 2^32 × 10'240'000, this mechanism could cause a single cycle glitch when 'gpssec' rolls over. This will occur once every 136 years, and will occur first in the year 2116. To prevent this effect, a roll-over term is included. The roll over should be added starting at the roll-over event in the year 2116. The roll-over term is 74 for N = 812 and 129 for N = 149.

Appendix V

DTI high-speed clock considerations

(This appendix does not form an integral part of this Recommendation)

One key aspect of the DTI timing protocol is the adoption of the nominal 149.8-MHz DTI high-speed clock. The precise definition of the DTI high-speed clock is: 10.24 MHz * 512/35. The DTI high-speed clock permits an all-digital integrated implementation of phase measurement functions with low residual jitter and phase bias. Phase measurement is required in the client to precisely lock the client 10-kHz clock to the receive clock with cable advance applied. The server requires precise phase measurement to perform calculation of cable advance. Also digital receive clock recovery may utilize the high-speed clock to support all digital implementations. The selection of the DTI high-speed clock is a trade-off between output jitter and bias.

For example, one simple approach is to select a direct multiple of the master clock. A high-speed clock of 153.6 MHz is exactly 10.24 MHz * 15. One could consider a counter measuring the delta phase between the 10-kHz receive clock and the local client 10-kHz clock[11]. In the absence of noise, the measurement result would be static for delay changes up to the nominal 6.5 ns of the high-speed clock. While the resulting jitter would be low, the alignment error could be the full 6.5 ns. Real world noise and bias variation would yield 6.5 ns transient activity and degrade operation, especially S-CDMA precise ranging.

The selection of the non-integer (512/35 = 14.62857….) multiple generates a fractional clock dither pattern that repeats every 35 DTI timeslots as shown in Figure V.1.

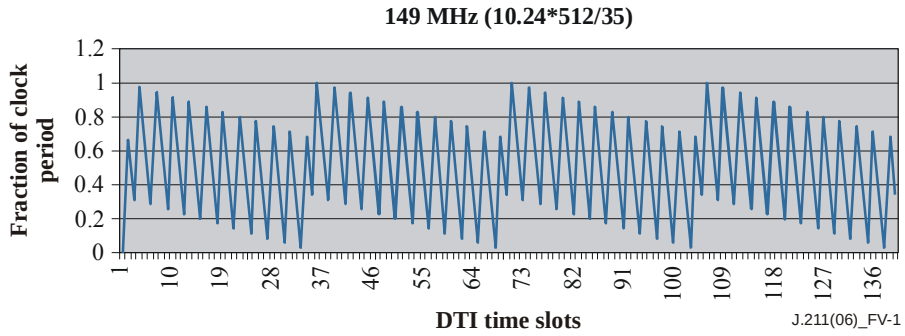
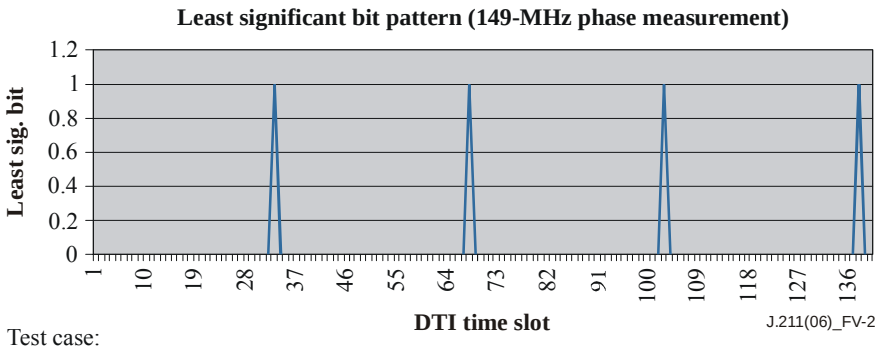


Figure V.1 – Fractional clock dither pattern

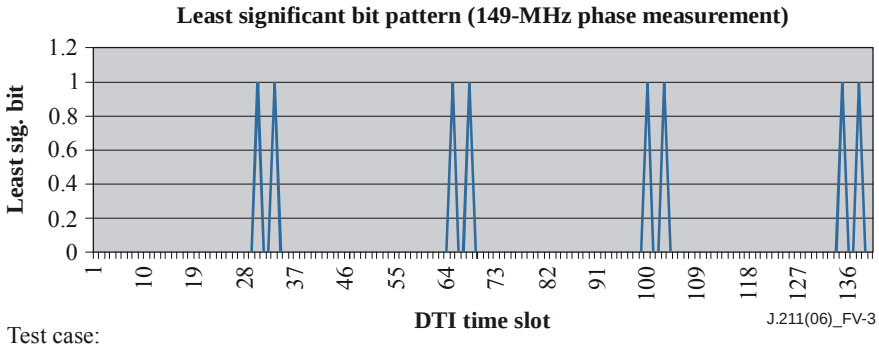
This dither pattern permits discrimination of phase shifts error to 190 ps resolution while constraining pattern jitter so that the client PLL can effectively filter it. Consider the same counter as above measuring the delta phase between the receive signal and local 10-kHz signal, but now using the 149.8-MHz DTI high-speed clock. If the phase offset is 191 ps, the least significant bit of the counter will toggle as shown in Figure V.2. The least significant bit toggles to "one" once every 35 DTI timeslots. This pattern will be averaged over the client PLL bandwidth and for a 10-Hz PLL the average phase is 187 ps with less than 5 ps residual jitter. If we increase the phase offset to 381 ps the least significant bit will now toggle as shown in Figure V.3. Now, the pattern is two "one" pulses every 35 DTI timeslots with the average output phase measurement of 374 ps and less than 5 ps of residual jitter.

[11] This is just one example where jitter and bias issues could arise. The same issues need to be considered for digital clock recovery of the DTI receive signal as well as cable delay measurement.



Test case:
Input phase bias 191 ps
Measured phase bias 187 ps

Figure V.2 – Phase measurement dither pattern 191 ps offset



Test case:
Input phase bias 381 ps
Measured phase bias 374 ps

Figure V.3 – Phase measurement dither pattern 381 ps offset

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